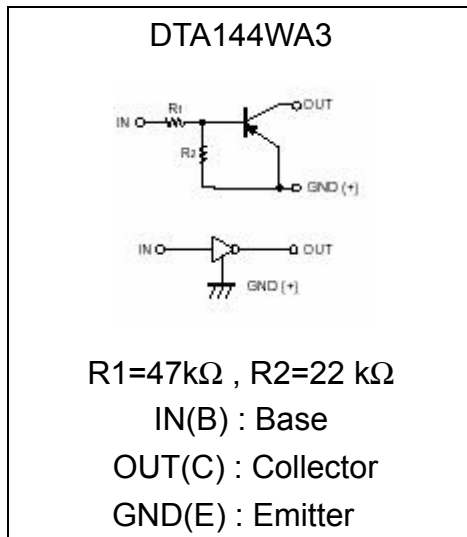
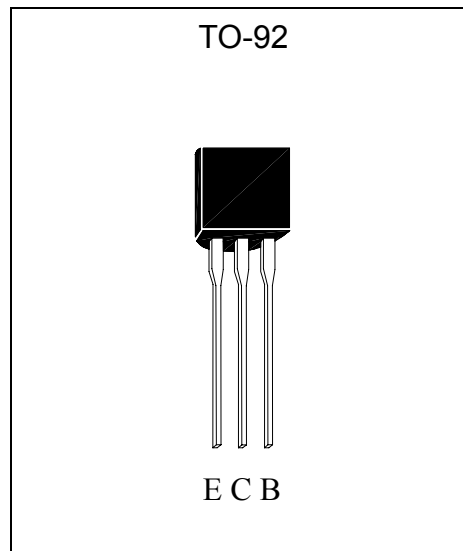


PNP Digital Transistors (Built-in Resistors)

DTA144WA3

Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTC144WA3
- Pb-free lead plating and Halogen-free package

Equivalent Circuit**Outline**

**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Supply Voltage	V _{CC}	-50	V
Collector-Base Voltage	V _{CB0}	-50	V
Collector-Emitter Voltage	V _{CEO}	-50	V
Emitter-Base Voltage	V _{EBO}	-10	V
Input Voltage	V _I	-40~+10	V
Output Current	I _O	-100	mA
	I _{O(max.)}	-100	mA
Power Dissipation @ T _A =25°C	P _d	500	mW
Thermal Resistance, Junction to Ambient	R _{θJA}	250	°C/W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-65~+150	°C
Operating Ambient Temperature	T _{amb}	-65~+150	°C

Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V _{I(off)}	-	-1.7	-1.2	V	V _{CC} =-5V, I _O =-100μA
	V _{I(on)}	-4	-2.4	-	V	V _O =-0.3V, I _O =-2mA
Output Voltage	V _{O(on)}	-	-90	-150	mV	I _O =-10mA, I _I =-0.5mA
Input Current	I _I	-	-	-0.16	mA	V _I =-5V
Output Current	I _{O(off)}	-	-	-100	nA	V _{CC} =-50V, V _I =0V
Collector Base Cutoff Current	I _{CB0}	-	-	-100	nA	V _{CB} =-50V, I _E =0A
Collector Emitter Cutoff Current	I _{CEO}	-	-	-500	nA	V _{CE} =-50V, I _B =0A
DC Current Gain	G _I	60	-	-	-	V _O =-5V, I _O =-5mA
Input Resistance	R _I	32.9	47	61.1	kΩ	-
Resistance Ratio	R ₂ /R ₁	0.37	0.47	0.57	-	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =-10V, I _C =-5mA, f=100MHz *

* Transition frequency of the device

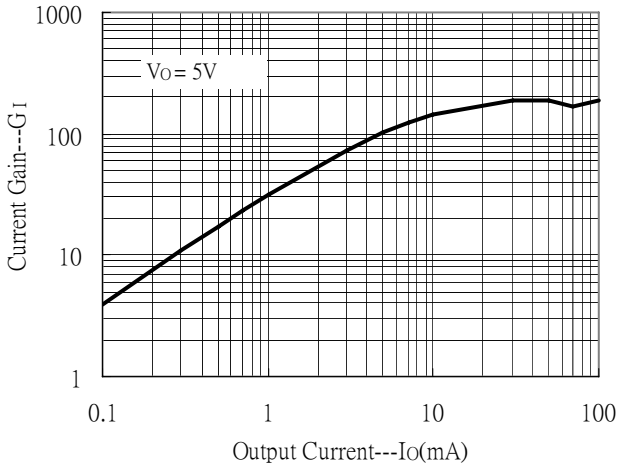
Ordering Information

Device	Package	Shipping	Marking
DTA144WA3	TO-92 (Pb-free lead plating and Halogen-free package)	2000 pcs / tape & box	A144W

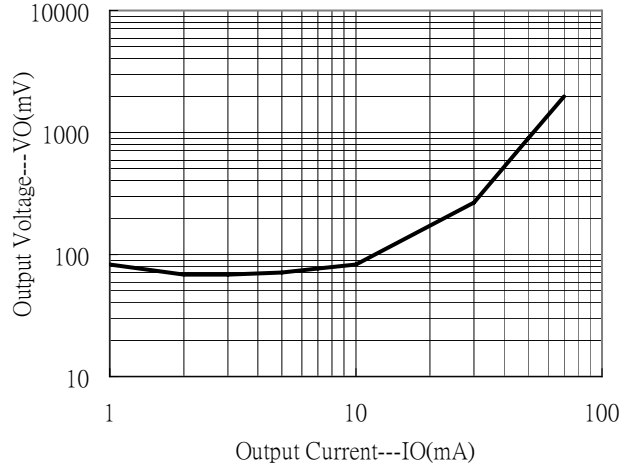


Characteristic Curves

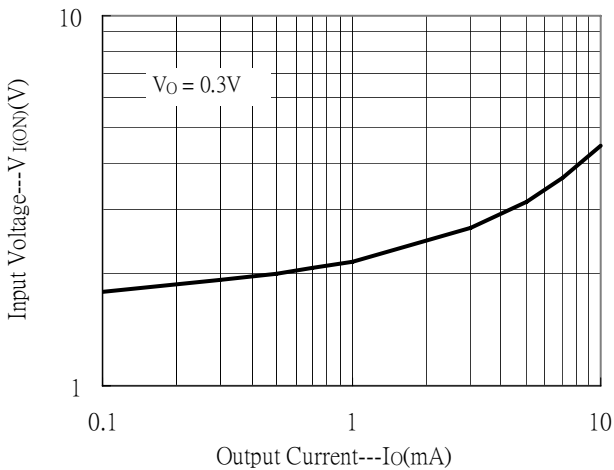
Current Gain vs Output Current



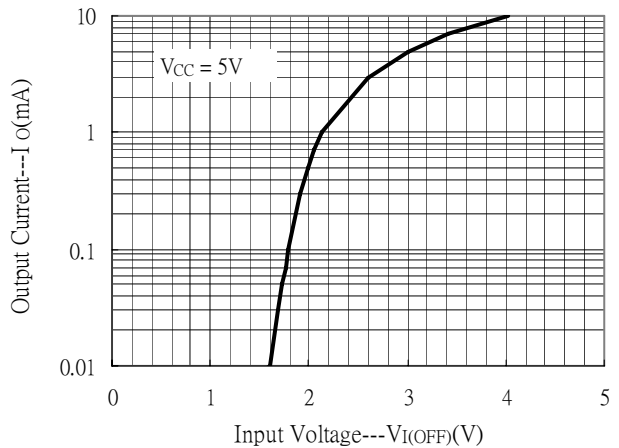
Output Voltage vs Output Current



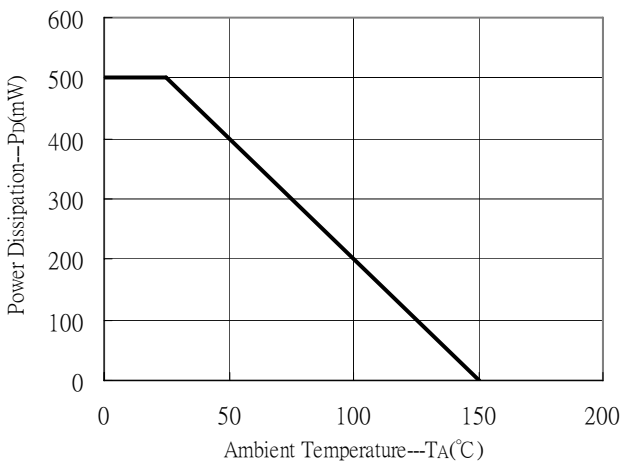
Input Voltage vs Output Current(ON characteristics)



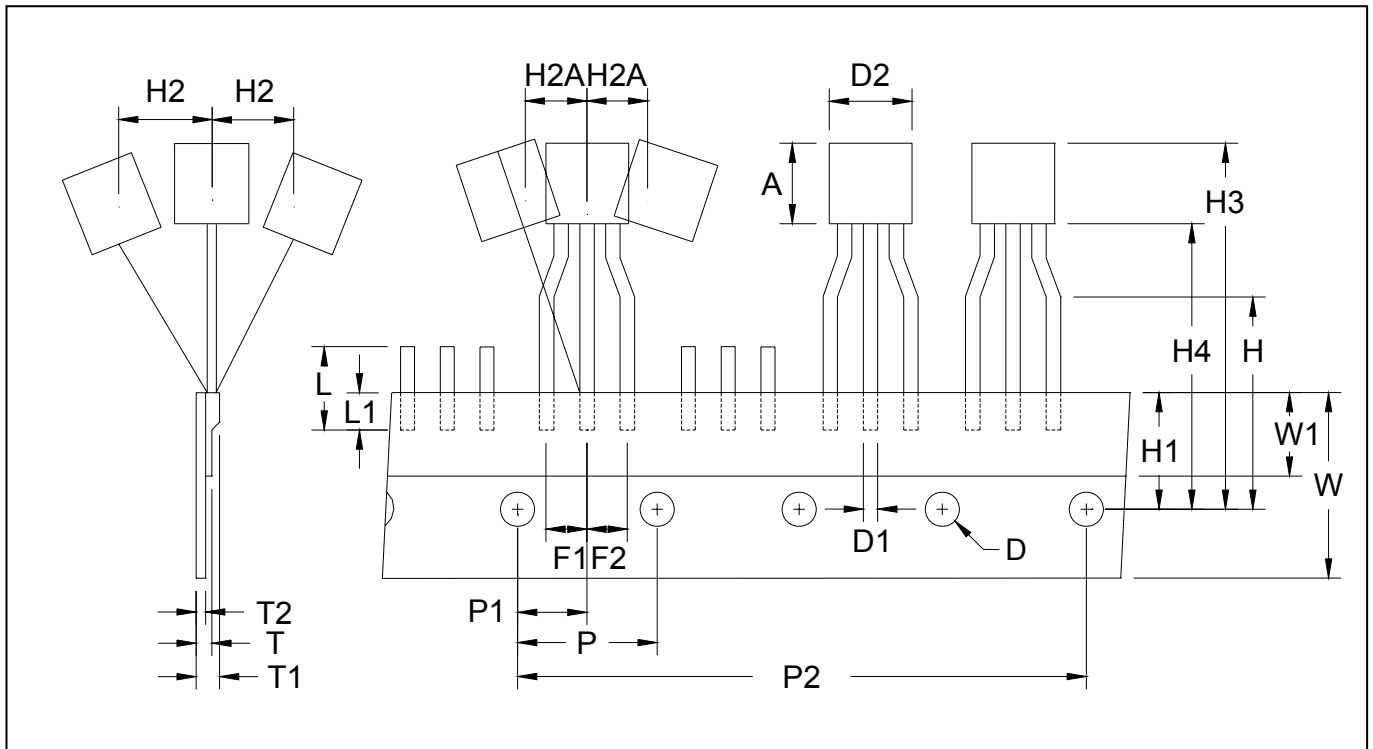
Output Current vs Input Voltage(OFF characteristics)



Power Derating Curve



TO-92 Taping Outline

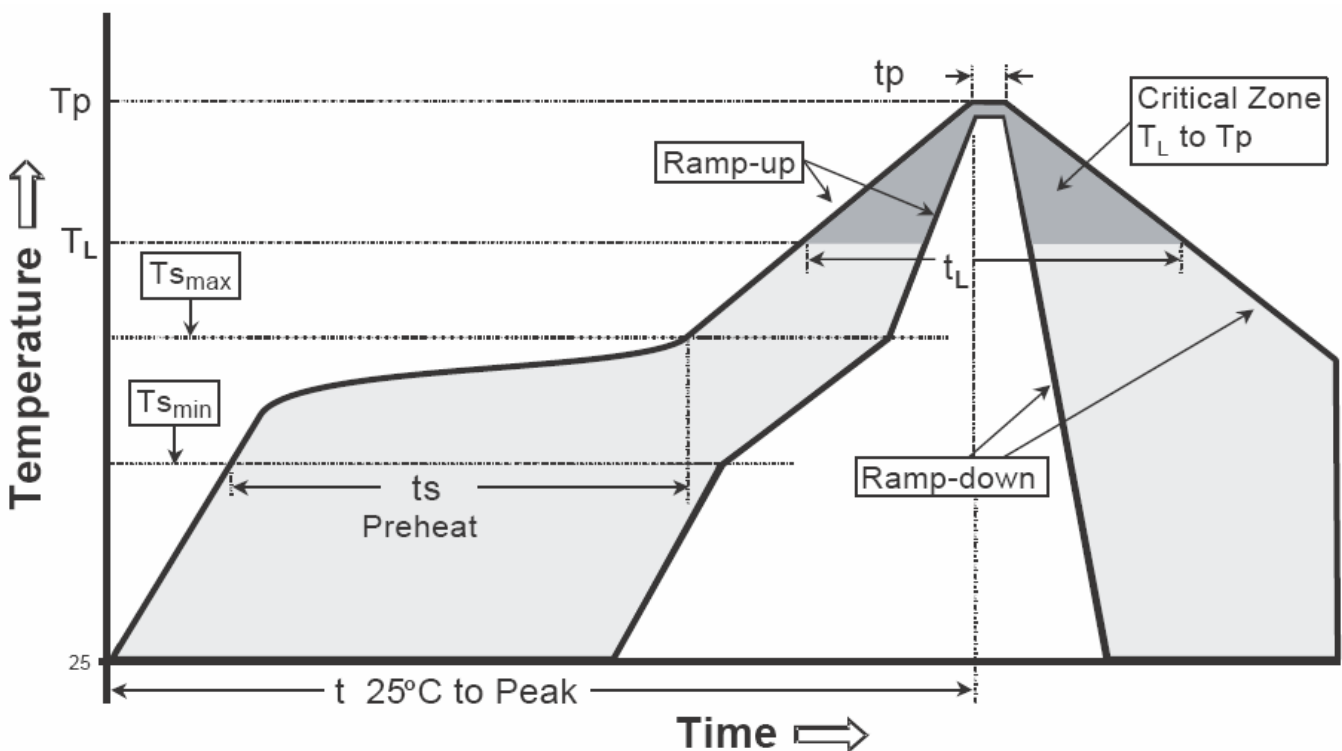


DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	265 +0/-5 °C	5 +1/-1 seconds

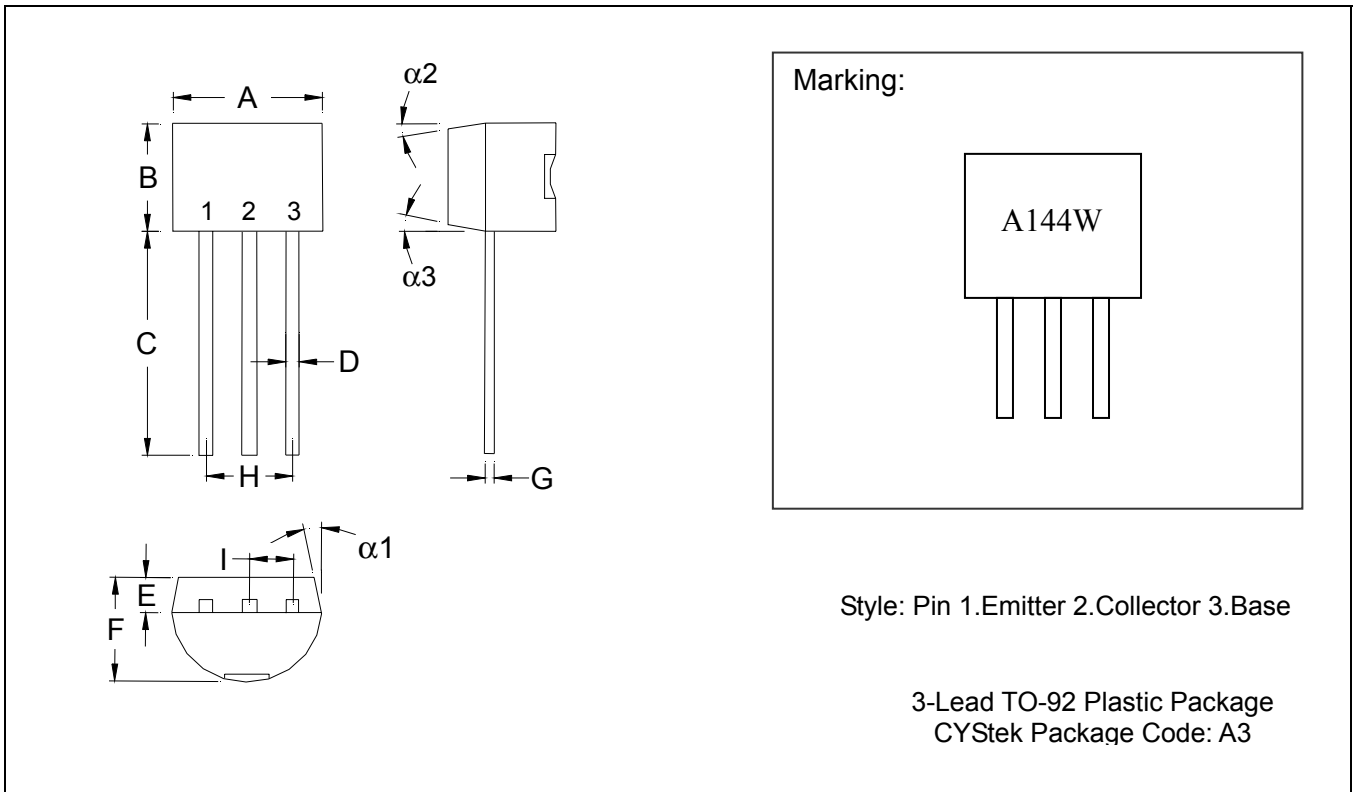
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	265 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-92 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	$\alpha 1$	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	$\alpha 2$	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	$\alpha 3$	-	*2°	-	*2°

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.