SIEMENS

High-Speed Clock and Data Recovery CDR 3300-00

Preliminary Data **Bipolar IC**

Features

- Data rate from 2.5 to 3.3 Gbit/s
- Supply range from – 4.0 V to – 5.0 V
- Supply current 350 mA typ.
- Input sensitivity 20 mVpp differential (BER = 10^{-12})
- Loss of signal (LOS) detection
- Lock indication

P-TQFP-100-4

Applications

- SH100G-based evaluation chip for CDR-macro GCDR 3300A for SDH/Sonet/ATM applications

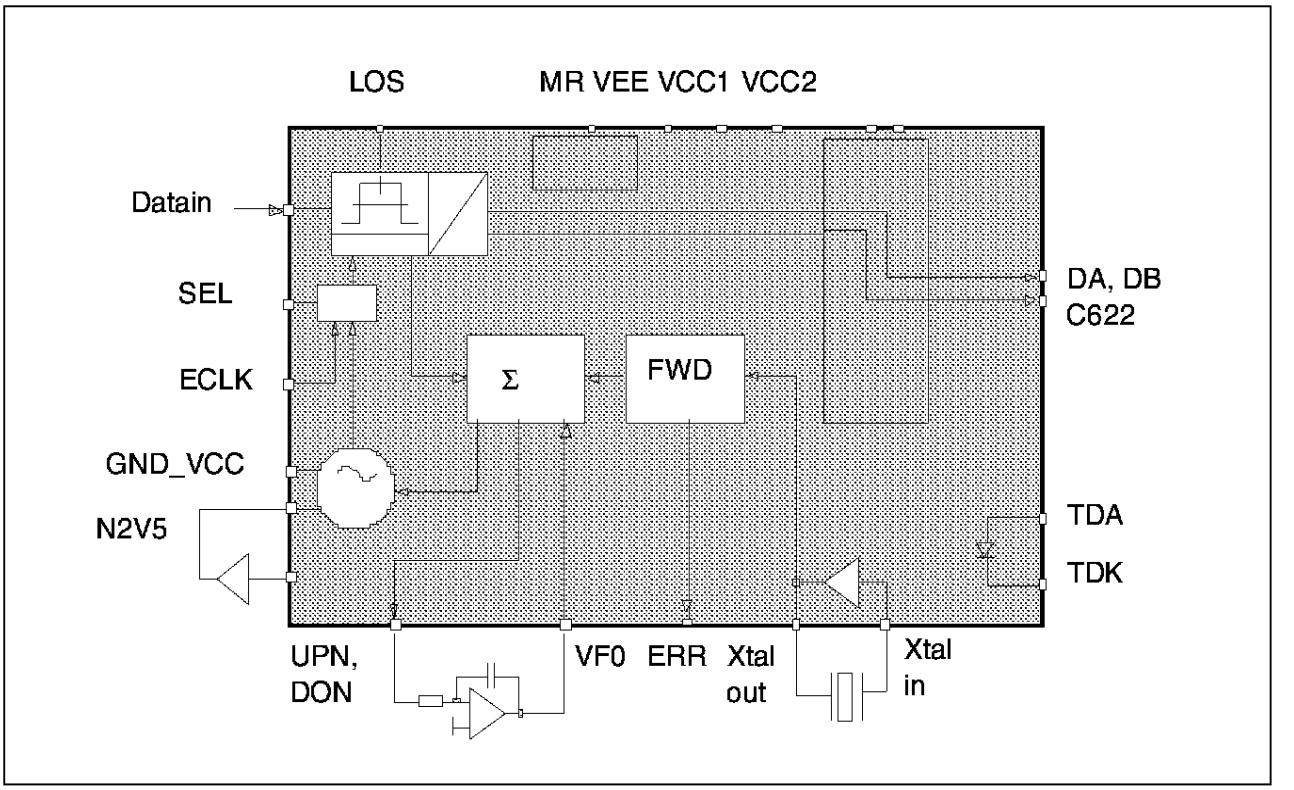

Figure 1 Block Diagram

Type	Ordering Code	Package
CDR 3300-00	on request	P-TQFP-100-4

Functional Description

CDR 3300-00 has been developed as high speed interface receiving an STM-16 channel and performing a serial to parallel conversion in order to prepare data for further high level processing at lower frequency.

High speed (2.48832 Gbit/s) NRZ serial data is applied to differential input DATAIN, DATAINN and a 2.48832 GHz master clock is recovered through a special on-chip macro cell.

The device demultiplexes the incoming data into 2 bit words which appear at the data output (DAOUT and DBOUT) and a system clock (C622OUT) is generated at 1/4 of the master clock frequency (622.08 MHz).

Details of the analog part are described in SH100G application notes as well as the frequency window detector soft macro and the LOS detector soft macro, both in the core area.

Data Recovery Characteristics

Bit rate:	2.488320 Gbit/s (ITU Rec. G.707)
Frequency	2.48832 GHz ± 20 ppm
Code:	NRZ scrambled, $1 + x^6 + x^7$ (ITU Rec. G.709), STM16 frame
Decision Sensitivity:	< 20 mVpp-differential
Phase Margin:	> 300 ps, 0.75 UI
Pattern Dependency	ITU test sequence, CID-pattern, ITU G.958
	different PRBS pattern causes no additional penalty
Power Supply Immunity	100 mVpp, f < 1 MHz

Clock Recovery Characteristics

The clock recovery function shall be able to recover a 2.488320 GHz clock from an input data stream as previously specified with the possibility of missing transitions up to 72 pulse periods. The input stream could be **wander** and **jitter** affected as specified below.

Input Jitter an Wander Tolerance (ITU Rec. G.825)

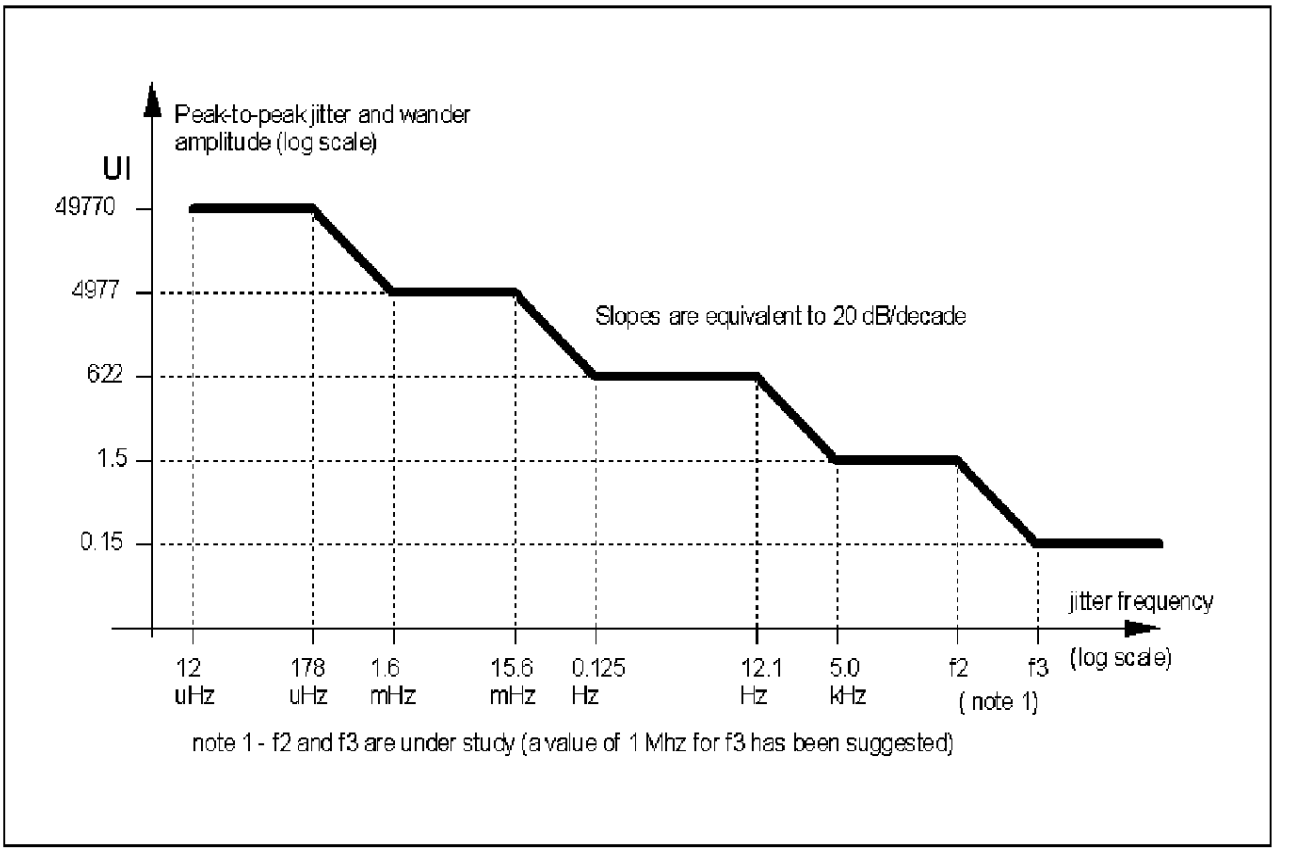

Figure 2 Lower Limit of Maximum Tolerable Jitter and Wander

Jitter Transfer Function

Jitter Transfer of CDR 3300-00

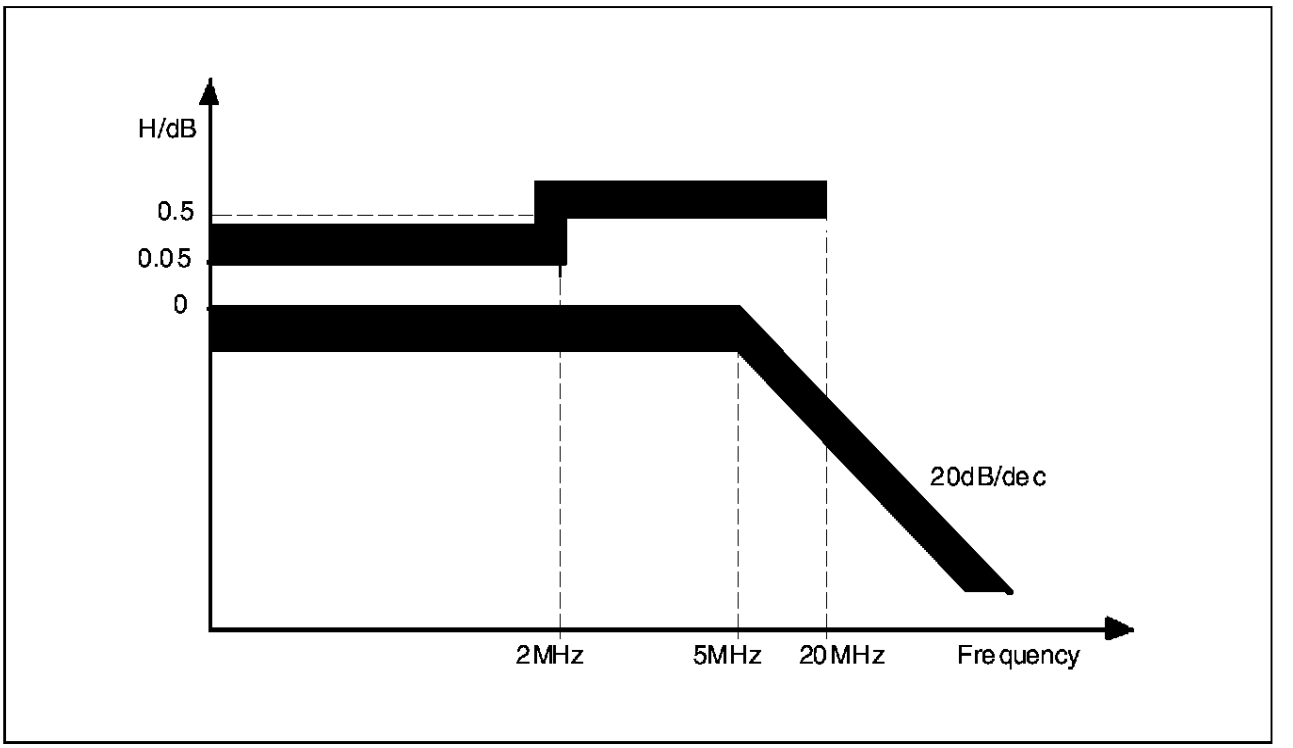

Figure 3 Jitter Transfer Function

Table 1 Pin Assignment

Protection measures have to be provided because not all pins are ESD protected.

#) no ESD protection

$) ESD protection related to VEE only

Pin	Signal Name	I/O	Type	DC-Range	AC-level (within DC range)	Term.	Description
1	VTTL	–	–	–	–	–	pos. power sup, not used, GND = 0 V
2	NC	–	–	–	–	–	–
3	XTALINN	–	–	–	–	–	not used (inverted XTALIN)
4	MR	I	–	V_{CC}, open	static	open	master reset, V_{CC} active
5	NC	–	–	–	–	–	–
6	NC	–	–	–	–	–	–
7	VCC2	–	–	–	–	–	power supply, GND = 0 V
8	VCC2	–	–	–	–	–	power supply, GND = 0 V
9	NC	–	–	–	–	–	–
10	NC	–	–	–	–	–	–
11	XTALOUTN	I$	analog	V_{CC} – 1 V, typ	250 mVpp typ	none	inv. output crystal osc. (E. Follower)
12	XTALIN	$	analog	– 1 V...0 V	–	–	buffer input crystal oscill.
13	VEE	–	–	– 4.95 V...– 4.05 V	–	–	neg. power supply
14	LOS	O#	CML	– 0.7 V...+ 5 V	1 mA ± 25%	ext. R	Output loss of signal detector
15	ERR	O#	CML	– 0.7 V...+ 5 V	1 mA ± 25%	ext. R	Output ERR detector
16	CKNNC0	O	CML	– 1 V...3 V	8 mA ± 25%	ext. R	not used open collector
17	CKN0	O	CML	– 1 V...3 V	8 mA ± 25%	ext. R	not used open collector
18	VCC2	–	–	–	–	–	power supply, GND = 0 V
19	VCC2	–	–	–	–	–	power supply, GND = 0 V
20	NC	–	–	–	–	–	–
21	NC	–	–	–	–	–	–
22	NC	–	–	–	–	–	–
23	TDK	–	analog	VEE...V_{CC}	I_{out} = 100 µA, typ	–	temperature diode cathode
24	TDA	–	analog	VEE...V_{CC}	I_{in}= 100 µA, typ	–	temperature diode anode
25	VTTL	–	–	–	–	–	pos. power sup, not used, GND = 0 V
26	NC	–	–	–	–	–	–
27	NC	–	–	–	–	–	–

Table 1 Pin Assignment (cont'd)

Protection measures have to be provided because not all pins are ESD protected.

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Pin	Signal Name	I/O	Type	DC-Range	AC-level (within DC range)	Term.	Description
28	NC	–	–	–	–	–	
29	VCC1	–	–	–	–	–	power supply, GND = 0 V
30	VCC1	–	–	–	–	–	power supply, GND = 0 V
31	NC	–	–	–	–	–	–
32	NC	–	–	–	–	–	–
33	NC	–	–	–	–	–	–
34	VEE	–	–	– 4.95 V...– 4.05 V	–	–	neg. power supply
35	VEE	–	–	– 4.95 V...– 4.05 V	–	–	neg. power supply
36	NC	–	–	–	–	–	–
37	NC	–	–	–	–	–	–
38	VCC1	–	–	–	–	–	power supply, GND = 0 V
39	NC	–	–	–	–	–	–
40	NC	–	–	–	–	–	–
41	VCC2	–	–	–	–	–	power supply, GND = 0 V
42	VCC2	–	–	–	–	–	power supply, GND = 0 V
43	NC	–	–	–	–	–	–
44	NC	–	–	–	–	–	–
45	NC	–	–	–	–	–	–
46	VCC1	–	–	–	–	–	power supply, GND = 0 V
47	VCC1	–	–	–	–	–	power supply, GND = 0 V
48	NC	–	–	–	–	–	–
49	NC	–	–	–	–	–	–
50	NC	–	–	–	–	–	–
51	VTTL	–	–	–	–	–	pos. power sup, not used, GND = 0 V
52	NC	–	–	–	–	–	–
53	NC	–	–	–	–	–	–
54	ECLK	I	ECL100k	V_{CC} – 2 V... V_{CC}	400 mVpp typ	ext.	clock 2.5 GHz input, only for test
55	ECLKN	I	ECL100k	V_{CC} – 2 V... V_{CC}	400 mVpp typ	ext.	clock 2.5 GHz input inv., only for test
56	N2V5	–	–	– 2.5 V typ, 15 mA	–	–	neg. power supply VCO

Table 1 Pin Assignment (cont'd)

Protection measures have to be provided because not all pins are ESD protected.

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Pin	Signal Name	I/O	Type	DC-Range	AC-level (within DC range)	Term.	Description
57	VCC2	–	–	–	–	–	power supply, GND = 0 V
58	VCC2	–	–	–	–	–	power supply, GND = 0 V
59	DATAIN	I#	analog	– 0.6 V...+ 0.25 V	20...500 mVpp	int. 50 Ω to VCCZ1	RF data input 2500 Mbit/s
60	VCCZ1	–	–	–	–	–	power supply VCO, GND = 0 V
61	DATAINN	I#	analog	– 0.6 V...+ 0.25 V	20...500 mVpp	int. 50 Ω to VCCZ1	RF data input inv. 2500 Mbit/s
62	VCCZ2	–	–	–	–	–	power supply VCO, GND = 0 V
63	VEE	–	–	– 4.95 V...– 4.05 V	–	–	neg. power supply
64	VF0	I	analog	VEE... V_{CC}, 6 mA	– 2.5 V... – 2.0 V typ	–	VCO control input, integrator output
65	UPN	O	CML	– 1 V...3 V	1 mA ± 25%	int. 800 Ω	inverted PD/FD output UP
66	DON	O	CML	– 1 V...3 V	1 mA ± 25%	int. 800 Ω	inverted PD/FD output down
67	VBB	O$	analog	I_{out} < 100 µA	–	–	Reference voltage – 1.3 V
68	VCC2	–	–	–	–	–	power supply, GND = 0 V
69	VCC2	–	–	–	–	–	power supply, GND = 0 V
70	SEL	I	ECK100k	active H	static		enable ext. clock 2.5 GHz input, P.D.
71	NC	–	–	–	–	–	–
72	NC	–	–	–	–	–	–
73	NC	–	–	–	–	–	–
74	NC	–	–	–	–	–	–
75	VTTL	–	–	–	–	–	pos. power supply, not used
76	DAOUT	O	CML	– 1 V ... 3 V	8 mA ± 25%	int 100 Ω	Data output 1244 Mbit/s
77	DAOUTN	O	CML	– 1 V ... 3 V	8 mA ± 25%	int 100 Ω	Data output 1244 Mbit/s inv.
78	DBOUT	O	CML	– 1 V ... 3 V	8 mA ± 25%	int 100 Ω	Data output 1244 Mbit/s
79	VCC1	–	–	–	–	–	power supply, GND = 0 V

Table 1 Pin Assignment (cont'd)

Protection measures have to be provided because not all pins are ESD protected.

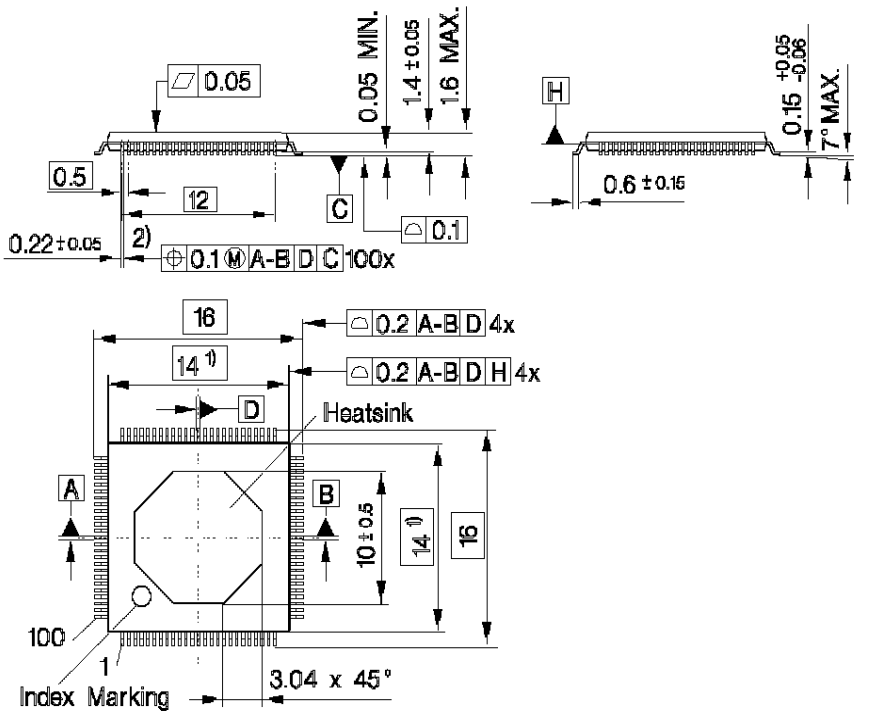
#) no ESD protection

$) ESD protection related to VEE only

Pin	Signal Name	I/O	Type	DC-Range	AC-level (within DC range)	Term.	Description
80	VCC1	–	–	–	–	–	power supply, GND = 0 V
81	DBOUTN	O	CML	– 1 V ... 3 V	8 mA ± 25%	int 100 Ω	Data output 1244 Mbit/s inv.
82	C622OUT	O	CML	– 1 V ... 3 V	8 mA ± 25%	int 100 Ω	Clock output 622 MHz
83	C622OUTN	O	CML	– 1 V ... 3 V	8 mA ± 25%	int 100 Ω	Clock output 622 MHz inv.
84	VEE	–	–	– 4.95 V...– 4.05 V	–	–	neg. power supply
85	VEE	–	–	– 4.95 V...– 4.05 V	–	–	neg. power supply
86	SC622OUT	O	ECL	– 1 V ... 3 V	–	ext. R	Clock output 622 Mbit/s
87	SC622OUTN	O	ECL	– 1 V ... 3 V	–	ext. R	Clock output 622 Mbit/s inv.
88	VCC1	–	–	–	–	–	power supply, GND = 0 V
89	NC	–	–	–	–	–	–
90	NC	–	–	–	–	–	–
91	VCC2	–	–	–	–	–	power supply, GND = 0 V
92	VCC2	–	–	–	–	–	power supply, GND = 0 V
93	NC	–	–	–	–	–	–
94	NC	–	–	–	–	–	–
95	NC	–	–	–	–	–	–
96	VCC1	–	–	–	–	–	power supply, GND = 0 V
97	VCC1	–	–	–	–	–	power supply, GND = 0 V
98	NC	–	–	–	–	–	–
99	NC	–	–	–	–	–	–
100	NC	–	–	–	–	–	–

Package Outlines

P-TQFP-100-4
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

27

The package is a Thermal-Plastic-Quad-Flat-Pack with 100 pins, P-TQFP-100-4 and includes a heat-slug in order to attach an additional heatsink.

The heat-slug is connected to the negative power supply.

For the heat sink attach no soldering procedure is allowed, glueing only.

Thermal Resistance R_{thJC} = 4 K/W, R_{thJA} = 36 K/W

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm