AIE Adaptive Image Enhancer Series

Real Time Video Processor IC

BU1574GUW

No.09060EAT04

●Description

BU1574GUW is AIE : Adaptive Image Enhancer (image processing technology by ROHM's hardware).

●Features

1) Compatible with image data from QCIF size (176 × 144) up to WVGA+ size (864 × 480).
2) Compatible with I/O data formats of ITU-R BT.656-4 or YCbCr with synchronizing signals.
3) Multiple operation modes: Image Enhance, Through and Sleep.
4) Registers can be set up through the 2-wire serial interface (I^2C).
5) PWM output for image adjustment LCD backlight control.
6) Built-in edge-enhancement and gamma filters.

●Applications

Car camera, Car display, Car navigation system, Mobile phone, and portable DVD etc.

●Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Power supply voltage 1	VDDIO	-0.3～+4.2	V
Power supply voltage 2	VDD	-0.3～+2.1	V
Input voltage	VIN	-0.3～VDDIO+0.3	V
Storage temperature range	Tstg	-40～+125	℃
Power dissipation	PD	310[*1],570[*2]	mW

*1 IC only. In the case exceeding 25 °C, 3.1 mW should be reduced per 1 °C.
*2 When mounted on a glass epoxy board of 70 x 70 x 1.6 mm. If exceeding 25 °C, 5.7 mW should be reduced per 1 °C.
* Has not been designed to withstand radiation.
* Operation is not guaranteed.

●Operating conditions

Parameter	Symbol	Rating	Unit
Power supply voltage 1 (IO)	VDDIO	2.70～3.60(Typ:3.00)	V
Power supply voltage 2 (CORE)	VDD	1.40～1.60(Typ:1.50)	V
Input voltage range	VIN-VDDIO	0～VDDIO	V
Operating temperature range	Topr	-40～+85	℃

* Supply the power source in order of VDD → VDDIO.

●Electrical characteristics

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input frequency	f_{IN}	-	-	36.0	MHz	CAMCKI (DUTY45%～55%)
Operating current consumption	IDD1	-	24	-	mA	At Enhance mode setting (36 MHz).
Static current consumption	IDDst	-	-	30	uA	At Sleep mode setting input terminal= GND setting
Input "H" current	IIH	-10	-	10	uA	VIH=VDDIO
Input "L" current	IIL	-10	-	10	uA	VIL=GND
Input "H" voltage 1	VIH1	VDDIO x0.8	-	VDDIO +0.3	V	Normal input (including the input mode of I/O terminal)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO x0.2	V	Normal input (including the input mode of I/O terminal)
Input "H" voltage 2	VIH2	VDDIO x0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC, I2CDEV0)
Input "L" voltage 2	VIL2	-0.3	-	VDDIO x0.15	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC, I2CDEV0)
Hysteresis voltage width	Vhys	-	0.7	-	V	Hysteresis input (RESETB, CAMCKI, SDA, SDC, I2CDEV0)
Output "H" voltage	VOH	VDDIO -0.4	-	VDDIO	V	IOH = -1.0 mA (DC) (including the output mode of I/O terminal)
Output "L" voltage	VOL	0.0	-	0.4	V	IOL = 1.0 mA (DC) (including the output mode of I/O terminal)

(Unless otherwise specified; VDD = 1.50 V, VDDIO = 3.00 V, GND = 0.0 V, Ta = 25 ℃, fIN = 36.0 MHz)

●Terminal Layout

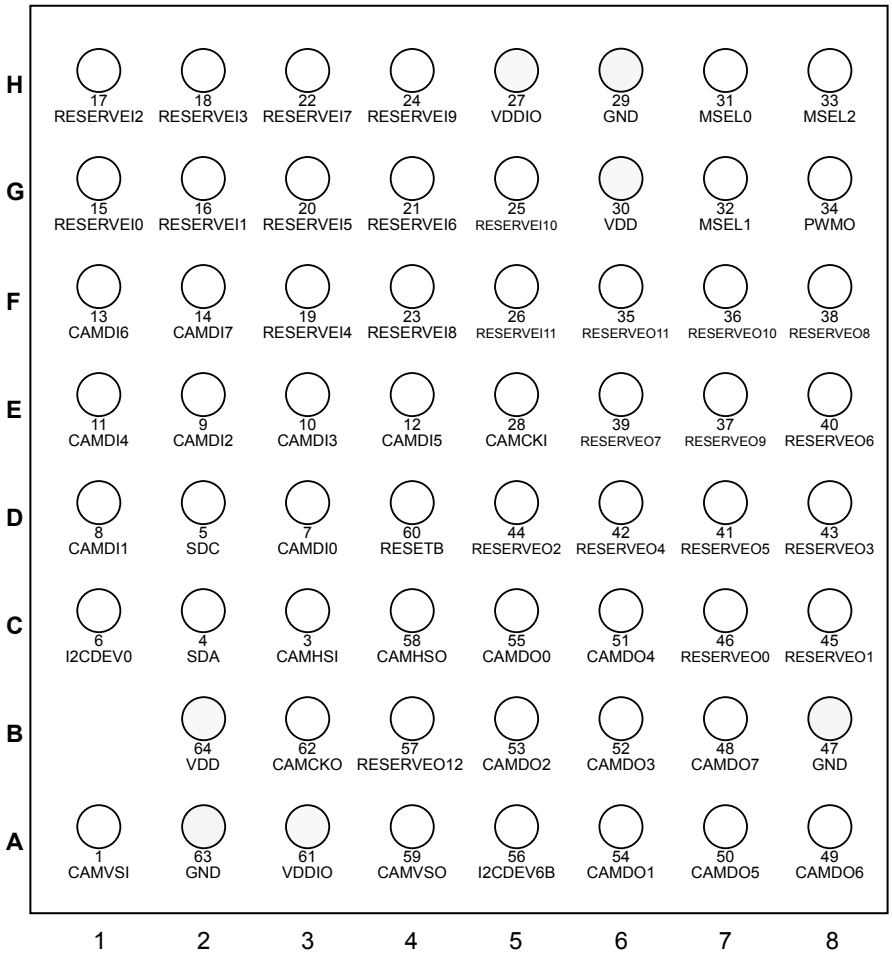


Fig.1 Terminal Layout (Bottom View)

●Terminal functions

PIN No.	Pin Name	In/Out	Active Level	Init	Descriptions	In/Output type
1	CAMVSI	In	*	-	Vertical timing input	C*1
2	N.C. *2	-	-	-	-	-
3	CAMHSI	In	*	-	Horizontal timing input	C*1
4	SDA	In/Out	DATA	In	In/Output serial data	F
5	SDC	In	CLK	-	In/Output serial clock	D*1
6	I2CDEV0	In	*	-	I2C device address setting	D*1
7	CAMDI0	In	DATA	-	Data input: bit 0	G*1
8	CAMDI1	In	DATA	-	Data input: bit 1	G*1
9	CAMDI2	In	DATA	-	Data input: bit 2	G*1
10	CAMDI3	In	DATA	-	Data input: bit 3	G*1
11	CAMDI4	In	DATA	-	Data input: bit 4	G*1
12	CAMDI5	In	DATA	-	Data input: bit 5	G*1
13	CAMDI6	In	DATA	-	Data input: bit 6	G*1
14	CAMDI7	In	DATA	-	Data input: bit 7	G*1
15	RESERVEI0 *3	In	*	-	RESERVE	C*1
16	RESERVEI1 *3	In	*	-	RESERVE	C*1
17	RESERVEI2 *3	In	*	-	RESERVE	C*1
18	RESERVEI3 *3	In	*	-	RESERVE	C*1
19	RESERVEI4 *3	In	*	-	RESERVE	C*1
20	RESERVEI5 *3	In	*	-	RESERVE	C*1
21	RESERVEI6 *3	In	*	-	RESERVE	C*1
22	RESERVEI7 *3	In	*	-	RESERVE	C*1
23	RESERVEI8 *3	In	*	-	RESERVE	C*1
24	RESERVEI9 *3	In	*	-	RESERVE	C*1
25	RESERVEI10 *3	In	*	-	RESERVE	C*1
26	RESERVEI11 *3	In	*	-	RESERVE	C*1
27	VDDIO	-	PWR	-	DIGITAL IO power source	-
28	CAMCKI	In	CLK	-	Clock input	D*1
29	GND	-	GND	-	Common GROUND	-
30	VDD	-	PWR	-	CORE power source	-
31	MSEL0 *3	In	*	-	Mode select 0	A
32	MSEL1 *3	In	*	-	Mode select 1	A

Change by setup by the register is possible for the "" display in the column of an Active level. Moreover, Init is a pin state under reset.
*1 : It suspends during reset (initial state)
*2 : Please connect with GND
*3 : Please connect with GND.

PIN No.	Pin Name	In/Out	Active Level	Init	Descriptions	In/Output type
33	MSEL2 *4	In	*	-	Mode select 2	A
34	PWMO	Out	*	Low	PWM output for LCD backlight	E
35	RESERVEO11 *5	Out	*	Low	RESERVE	E
36	RESERVEO10 *5	Out	*	Low	RESERVE	E
37	RESERVEO9 *5	Out	*	Low	RESERVE	E
38	RESERVEO8 *5	Out	*	Low	RESERVE	E
39	RESERVEO7 *5	Out	*	Low	RESERVE	E
40	RESERVEO6 *5	Out	*	Low	RESERVE	E
41	RESERVEO5 *5	Out	*	Low	RESERVE	E
42	RESERVEO4 *5	Out	*	Low	RESERVE	E
43	RESERVEO3 *5	Out	*	Low	RESERVE	E
44	RESERVEO2 *5	Out	*	Low	RESERVE	E
45	RESERVEO1 *5	Out	*	Low	RESERVE	E
46	RESERVEO0 *5	Out	*	Low	RESERVE	E
47	GND	-	GND	-	Common GROUND	-
48	CAMDO7	Out	DATA	Low	Data output: bit 7	E
49	CAMDO6	Out	DATA	Low	Data output: bit 6	E
50	CAMDO5	Out	DATA	Low	Data output: bit 5	E
51	CAMDO4	Out	DATA	Low	Data output: bit 4	E
52	CAMDO3	Out	DATA	Low	Data output: bit 3	E
53	CAMDO2	Out	DATA	Low	Data output: bit 2	E
54	CAMDO1	Out	DATA	Low	Data output: bit 1	E
55	CAMDO0	Out	DATA	Low	Data output: bit 0	E
56	I2CDEV6B *3	In	*	-	RESERVE	A
57	RESERVEO12 *5	Out	*	High	RESERVE	E
58	CAMHSO	Out	*	Low	Horizontal timing output signal	E
59	CAMVSO	Out	*	Low	Vertical timing output signal	E
60	RESETB	In	Low	-	System reset signal	B
61	VDDIO	-	PWR	-	DIGITAL IO power source	-
62	CAMCKO	Out	CLK	Low	Clock output	E
63	GND	-	GND	-	Common GROUND	-
64	VDD	-	PWR	-	CORE power source	-

Change by setup by the register is possible for the "" display in the column of an Active level. Moreover, Init is a pin state under reset.
*3 : Please connect with GND
*4 : Please connect with VDDIO
*5 : Leave OPEN

●I/O pins equivalent circuit diagrams

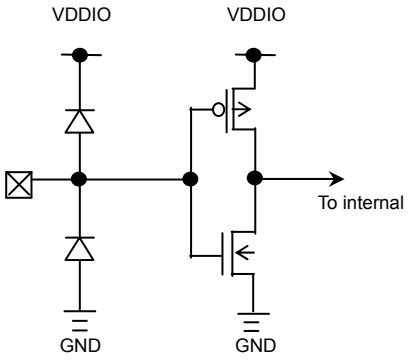
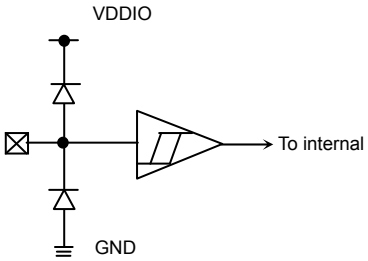
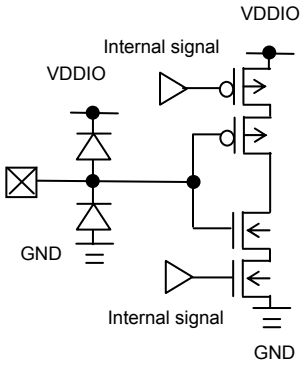
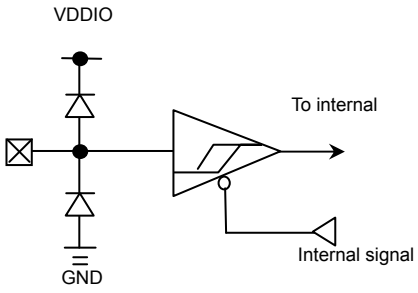
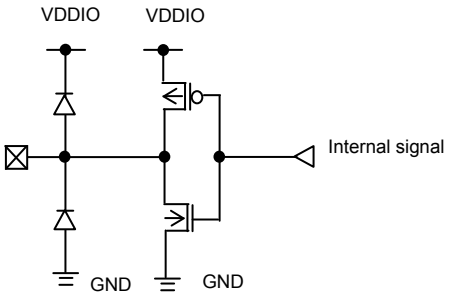
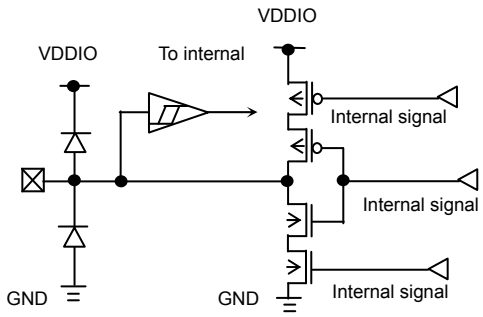
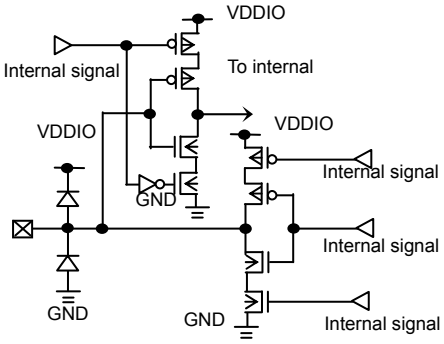
Type	Equivalent circuit structure	Type	Equivalent circuit structure
A	 Input pin	**B**	 Input pin with the hysteresis function
C	 Input pin with the suspend function	**D**	 Input pin with the hysteresis and suspend functions
E	 Output-pin	**F**	 In/output pin with the hysteresis function
G	 In/output pin with the suspend function		

Fig.2 I/O pins equivalent circuit diagrams

●Block diagram

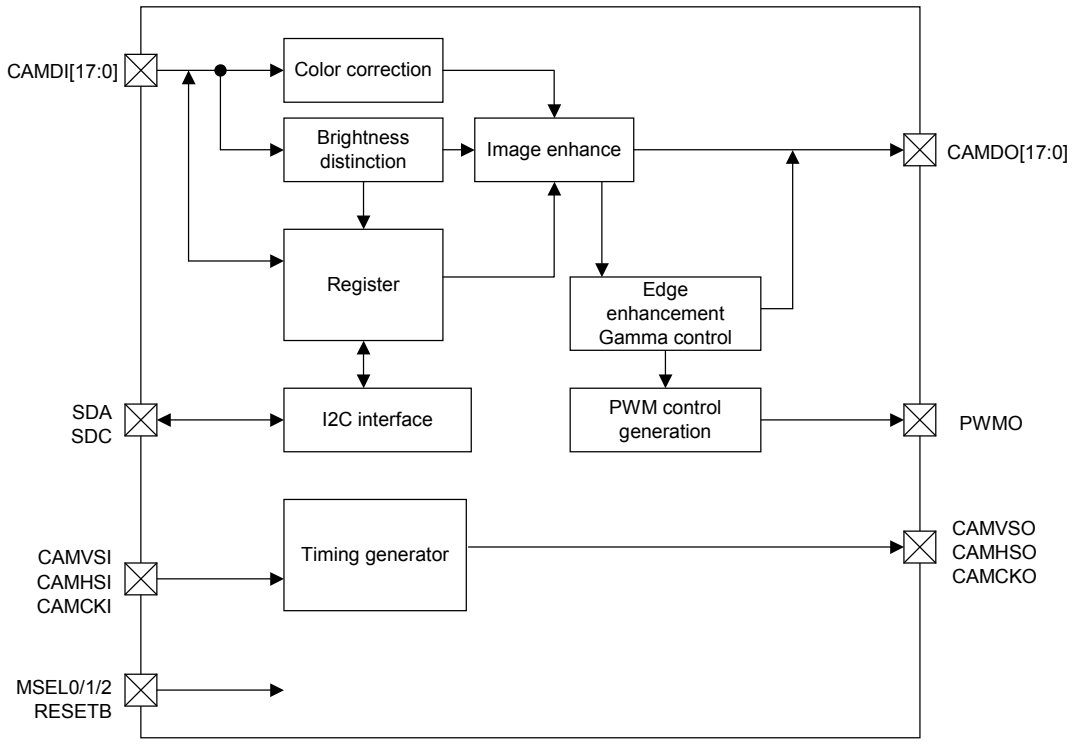


Fig.3 Block diagram

●Functional descriptions

1. Brightness distinction
   Luminance of the input image is analyzed, and collection coefficient value is calculated. Calculated collection coefficient value is kept until the next frame is input, and it is reflected on the image enhancement part and the color collection part when the next frame is processed.

2. Image enhance
   The correction operation is done to the luminance element of the input image based on the correction coefficient value from the luminance distinction part.
   It puts the chroma element from the color correction together, and outputs along output format.
   It is possible to change correction strength of the output image.

3. Color correction
   The correction operation is done to the chroma element of the input image based on the correction coefficient value from the luminance distinction part. Color correction strength can be changed.

4. Edge enhancement
   The edge emphasis filter is built into. The image is corrected to sharp image quality by emphasizing the outline.
   Strength of the edge emphasis filter can be adjusted.

5. Gamma control
   Gamma control can be given to the luminance element.
   A line form is interpolated with a setup point of the gamma curve between the setup point nine points, and output value is calculated from that curve.

6. PWM control generation
   The PWM signal for the LCD backlight control can be output. There is a setup of a manual by the register in the DUTY control of the PWM signal, and an auto-setup to be controlled automatically by BU1574GUW. As for the auto-setup, DUTY is calculated from the luminance information of the input image every frame.

7. Register
   The image correction parameter, the image size, and the format are set from the register.
   The data of the register can be written by the I^2C interface, and be read.

8. Data input format

8.1 ITU-R BT.656 input format

8.1.1 Horizontal direction synchronization timing

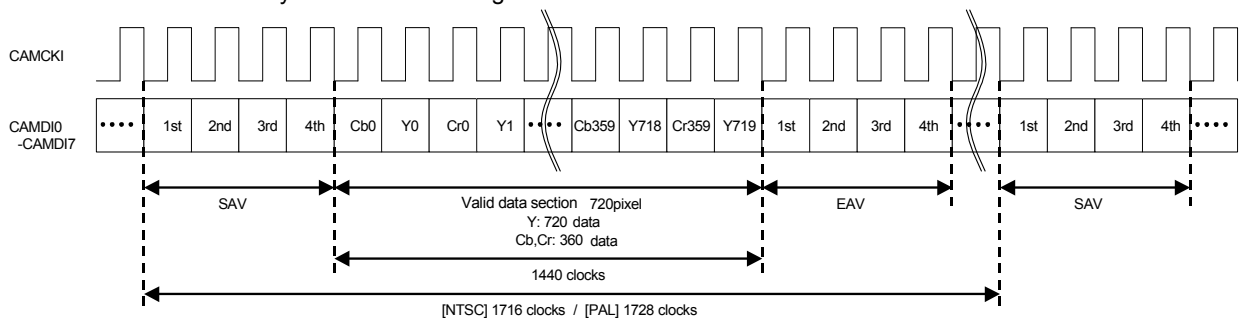


Fig.4 ITU-R BT.656 input format (horizontal direction)

8.1.2 Vertical direction synchronization timing

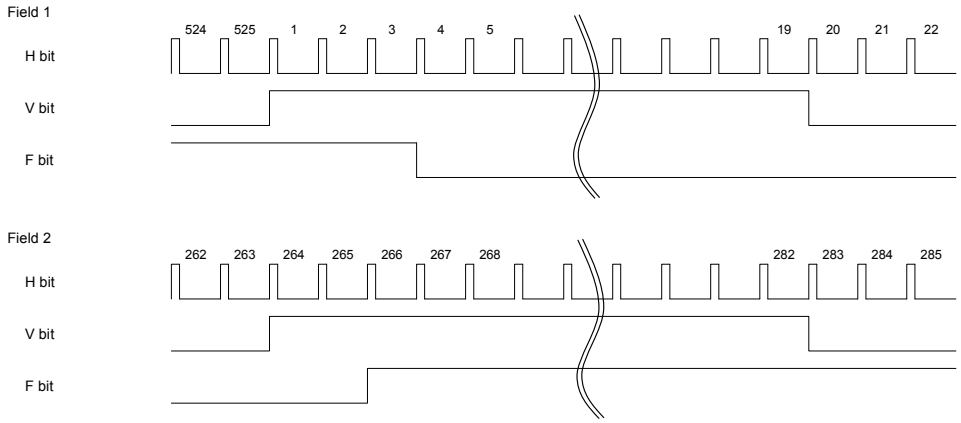


Fig.5 ITU-R BT.656 input format for NTSC (vertical direction)

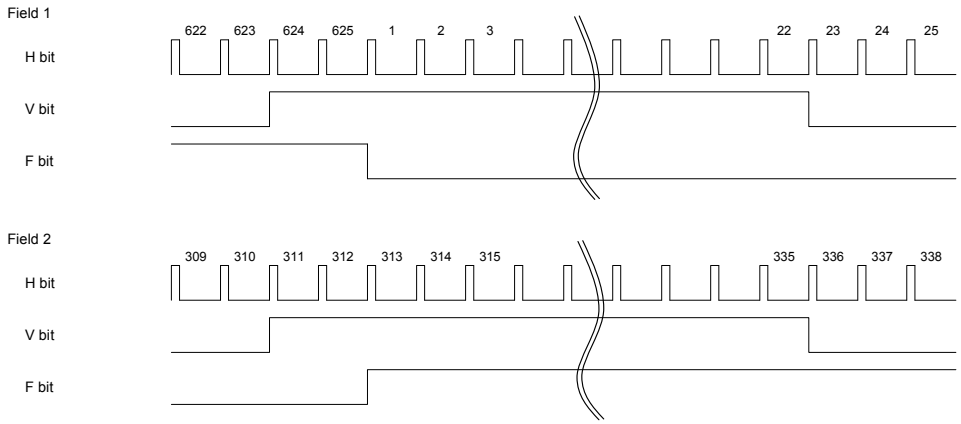


Fig.6 ITU-R BT.656 input format for PAL (vertical direction, bottom view)

8.2. YCbCr with synchronizing signals 8-bit input format
8.2.1. Horizontal direction synchronization timing

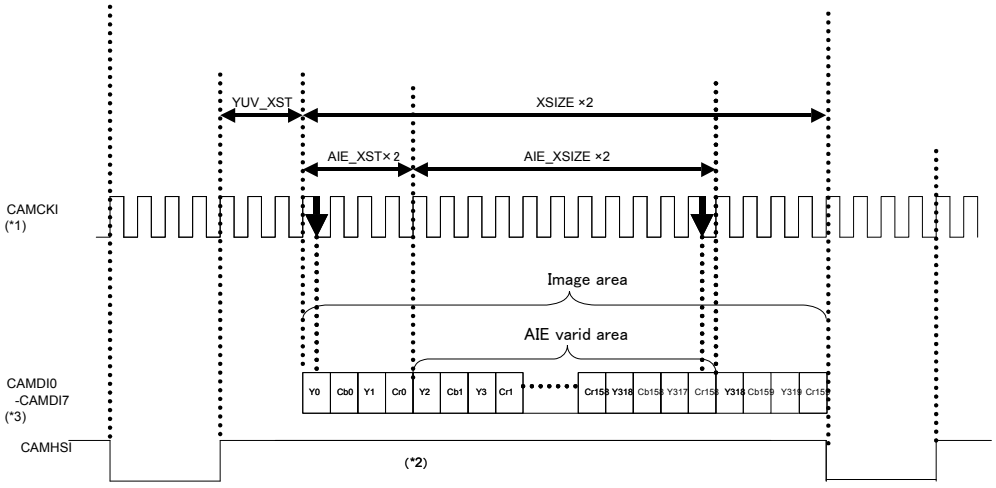


Fig.7 Horizontal direction synchronization timing

(Note)
* YUV_XST, XSIZE x 2, AIE_XST x 2 and AIE_XSIZE×2, which are described in the figures and the notes, are set by the registers.
(*1) By changing the setting of the POL register (INDEX Address: E1h), the polarities of CAMCKI, CAMVSI and CAMHSI can be set independently. The figure above shows the timing in the case that the data are fetched at the CAMCKI falling edge (CKPOL = 1 setting) and the polarity of HSYNC is low active (HSPOL = 0 setting).
(*2) Set CAMHSI so as not to become 'L' in other sections than the sync section (CAMHSI = 'L' section in the figure shown above).
(*3) Do not change the frequency of CAMCKI during the operation.
(*4) Take note of the items described above to input each signal.

8.2.2. Vertical direction synchronization timing

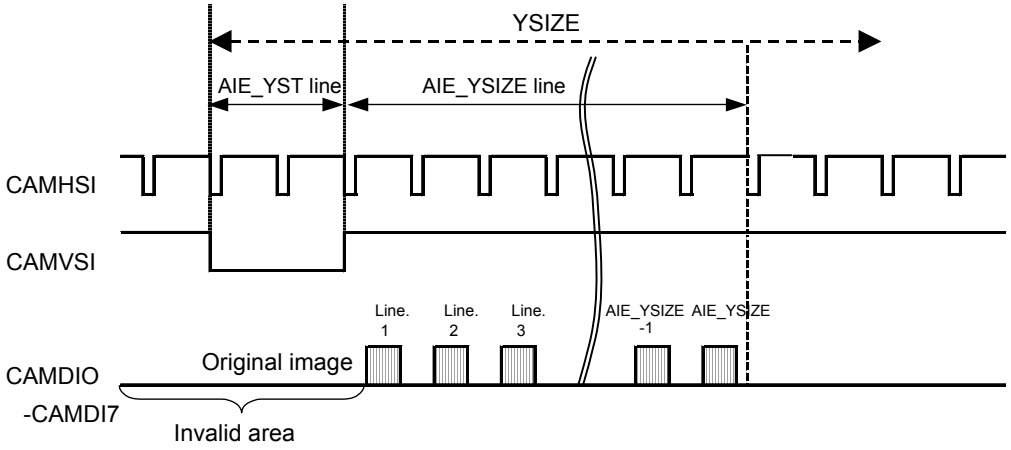


Fig.8 Vertical direction synchronization timing

(Note)
* Y_SIZE, AIE_YST and AIE_YSIZE, which are described in the figures and the notes, are set by the registers.
(*1) The figure above shows the timing in the case that the polarity of VSYNC is low active (VSPOL = 0 setting) and also the polarity of HSYNC is low active (HSPOL = 0 setting).
(*2) Take note of the items described above to input each signal.

9. I^2C Interface format

The slave address is 42h when I2CDEV0 = 0 and 43h when I2CDEV0 = 1.
When both of the write and read accesses are respectively executed successively 2 times or more, the sub-address is automatically incremented.

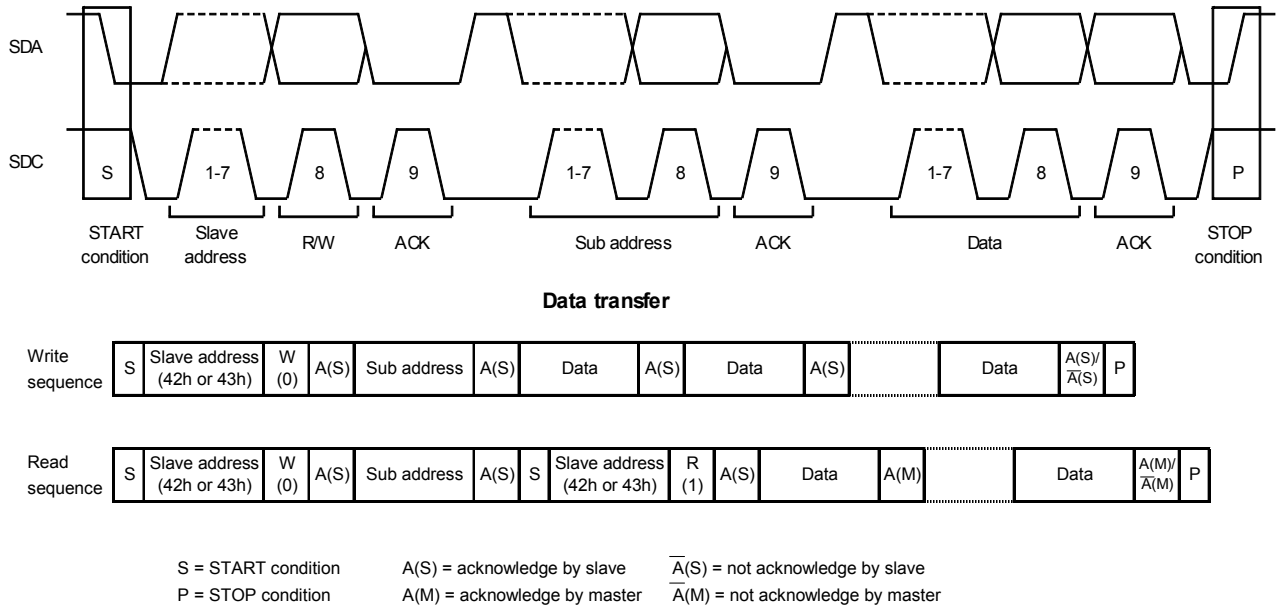


Fig.9 I^2C Interface format

●Timing chart

1. Data input interface timing

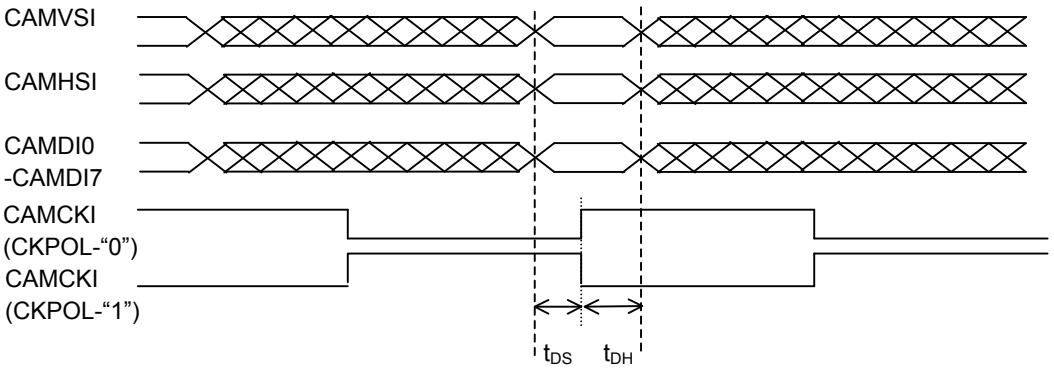


Fig.10 Data input interface timing

Symbol	Descriptions	MIN	TYP	MAX	Unit
t_{DS}	Setup time to CAMCKI rising / falling edge	8	-	-	ns
t_{DH}	Hold time to CAMCKI rising / falling edge	8	-	-	ns

2. Data output interface timing

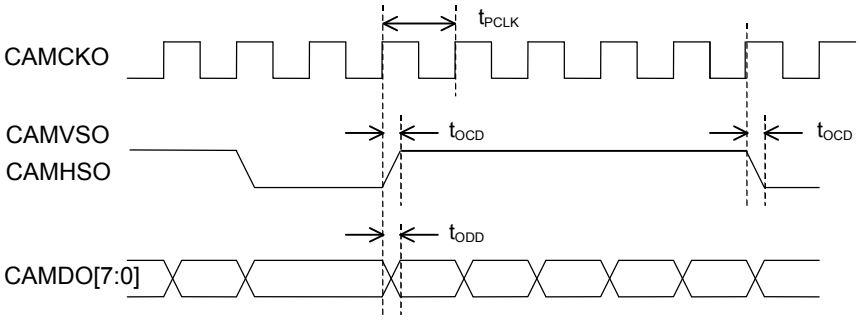


Fig.11 Data output interface timing

Symbol	Descriptions	MIN	TYP	MAX	Unit
tPCLK	Clock cycle	27.7	-	-	ns
dPCLK	Clock duty	40	50	60	%
tODD	CAMDO is defined from CAMCKO	-	-	5	ns
tOCD	CAMVSO and CAMHSO are defined from CAMCKO	-	-	5	ns

3. I^2C interface timing

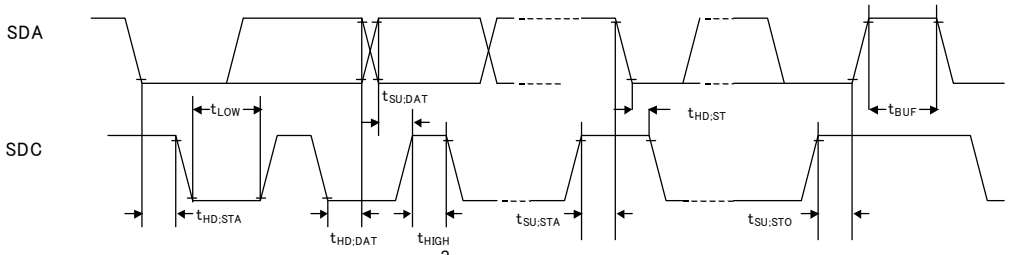


Fig.12 I^2C interface timing

Symbol	Descriptions	MIN	TYP	MAX	Unit
fSCL	SDC clock frequency	0	-	400	kHz
tHD;STA	Hold time (repeat) "START" condition The first clock pulse is generated after this period	0.6	-	-	µs
fLOW	SDC clock "L" period	1.3	-	-	µs
tHIGH	SDC clock "H" period	0.6	-	-	µs
tSU;STA	Repeat "START" condition setup time	0.6	-	-	µs
tHD;DAT	Data hold time	0			µs
tSU;DAT	Data setup time	100	-	-	ns
tSU;STO	"STOP" condition setup time	0.6	-	-	µs
tBUF	Bus free period between the "STOP" condition and "START" condition	1.3	-	-	µs

●Application example

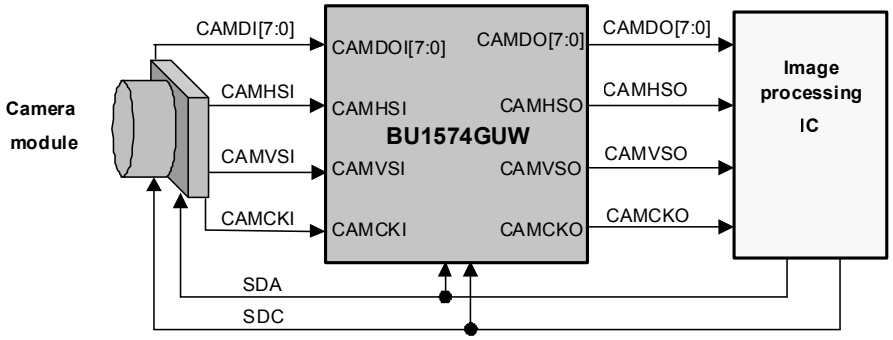


Fig.13 Application example

●Notes for use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.
Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

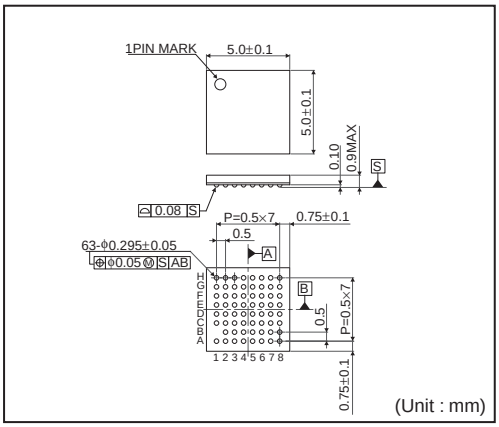
●Ordering part number

B	U	1	5	7	4	G	U	W	-	E	2

ROHM model name	Product number	Package type GUW: VBGA063W050	Taping model name E2: Embossed reel tape

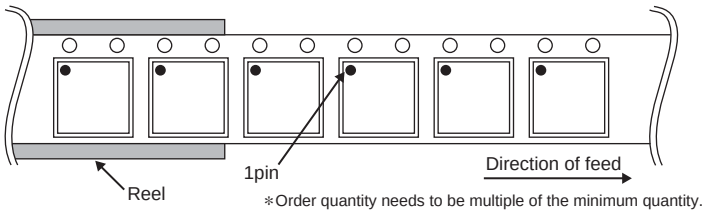
●Package specification

VBGA063W050



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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