



## TABLE OF CONTENTS

Features .....	1	2-Bit Logic Interface Mode (I2C/EN = 0).....	13
Applications.....	1	I <sup>2</sup> C Interface Mode (I2C/EN = 1).....	13
Functional Block Diagram .....	1	State Transitions .....	15
General Description .....	1	I <sup>2</sup> C Register Map .....	16
Revision History .....	2	Safety Features.....	19
Specifications.....	3	Overvoltage Fault .....	19
Recommended Specifications: Input and Output Capacitance and Inductance .....	4	Output Capacitor Fault.....	19
I <sup>2</sup> C-Compatible Interface Timing Specifications .....	5	Timeout Fault.....	19
Absolute Maximum Ratings.....	6	Overtemperature Fault .....	19
Thermal Data .....	6	Short-Circuit Fault .....	19
Thermal Resistance .....	6	Current Limit .....	19
ESD Caution.....	6	Amount of LED Detection.....	19
Pin Configuration and Function Descriptions.....	7	Input Undervoltage .....	19
Typical Performance Characteristics .....	8	Applications Information .....	20
Theory of Operation .....	12	External Component Selection .....	20
White LED Driver .....	12	PCB Layout.....	22
Assist Light and Torch Modes .....	12	Outline Dimensions .....	23
		Ordering Guide .....	23

## REVISION HISTORY

5/09—Revision 0: Initial Version

## SPECIFICATIONS

$V_{IN} = 3.6\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for minimum/maximum specifications and  $T_A = 25^\circ\text{C}$  for typical specifications, unless otherwise noted.

Table 1.

Parameter <sup>1</sup>	Conditions	Min	Typ	Max	Unit
<b>SUPPLY</b>					
Input Voltage Range		2.7		5.5	V
Undervoltage Lockout Threshold	$V_{IN}$ falling	2.3	2.4	2.5	V
Hysteresis		50	100	150	mV
Shutdown Current	$T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , current into VIN pin, $V_{IN} = 2.7\text{ V}$ to $4.5\text{ V}$		0.3	1	$\mu\text{A}$
Standby Current	$T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , current into VIN pin, $V_{IN} = 2.7\text{ V}$ to $4.5\text{ V}$		3	10	$\mu\text{A}$
I2C/EN = SCL/EN1 = SDA/EN2 = 1.8V					
Operating Quiescent Current	Torch mode, two LEDs, LED current = 40 mA		5.3		mA
SW Switch Leakage	$T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$			1	$\mu\text{A}$
<b>INPUTS</b>					
Input Logic Low Voltage				0.54	V
Input Logic High Voltage		1.26			V
TORCH, STROBE, TX_MASK Pull-Down			350		k $\Omega$
SCL/EN1, SDA/EN2 Pull-Down	I2C/EN = 0 V		350		k $\Omega$
TORCH Glitch Filtering Delay	From TORCH rising edge to device start	6.3	9	11.7	ms
<b>LED DRIVER</b>					
LED Current					
Assist Light, Torch	I2C/EN = 0, one LED		80		mA
	I2C/EN = 0, two LEDs		40		mA
	I2C/EN = 1, assist light value setting = 0 (000 binary)		20		mA
	I2C/EN = 1, assist light value setting = 7 (111 binary)		160		mA
Flash	I2C/EN = 0, one LED		500		mA
	I2C/EN = 0, two LEDs		320		mA
	I2C/EN = 1, flash value setting = 0 (0000 binary)		200		mA
	I2C/EN = 1, one LED, flash value setting = 15 (1111 binary)		500		mA
	I2C/EN = 1, two LEDs, flash value setting = 10 to 15 (1010 to 1111 binary)		400		mA
LED Current Accuracy	$I_{LED} = 320\text{ mA}$ to $500\text{ mA}$	-5		+5	%
	$I_{LED} = 60\text{ mA}$ to $320\text{ mA}$	-5		+10	%
	$I_{LED} = 20\text{ mA}$ to $60\text{ mA}$	-5		+20	%
LED Current Source Headroom <sup>2</sup>	Flash typical, 400 mA LED current		290		mV
	Torch 160 mA		190		
LED_OUT Ramp-Up Time				1	ms
LED_OUT Ramp-Down Time				0.5	ms
Maximum Timeout For Flash			850		ms
Timer Accuracy		-7.5		+7.5	%
<b>SWITCHING REGULATOR</b>					
Switching Frequency		1.85	2	2.15	MHz
Minimum Duty Cycle			9.0		%
N-FET Resistance			135		m $\Omega$
P-FET Resistance			290		m $\Omega$

# ADP1655

Parameter <sup>1</sup>	Conditions	Min	Typ	Max	Unit
SAFETY FEATURES					
Thermal Shutdown Threshold					
T <sub>J</sub> Rising			150		°C
T <sub>J</sub> Falling			140		°C
Overvoltage Threshold		9.0	9.5	10.1	V
Coil Peak Current Limit	Peak current value setting = 0 (00 binary)	1.13	1.25	1.38	A
	Peak current value setting = 1 (01 binary)	1.35	1.5	1.65	A
	Peak current value setting = 2 (10 binary)	1.58	1.75	1.93	A
	Peak current value setting = 3 (11 binary)	1.8	2.0	2.2	A
LED_OUT Short-Circuit Detection Comparator Reference Voltage			1.2	1.3	V
LED Counting Comparator Threshold Voltage	LED value setting = 0 (00 binary)		4.3		V
	LED value setting = 1 (01 binary)		4.6		V
	LED value setting = 2 (10 binary)		4.0		V
	LED value setting = 3 (11 binary)		4.9		V

<sup>1</sup> All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

<sup>2</sup> Two LEDs are used for this parameter.

## RECOMMENDED SPECIFICATIONS: INPUT AND OUTPUT CAPACITANCE AND INDUCTANCE

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CAPACITANCE						
Input	C <sub>MIN</sub>	T <sub>A</sub> = -40°C to +125°C	4.0			μF
Output		T <sub>A</sub> = -40°C to +125°C	4.0		20	μF
MINIMUM AND MAXIMUM INDUCTANCE						
	L	T <sub>A</sub> = -40°C to +125°C	1.5		2.8	μH

I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

Table 3.

Parameter <sup>1</sup>	Min	Max	Unit	Description
f <sub>SCL</sub>		400	kHz	SCL clock frequency
t <sub>HIGH</sub>	0.6		μs	SCL high time
t <sub>LOW</sub>	1.3		μs	SCL low time
t <sub>SU, DAT</sub>	100		ns	Data setup time
t <sub>HD, DAT</sub>	0	0.9	μs	Data hold time
t <sub>SU, STA</sub>	0.6		μs	Setup time for repeated start
t <sub>HD, STA</sub>	0.6		μs	Hold time for start/repeated start
t <sub>BUF</sub>	1.3		μs	Bus free time between a stop and a start condition
t <sub>SU, STO</sub>	0.6		μs	Setup time for stop condition
t <sub>R</sub>	20 + 0.1 C <sub>B</sub> <sup>2</sup>	300	ns	Rise time of SCL and SDA
t <sub>F</sub>	20 + 0.1 C <sub>B</sub>	300	ns	Fall time of SCL and SDA
t <sub>SP</sub>	0	50	ns	Pulse width of suppressed spike
C <sub>B</sub>		400	pF	Capacitive load for each bus line

<sup>1</sup> Guaranteed by design.

<sup>2</sup> C<sub>B</sub> is the total capacitance of one bus line in picofarads.

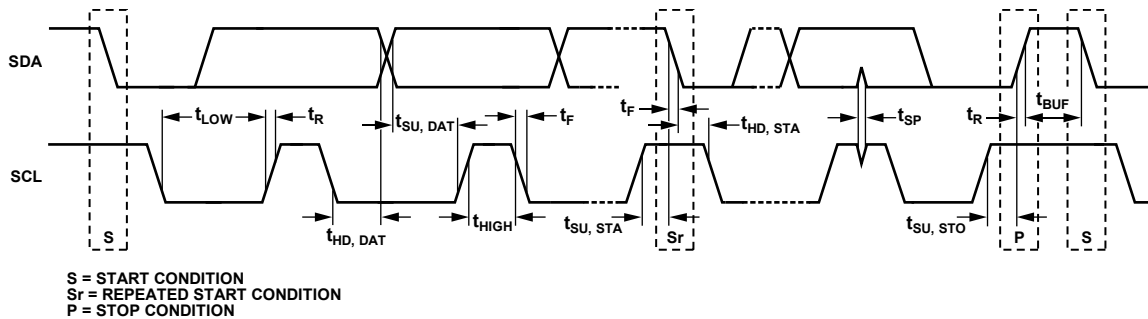


Figure 3. I<sup>2</sup>C-Compatible Interface Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN, SDA/EN2, SCL/EN1, I2C/EN, STROBE, TORCH, TX_MASK to SGND	−0.3 V to +6 V
LED_OUT, SW, VOUT to SGND	−0.3 V to +12 V
PGND to SGND	−0.3 V to +0.3 V
VOUT to LED_OUT	−0.3 V to +6 V
Ambient Temperature Range (T <sub>A</sub> )	−40°C to +85°C
Junction Temperature Range (T <sub>J</sub> )	−40°C to +125°C
Storage Temperature	JEDEC J-STD-020
ESD Human Body Model	±2000 V
ESD Charged Device Model	±1000 V
ESD Machine Model	±200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL DATA

The ADP1655 may be damaged if the junction temperature limits are exceeded. Monitoring T<sub>A</sub> does not guarantee that T<sub>J</sub> is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum T<sub>A</sub> may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum T<sub>A</sub> can exceed the maximum limit as long as the T<sub>J</sub> is within specification limits. T<sub>J</sub> of the device is dependent on the T<sub>A</sub>, the power dissipation (PD) of the device, and the junction-to-ambient thermal resistance (θ<sub>JA</sub>) of the package. Maximum T<sub>J</sub> is calculated from the T<sub>A</sub> and PD using the following formula:

$$T_J = T_A + (PD \times \theta_{JA})$$

### THERMAL RESISTANCE

θ<sub>JA</sub> of the package is based on modeling and calculation using a 4-layer board. θ<sub>JA</sub> is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ<sub>JA</sub> may vary, depending on PCB material, layout, and environmental conditions. The specified value of θ<sub>JA</sub> is based on a 4-layer, 4 in × 3 in, 2 1/2 oz copper board, per JEDEC standards. For more information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

θ<sub>JA</sub> is specified for a device mounted on a JEDEC 2S2P PCB.

Table 3. Thermal Resistance

Package Type	θ <sub>JA</sub>	Unit
12-Ball WLCSP	75	°C/W

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

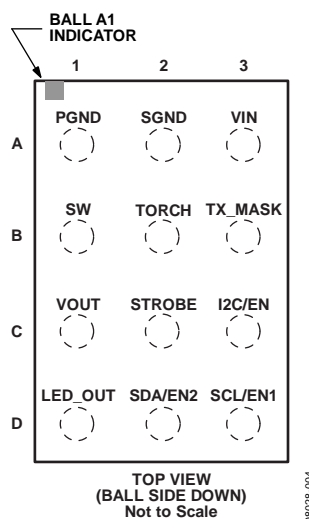


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	PGND	Ground	Ground for Internal Switching FET.
A2	SGND	Ground	Connect this pin at a single point to the power ground.
A3	VIN	Supply	Connect the battery between VIN and PGND. Bypass VIN with a 10 $\mu$ F, 6.3 V or greater X5R/X7R capacitor.
B1	SW	Output	Connect a 2.2 $\mu$ H inductor between SW and the battery.
B2	TORCH	Digital Input	This pin enables the torch, provided that the device is not in flash or assist light mode.
B3	TX_MASK	Digital Input	Connect a digital signal to the TX_MASK pin. When the logic level is driven high during a flash event the current is reduced to the torch level.
C1	VOUT	Output	VOUT senses the output voltage of the boost converter and provides the input voltage to the LED current source. The VOUT pin features a comparator to detect an overvoltage condition if the LED string is open circuited. Connect a 10.0 $\mu$ F capacitor between VOUT and PGND.
C2	STROBE	Digital Input/ Output	The STROBE input is used to synchronize the timing of the camera module to the LED driver in I <sup>2</sup> C-compatible interface mode. In 2-bit logic interface mode, this acts as an output, indicating the number of LEDs attached. STROBE = high indicates two LEDs, whereas STROBE = low indicates one LED.
C3	I2C/EN	Digital Input	A logic low selects the 2-bit logic interface, whereas logic high selects I <sup>2</sup> C-compatible interface. If I2C/EN is low and SDA/EN2 and SCL/EN1 are low, the driver enters shutdown mode with consumption < 1 $\mu$ A.
D1	LED_OUT	Output	White LED Anode Connection. Connect LED_OUT to the anode of the white LED. LED_OUT is internally connected to a programmable PMOS current source, which regulates the LED current.
D2	SDA/EN2	Digital Input/ Output	Data Input/Output (SDA). In 2-bit logic interface mode, SDA/EN2 is the second input bit of the digital interface. Second Input Bit (EN2). In I <sup>2</sup> C mode, SDA is the data input/output of the I <sup>2</sup> C-compatible interface.
D3	SCL/EN1	Digital Input	Clock Input (SCL). In 2-bit logic interface mode, SCL/EN1 is the first input bit of the digital interface. First Input Bit (EN1). In I <sup>2</sup> C mode, SCL is the clock input of the I <sup>2</sup> C-compatible interface.

## TYPICAL PERFORMANCE CHARACTERISTICS

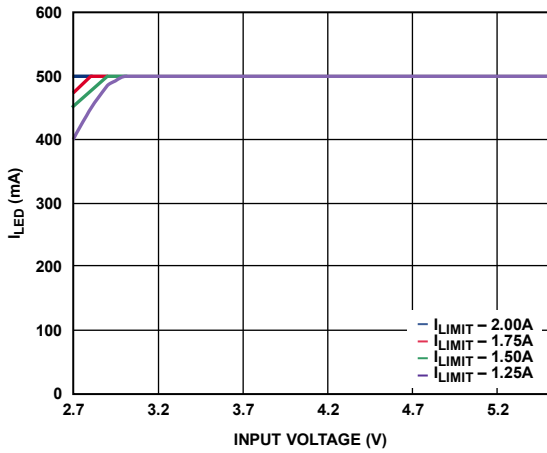


Figure 5. Maximum Current vs. Input Voltage, One LED

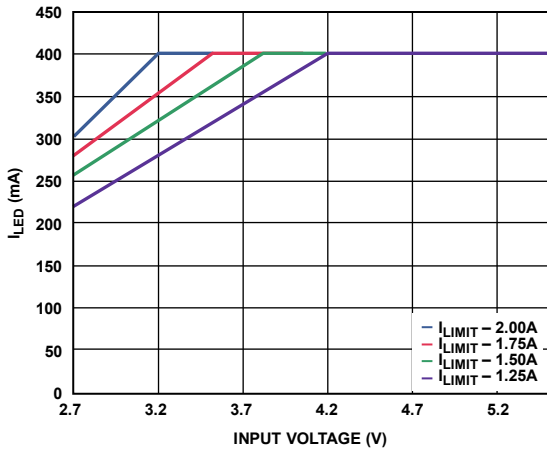


Figure 6. Maximum Current vs. Input Voltage, Two LEDs; LED Forward Voltage ( $V_f$ ) = 4.3 V for each LED

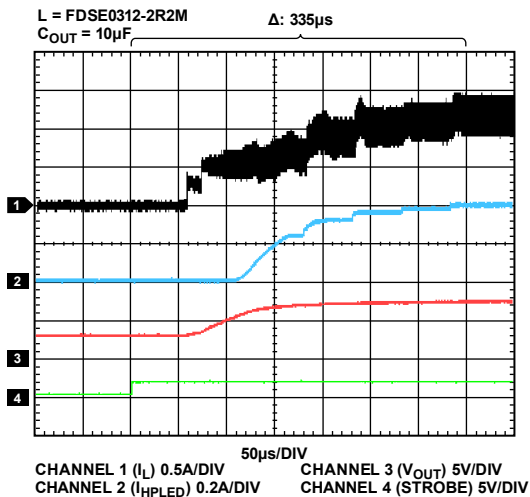


Figure 7. Startup, Two LEDs Flash Mode,  $I_{LED} = 400$  mA,  $V_{IN} = 3.2$  V

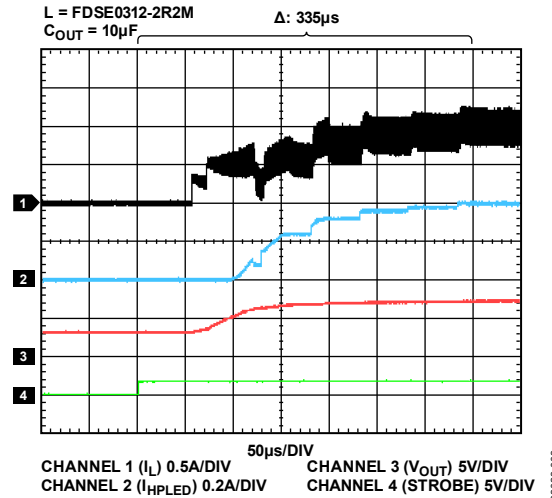


Figure 8. Startup, Two LEDs Flash Mode,  $I_{LED} = 400$  mA,  $V_{IN} = 3.6$  V

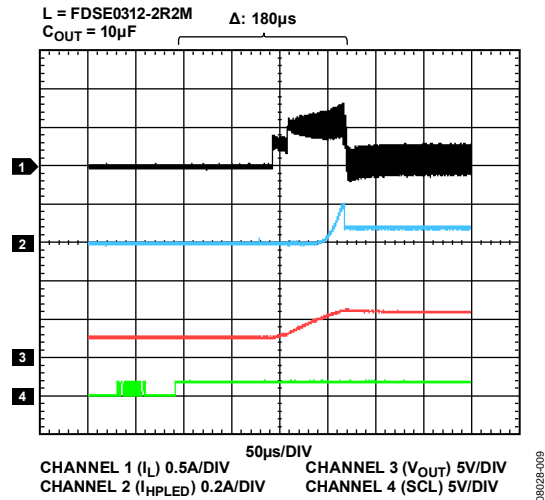


Figure 9. Startup, Two LEDs Assist Light Mode,  $I_{LED} = 40$  mA,  $V_{IN} = 3.2$  V

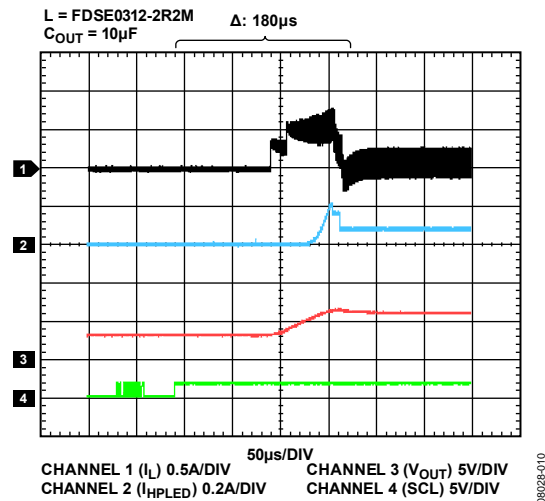


Figure 10. Startup, Two LEDs Torch Mode,  $I_{LED} = 40$  mA,  $V_{IN} = 3.6$  V



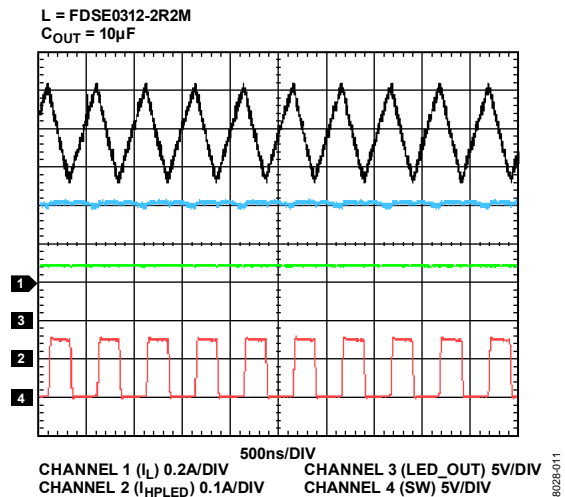


Figure 11. Inductor Current, Two LEDs Flash Mode, I<sub>LED</sub> = 400 mA, V<sub>IN</sub> = 3.6 V

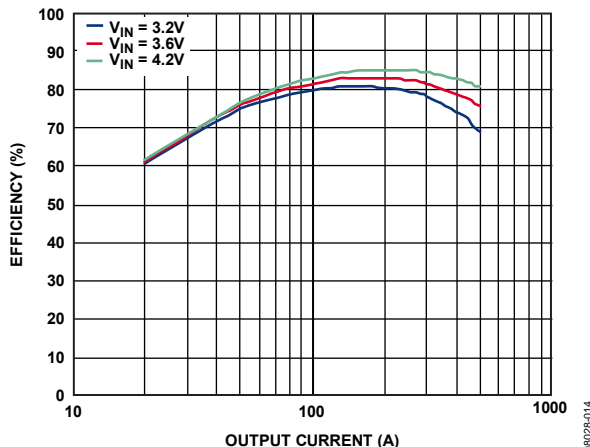


Figure 14. Efficiency P<sub>LED</sub>/P<sub>IN</sub>, Two High Power White LEDs in Series

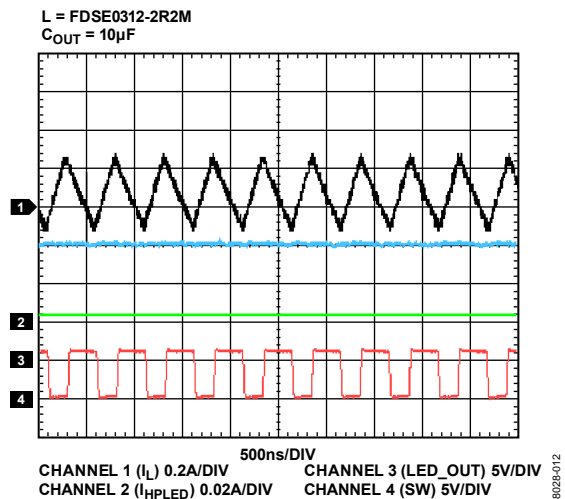


Figure 12. Inductor Current, Two LEDs Torch Mode, I<sub>LED</sub> = 40 mA, V<sub>IN</sub> = 3.6 V

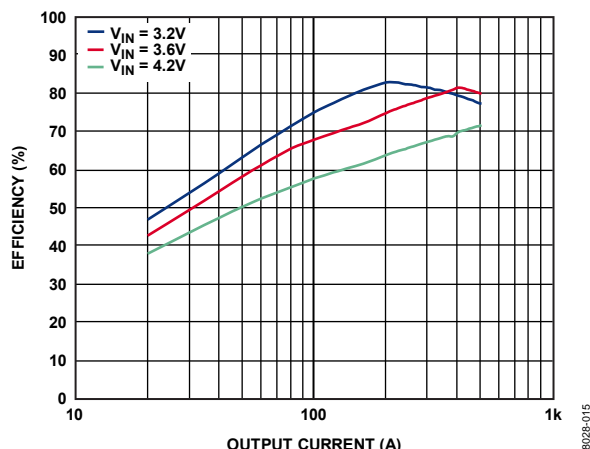


Figure 15. Efficiency P<sub>LED</sub>/P<sub>IN</sub>, One High Power White LED

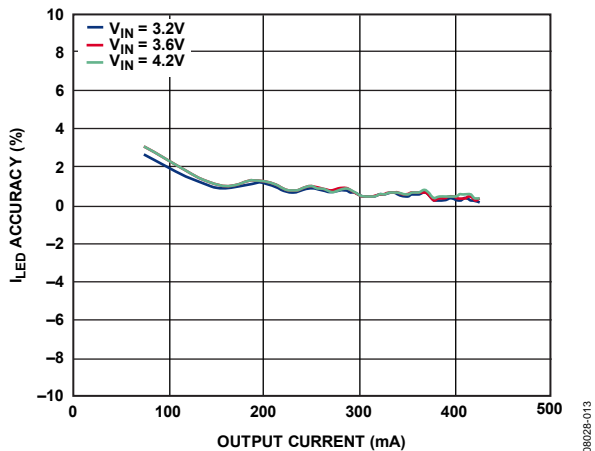


Figure 13. LED Current Accuracy vs. Output Current

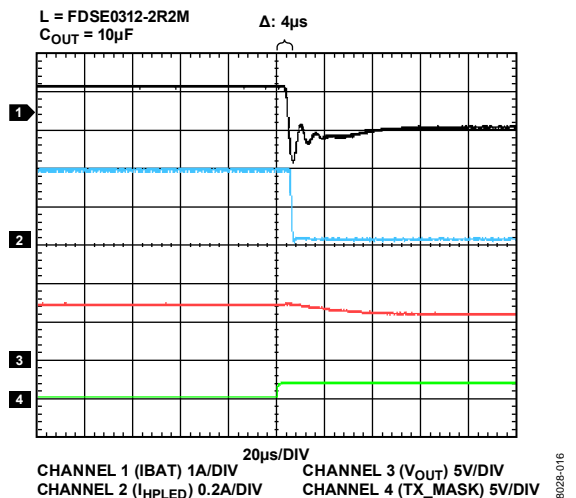


Figure 16. Tx Masking Response, TX\_MASK = 0 V to 1.8 V, I<sub>LED</sub> = 40 mA to 400 mA, V<sub>IN</sub> = 3.2 V

# ADP1655

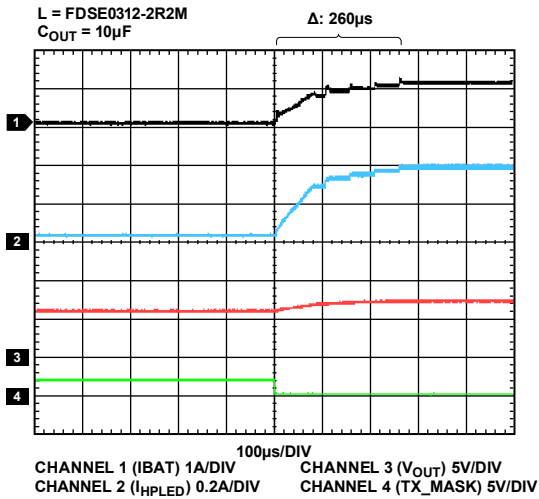


Figure 17. Tx Masking Response, TX\_MASK = 1.8 V to 0 V, I<sub>LED</sub> = 40 mA to 400 mA, V<sub>IN</sub> = 3.2 V

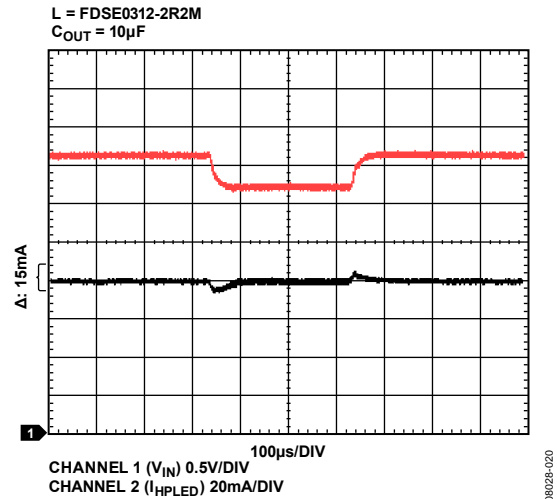


Figure 20. Line Transient, V<sub>IN</sub> = 3.2 V to 3.6 V, I<sub>LED</sub> = 400 mA

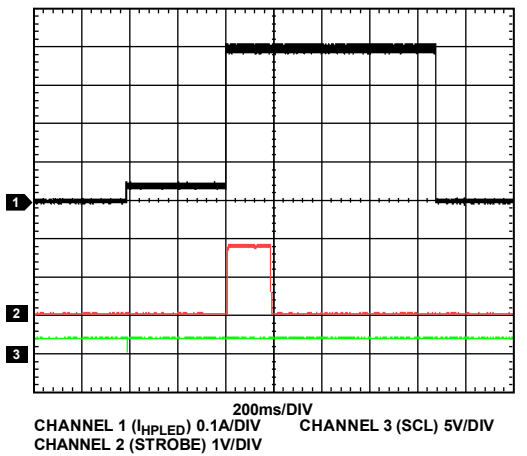


Figure 18. Assist Light and Flash, STROBE Edge Sensitive Mode, Two LEDs, Timer = 850 ms, I<sub>LED</sub> = 40 mA to 400 mA, V<sub>IN</sub> = 3.6 V

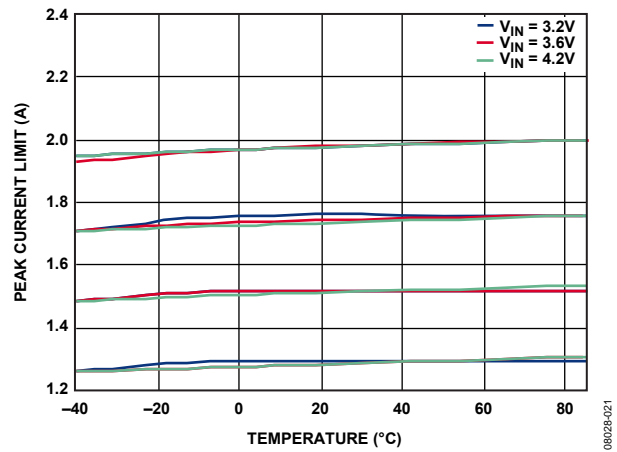


Figure 21. Coil Peak Current Limit vs. Temperature, Output Mode Register = 00, 01, 10, and 11 (Binary)

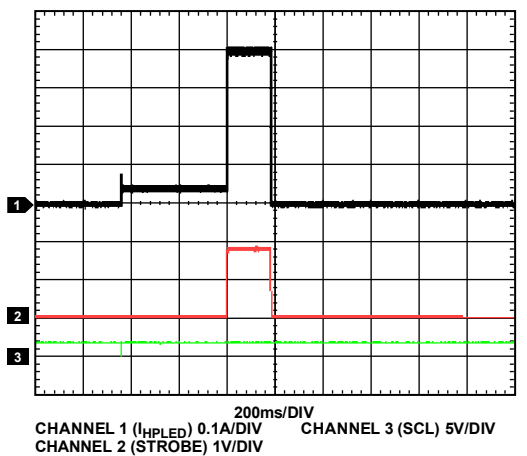


Figure 19. Assist Light and Flash, STROBE Level Sensitive Mode, Two LEDs, I<sub>LED</sub> = 40 mA to 400 mA, V<sub>IN</sub> = 3.6 V

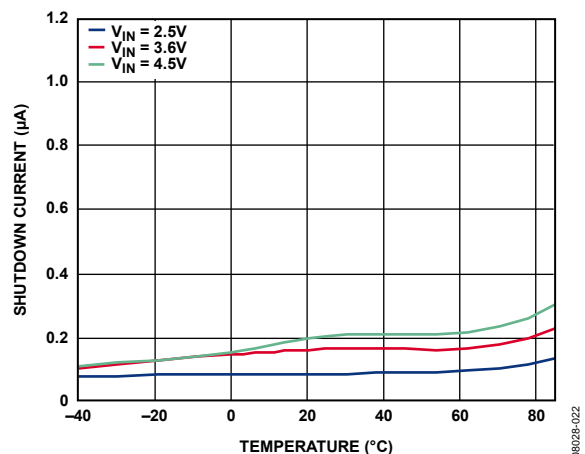


Figure 22. Shutdown Current vs. Temperature vs. V<sub>IN</sub>

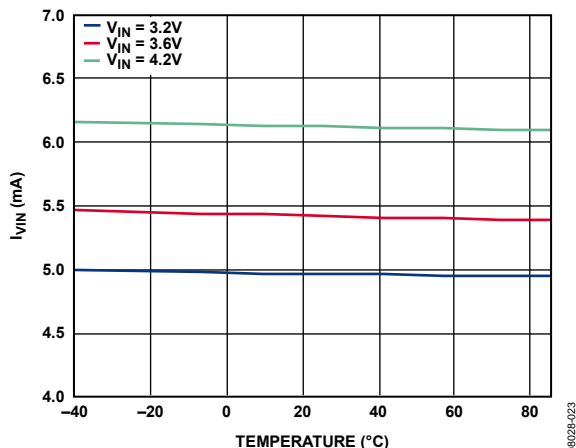


Figure 23. Operating Quiescent Current vs. Temperature, Torch Mode

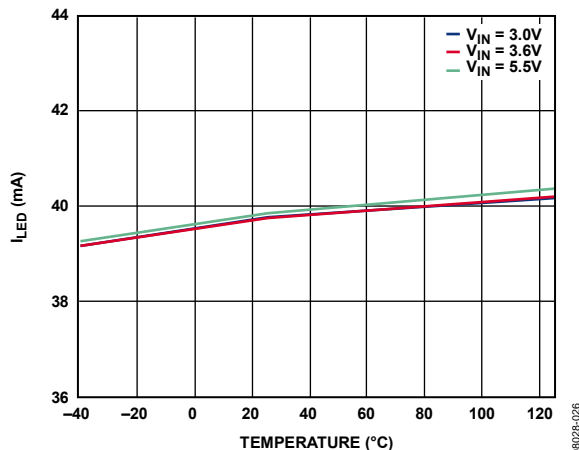


Figure 26. LED Regulation, Set at 40 mA, Current Set Register = 001 (Binary)

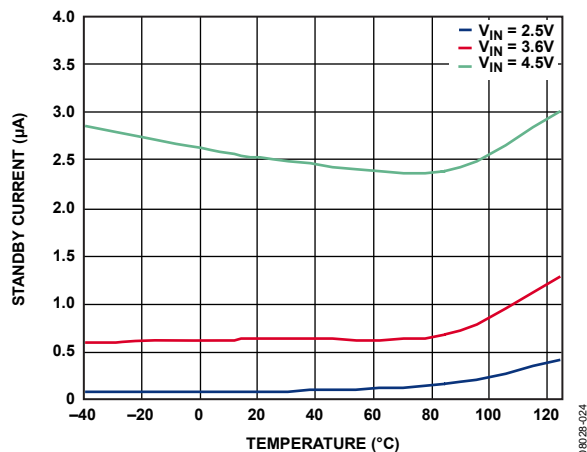


Figure 24. Standby Current vs. Temperature vs.  $V_{IN}$ ,  $I_{2C}/EN = SCL/EN1 = SDA/EN2 = 1.8V$

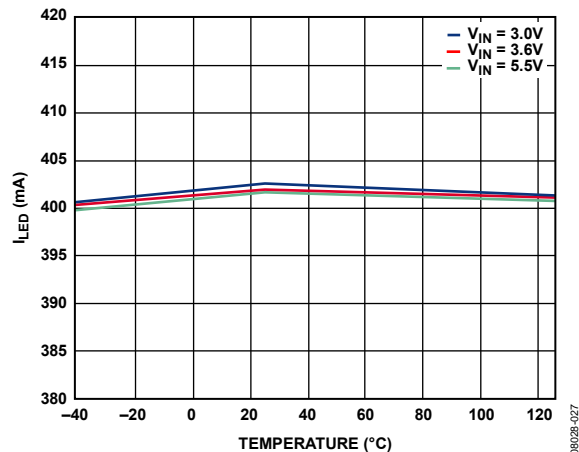


Figure 27. LED Regulation, Set at 400 mA, Current Set Register = 1010 (Binary)

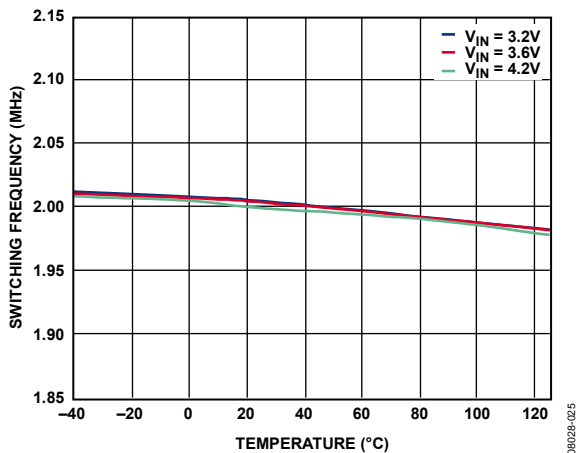


Figure 25. Switching Frequency vs. Temperature vs.  $V_{IN}$

## THEORY OF OPERATION

The ADP1655 is a high power, white LED driver ideal for driving white LEDs for use as a camera flash. The ADP1655 includes a boost converter and a current regulator suitable for powering one or two high power, white LEDs.

The ADP1655 responds to a 2-pin control interface that can operate in two separate pin-selectable modes: tying the I2C/EN pin high enables the I<sup>2</sup>C interface; tying the I2C/EN pin low enables a 2-bit logic interface.

### WHITE LED DRIVER

The ADP1655 drives a synchronous boost converter to power one or two series-connected, high power LEDs. The white LED driver regulates the high power LED current for accurate brightness control. The ADP1655 uses an integrated PFET current regulator.

When the white LED is turned on, the step-up converter output voltage slew is limited to prevent excessive battery current while charging the output capacitor. The output voltage of the boost

converter is sensed at VOUT. If the output voltage exceeds the 9.5 V (typical) limit, the white LED driver turns off and indicates that a fault condition has occurred through the system registers. This feature prevents damage due to an overvoltage if the white LED string fails with an open-circuit condition.

Setting the LED regulation currents depends on the 2-pin control interface used.

### ASSIST LIGHT AND TORCH MODES

The ADP1655 features a programmable assist light mode that provides continuous LED current. The STROBE pin or the 2-bit logic interface can be used to transition from assist light mode directly to flash mode. The TORCH pin provides an alternative means of accessing a continuous LED current mode of operation. Both assist light and torch modes deliver the same current, which is programmable via the I<sup>2</sup>C-compatible interface.

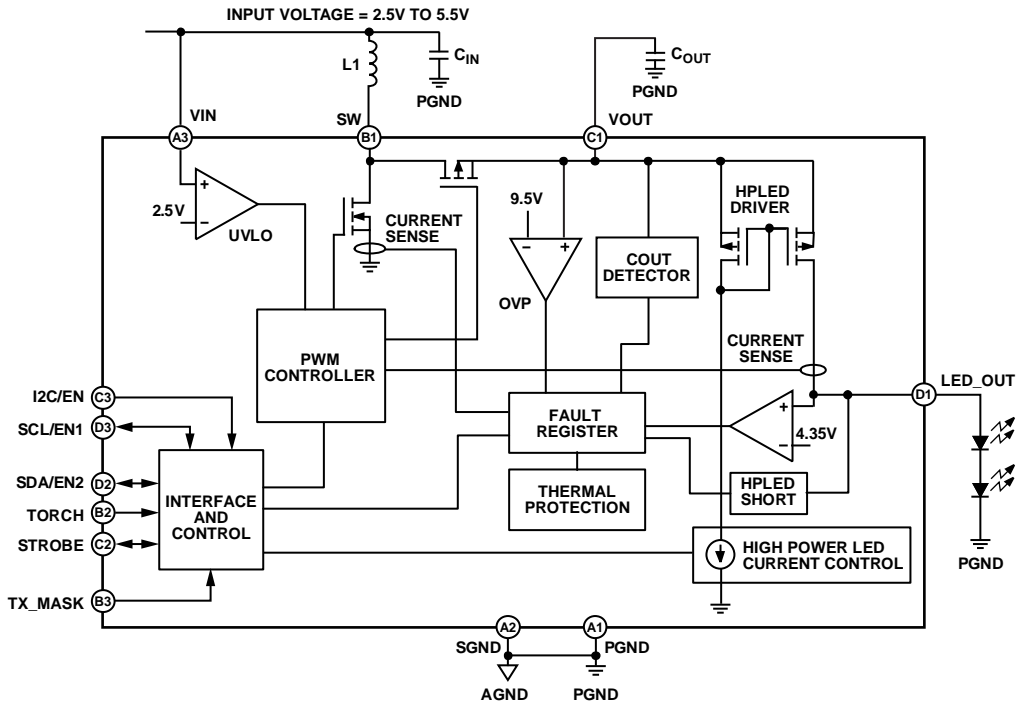


Figure 28. Detailed Block Diagram

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### 2-BIT LOGIC INTERFACE MODE (I2C/EN = 0)

In 2-bit logic interface mode, the two control pins, EN1 and EN2, select whether the part is disabled or operating in assist light mode or flash mode, as outlined in Table 6. Additionally, the TORCH pin selects torch mode.

Figure 29 illustrates state transitions of 2-bit logic mode controlled by digital inputs EN1, EN2, TORCH, and TX\_MASK.

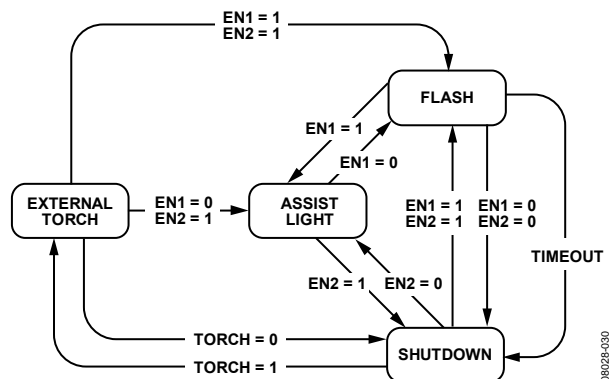


Figure 29. 2-Bit Logic Mode State Transitions (I2C/EN = 0)

When the ADP1655 is in flash mode, the TX\_MASK pin can be used to reduce the battery load. The device remains in flash mode, but the LED driver output current is reduced to the assist light level.

Table 6. 2-Bit Logic Interface Mode Selection

Mode	I2C/ EN	EN1	EN2	TORCH	Output Current
Shutdown	0	0	0	0	0 mA
Torch	0	0	0	1	One LED: 80 mA Two LEDs: 40 mA
Assist light	0	0	1	X	One LED: 80 mA Two LEDs: 40 mA
Reserved	0	1	0	X	0 mA
Flash	0	1	1	X	One LED: 500 mA Two LEDs: 320 mA

### I<sup>2</sup>C INTERFACE MODE (I2C/EN = 1)

The ADP1655 includes an I<sup>2</sup>C-compatible serial interface for control of the LED current, as well as for a readback of system status registers. The I<sup>2</sup>C chip address is 0x60 in write mode and 0x61 in read mode.

Table 7. I<sup>2</sup>C Interface Mode Selection

Mode	I2C/ EN	SCL	SDA	TORCH	Output Current
Standby	1	X	X	0	0 mA
Torch	1	X	X	1	20 mA to 160 mA <sup>1,2</sup>
Assist light	1	X	X	X	20 mA to 160 mA <sup>2</sup>
Flash	1	X	X	X	200 mA to 500 mA <sup>2</sup>

<sup>1</sup> Torch mode has to be enabled from Register 0x04.

<sup>2</sup> The output current value depends on the register settings.

Registers values are reset to the default values when VIN supply falls below the undervoltage (UVLO) level.

Figure 30 illustrates the I<sup>2</sup>C write sequence to a single register. The subaddress content selects which of the five ADP1655 registers is written to first. The ADP1655 sends an acknowledgement to the master after the 8-bit data byte has been written. The ADP1655 increments the subaddress automatically and starts receiving a data byte to the following register until the master sends an I<sup>2</sup>C stop as shown in Figure 31. Figure 32 shows the I<sup>2</sup>C read sequence of a single register. ADP1655 sends the data from the register denoted by the subaddress and increments the subaddress automatically, sending data from the next register until the master sends an I<sup>2</sup>C stop condition as shown in Figure 33.

State transitions between standby, assist light, flash, and external torch modes are described in the State Transitions section and Figure 34.

The register definitions are shown in the I<sup>2</sup>C Register Map section. The lowest bit number (0) represents the least significant bit, and the highest bit number (7) represents the most significant bit.



**STATE TRANSITIONS**

When the ADP1655 is in flash mode, the TX\_MASK pin can be used to reduce the battery load. The device remains in flash mode, but the LED driver output current is reduced to the assist

light level. In Figure 34, if the flash was triggered by the strobe pin in level-sensitive mode, a timeout triggers a timeout fault, as defined in the Safety Features section.

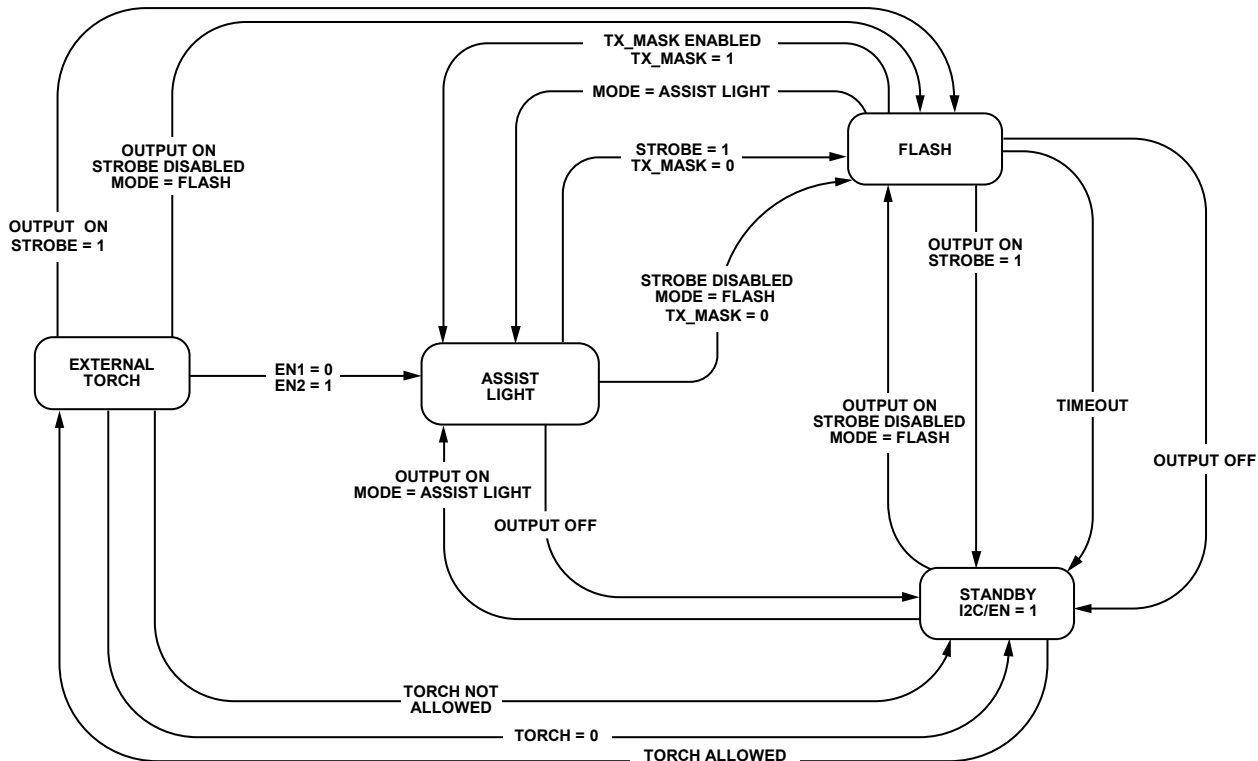


Figure 34. PC Interface Mode: State Transitions

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# ADP1655

## I<sup>2</sup>C REGISTER MAP

The lowest bit number (0) represents the least significant bit, and the highest bit number (7) represents the most significant bit.

**Table 8. Design Information Register (Register 0x00)**

Bit	R/W	Reset State
7:0	R	00100001

**Table 9. Version Register (Register 0x01)**

Bit	R/W	Reset State
7:0	R	00000001

**Table 10. VREF and Timer Register (Register 0x02)**

Bit	R/W	Description
7:6	R/W	Reserved
5:4	R/W	Number of LEDs detection comparator reference level 00 = 4.3 V (default) 01 = 4.6 V 10 = 4.0 V 11 = 4.9 V
3:0	R/W	Flash timer value setting 0000 = 100 ms 0001 = 150 ms 0010 = 200 ms 0011 = 250 ms 0100 = 300 ms 0101 = 350 ms 0110 = 400 ms 0111 = 450 ms 1000 = 500 ms 1001 = 550 ms 1010 = 600 ms 1011 = 650 ms 1100 = 700 ms 1101 = 750 ms 1110 = 800 ms 1111 = 850 ms (default)



Table 11. Current Set Register (Register 0x03)

Bit	R/W	Description
7:4	R/W	Flash current value setting 0000 = 200 mA 0001 = 220 mA 0010 = 240 mA 0011 = 260 mA 0100 = 280 mA 0101 = 300 mA 0110 = 320 mA (default for two LEDs) 0111 = 340 mA 1000 = 360 mA 1001 = 380 mA 1010 = 400 mA 1011 = 420 mA 1100 = 440 mA 1101 = 460 mA 1110 = 480 mA 1111 = 500 mA (default for one LED)
3		N/A
2:0	R/W	Torch and assist light current value setting 000 = 20 mA 001 = 40 mA (default) 010 = 60 mA 011 = 80 mA 100 = 100 mA 101 = 120 mA 110 = 140 mA 111 = 160 mA

Table 12. Output Mode Register (Register 0x04)

Bit	R/W	Description
7:6	R/W	Inductor peak current limit setting 00 = 1.25 A 01 = 1.5 A 10 = 1.75 A (default) 11 = 2.0 A
5	R/W	0 = edge sensitive 1 = level sensitive (default)
4	R/W	0 = TORCH not allowed 1 = TORCH allowed (default)
3	R/W	0 = LED_OUT off (default) 1 = LED_OUT on
2	R/W	0 = STROBE disabled 1 = STROBE enabled (default)
1:0	R/W	Configures LED output mode 00 = standby mode (default) 01 = reserved 10 = assist light mode 11 = flash mode

# ADP1655

**Table 13. Fault Information Register (Register 0x05)**

Bit	R/W	Description
7	R	0 = no fault (default) 1 = overvoltage or C <sub>OUT</sub> fault
6	R	0 = no fault (default) 1 = short-circuit fault
5	R	0 = no fault (default) 1 = overtemperature fault
4	R	0 = no fault (default) 1 = timeout 850 ms fault
3	R/W	0 = one LED 1 = two LEDs (default)
2	R	Reserved
1	R	0 = no fault (default) 1 = current limit fault
0	R	Reserved

**Table 14. Input Control Register (Register 0x06)**

Bit	R/W	Description
7:3		Reserved
2	R/W	0 = Strobe 0 triggers flash in level sensitive mode, Strobe 1 > 0 triggers flash in edge sensitive mode 1 = Strobe 1 triggers flash in level sensitive mode, Strobe 0 > 1 triggers flash in edge sensitive mode (default)
1	R/W	0 = TX_MASK function disabled 1 = TX_MASK function allowed (default)
0	R	Reserved

## SAFETY FEATURES

For critical system conditions, such as output overvoltage, flash timeout, LED output short circuit, and overtemperature conditions, the ADP1655 has built-in safety mechanisms. If one of the fault conditions occurs, the device shuts down and a corresponding flag is set in the fault information register (Register 0x05). In I<sup>2</sup>C interface mode, the system baseband processor can read the fault information register through the I<sup>2</sup>C interface to determine the nature of the fault condition and, consequently, the fault flag is cleared. The device is disabled until the fault information register is cleared.

In 2-bit logic interface mode, the I<sup>2</sup>C register readback is not available. To clear a fault, set EN1, EN2, and TORCH low.

### OVERVOLTAGE FAULT

The ADP1655 contains a comparator at the VOUT pin that monitors the voltage between VOUT and SGND. If the voltage exceeds 9.5 V (typical), the ADP1655 shuts down. In I<sup>2</sup>C mode, Bit 7 in the fault information register is read back as high. The ADP1655 is disabled until the fault is cleared, ensuring protection against an open circuit.

### OUTPUT CAPACITOR FAULT

If no output capacitor is present at the VOUT pin when the ADP1655 is enabled for a flash, torch, or assist light event, the part shuts down and Bit 7 in the fault information register is read back as high. The ADP1655 is disabled until the fault is cleared. The output capacitor detection scheme does not cause the VOUT pin to rise above the overvoltage threshold even though the overvoltage flag (Bit 7) in the fault information register (Register 5) is set. The overvoltage and output capacitor fault flags share a single register bit to reduce the required number of registers.

### TIMEOUT FAULT

If the 2-bit logic interface is used, the maximum duration for flash being enabled (EN1/EN2 = 1) is preset to 850 ms. If EN1 and EN2 remain high for longer than 850 ms, ADP1655 is disabled until the fault is cleared (EN1, EN2, and TORCH low).

In I<sup>2</sup>C mode, if strobe mode is enabled (Register 0x04, Bit 2), strobe is set to level sensitive mode (Register 0x04, Bit 5), and if strobe remains high for longer than 850 ms, the timeout fault bit, Register 0x05, Bit 4), is read back as high. The ADP1655 is disabled until the fault is cleared.

### OVERTEMPERATURE FAULT

If the junction temperature of the ADP1655 rises above 150°C, a thermal protection circuit shuts down the device. In I<sup>2</sup>C mode, Bit 5 of the fault information register is read back as high. The ADP1655 is disabled until the fault is cleared.

### SHORT-CIRCUIT FAULT

The LED\_OUT pin features short-circuit protection that disables the ADP1655 if it detects a short circuit to ground at the LED\_OUT pin. The ADP1655 monitors the LED voltage when the LED driver is enabled. If the LED\_OUT pin remains below the short-circuit detection threshold during startup, a short circuit is detected. Bit 6 of the fault information register is read back as high. The ADP1655 is disabled until the fault is cleared.

### CURRENT LIMIT

The internal switch limits battery current by ensuring that the peak inductor current does not exceed the programmed limit (current limit is set by Bit 6 and Bit 7 in the output mode register, Register 0x04). If the peak inductor current exceeds the limit, the part shuts down and Bit 1 of the fault information register is read back as high. The ADP1655 is disabled until the fault is cleared.

### AMOUNT OF LED DETECTION

The ADP1655 is able to detect the amount of LED connected in series between the LED\_OUT pin and the PGND potential. In I<sup>2</sup>C mode, the detection is enabled with Bit 3 in the output mode register. The part uses an 80 mA LED driver current setting to detect the LED forward voltage (V<sub>f</sub>) with a voltage comparator at the start of a flash, torch, or assist light event. If the detected forward voltage is higher than 4.3 V (typical), Bit 3 of the fault information register is read back as high.

### INPUT UNDERVOLTAGE

The ADP1655 includes an input undervoltage lockout circuit. If the battery voltage drops below the 2.4 V (typical) input UVLO threshold, the ADP1655 shuts down. In this case, information in all registers is lost, and when power is reapplied, a power-on reset circuit resets the registers to their default conditions.

## APPLICATIONS INFORMATION

### EXTERNAL COMPONENT SELECTION

#### Selecting the Inductor

The ADP1655 boost converter increases the battery voltage to allow driving of one or two LEDs, whose combined voltage drop is higher than the battery voltage plus the current source headroom voltage. This allows the converter to regulate the LED current over the entire battery voltage range and with a wide variation of LED forward voltage.

The inductor saturation current should be greater than the sum of the dc input current and half the inductor ripple current. A reduction in the effective inductance due to saturation increases the inductor current ripple. Suggested inductors are shown in Table 15.

**Table 15. Suggested Inductors**

Vendor	Value (μH)	Part No.	DCR (mΩ)	ISAT (A)	Dimensions L × W × H (mm)
Toko	2.2	FDSE0312	160	3.1	3 × 3 × 1.2
Toko	2.0	DE2812C	67	1.8	3.0 × 3.2 × 1.22
Coilcraft	2.2	LPS3010	220	1.4	3 × 3 × 1.0
Coilcraft	2.2	LPS3314	100	1.5	3 × 3 × 1.4

#### Selecting the Input Capacitor

The ADP1655 requires an input bypass capacitor to supply transient currents while maintaining constant input and output voltages. The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. Use an input capacitor with a sufficient ripple current rating to handle the inductor ripple. Increased input capacitance reduces the amplitude of the switching frequency ripple on the battery. Because of the dc bias characteristics of ceramic capacitors, a 0603, 6.3 V X5R/X7R, 10 μF ceramic capacitor is preferable.

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the ADP1655 as possible. As with the output capacitor, a low ESR capacitor is suggested. A list of suggested input capacitors is shown in Table 16.

**Table 16. Suggested Input Capacitors**

Vendor	Value	Part No.	Dimensions L × W × H (mm)
Murata	10 μF, 6.3 V	GRM188R60J106ME47	1.6 × 0.8 × 0.8
TDK	10 μF, 6.3 V	C1608JB0J106K	1.6 × 0.8 × 0.8
Taiyo Yuden	10 μF, 6.3 V	JMK107BJ106MA	1.6 × 0.8 × 0.8

#### Selecting the Output Capacitor

The output capacitor maintains the output voltage and supplies the LED current during NFET power switch on period. It also stabilizes the loop. A 10.0 μF, 16 V X5R/X7R ceramic capacitor is suggested.

Note that dc bias characterization data is available from capacitor manufacturers and should be taken into account when selecting input and output capacitors. 16 V capacitors are recommended for most two-LED designs. Designs with 1 mm height restrictions can also use 0603 case size, 16 V capacitors in parallel. A list of suggested output capacitors is shown in Table 17.

**Table 17. Suggested Output Capacitors**

Vendor	Value	Part No.	Dimensions L × W × H (mm)
Murata	10.0 μF, 10 V	GRM21BR71A106KE51	2 × 1.25 × 1.25
Murata	10.0 μF, 16 V	GRM31CR61C106KA88	3.2 × 1.6 × 1.6
Taiyo Yuden	10.0 μF, 16 V	EMK212BJ106KG	2 × 1.25 × 1.25

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric that ensures the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 10.0 V or 16 V are suggested for best performance. Y5V and Z5U dielectrics are not suggested for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:

$C_{EFF}$  is the effective capacitance at the operating voltage.

$TEMPCO$  is the worst-case capacitor temperature coefficient.

$TOL$  is the worst-case component tolerance.

In this example,  $TEMPCO$  over  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  is assumed to be 15% for an X5R dielectric,  $TOL$  is assumed to be 10%, and  $C_{OUT}$  is  $9.528\ \mu\text{F}$  at 1.8 V, as shown in Figure 35.

Substituting these values in the equation yields

$$C_{EFF} = 9.528\ \mu\text{F} \times (1 - 0.15) \times (1 - 0.1) = 7.288\ \mu\text{F}$$

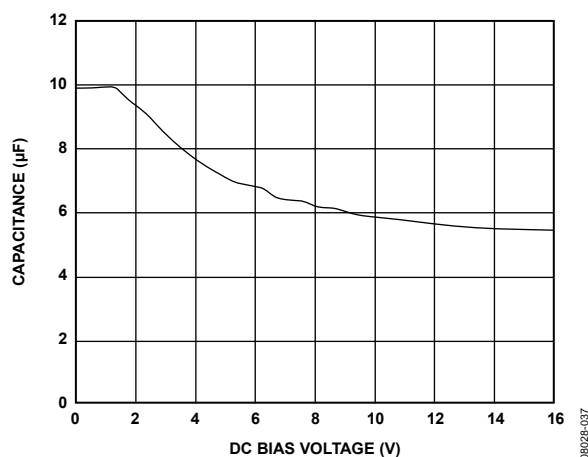


Figure 35. DC Bias Characteristic of a 16 V, 10  $\mu\text{F}$  Ceramic Capacitor

To guarantee the performance of the ADP1655, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{V_{IN}}{(2\pi \times f_{SW}) \times 2 \times L \times C_{OUT}} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{C_{OUT}} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is  $4\ \mu\text{F}$ .

## PCB LAYOUT

Poor layout can affect performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following rules and shown in Figure 36:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies and large tracks act as antennas.

- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

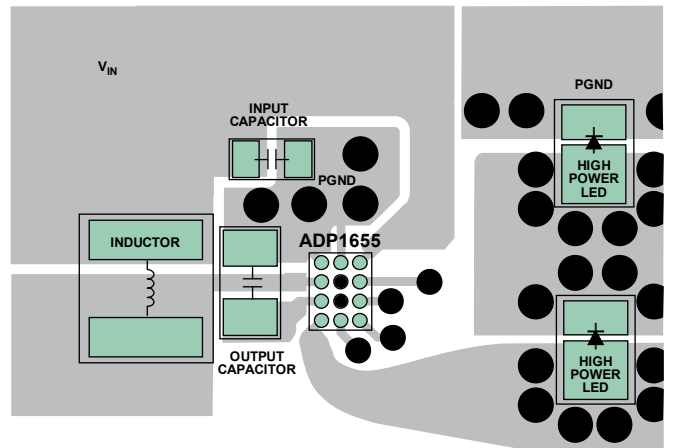


Figure 36. Example Layout of the ADP1655 Driving Two White LEDs

# OUTLINE DIMENSIONS

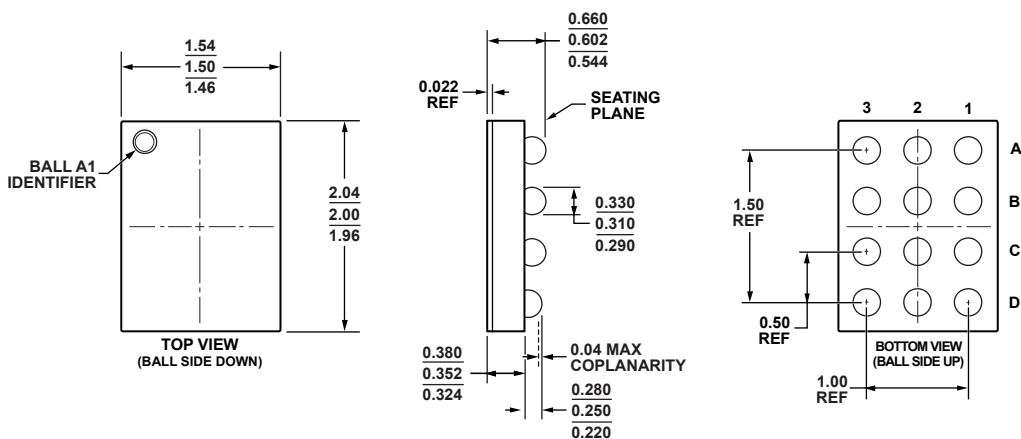


Figure 37. 12-Ball Wafer Level Chip Scale Package [WLCSP] (CB-12-4)

Dimensions shown in millimeters

020409-B

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADP1655ACBZ-R7 <sup>1</sup>	-40°C to +125°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	CB-12-4	LAM
ADP1655-EVALZ <sup>1</sup>		Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

**ADP1655**

**NOTES**