ADC1006S055/070

Single 10 bits ADC, up to 55 MHz or 70 MHz

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1006S055/070 are a family of Bipolar CMOS (BiCMOS) 10-bit Analog-to-Digital Converters (ADC) optimized for a wide range of applications such as cellular infrastructures, professional telecommunications, imaging, and digital radio. It converts the analog input signal into 10-bit binary coded digital words at a maximum sampling rate of 70 MHz. All static digital inputs (SH, $\overline{CE}$ and OTC) are Transistor-Transistor Logic (TTL) and CMOS compatible and all outputs are CMOS compatible. A sine wave clock input signal can also be used.

2. Features

- 10-bit resolution
- Sampling rate up to 70 MHz
- −3 dB bandwidth of 245 MHz
- 5 V power supplies and 3.3 V output power supply
- Binary or two's complement CMOS outputs
- In-range CMOS compatible output
- TTL and CMOS compatible static digital inputs
- TTL and CMOS compatible digital outputs
- Differential AC or Positive Emitter-Coupled Logic (PECL) clock input; TTL compatible
- Power dissipation 550 mW (typical)
- Low analog input capacitance (typical 2 pF), no buffer amplifier required
- Integrated sample-and-hold amplifier
- Differential analog input
- External amplitude range control
- Voltage controlled regulator included
- −40 °C to +85 °C ambient temperature

3. Applications

High-speed analog-to-digital conversion for:

- Cellular infrastructure
- Professional telecommunication
- Digital radio
- Radar
- Medical imaging
- Fixed network
- Cable modem

- Barcode scanner
- Cable Modem Termination System (CMTS)/Data Over Cable Service Interface Specification (DOCSIS)

4. Quick reference data

Table 1. Quick reference data

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	3.6	V
I_{CCA}	analog supply current		-	78	87	mA
I_{CCD}	digital supply current		-	27	30	mA
I_{CCO}	output supply current	f_{clk} = 20 MHz; f_i = 400 kHz	-	3	4	mA
INL	integral non-linearity	f_{clk} = 20 MHz; f_i = 400 kHz	-	±0.65	±1.12	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; f_i = 400 kHz (no missing code guaranteed)	-	±0.12	±0.27	LSB
$f_{clk(max)}$	maximum clock frequency	ADC1006S055H	55	-	-	MHz
		ADC1006S070H	70	-	-	MHz
P_{tot}	total power dissipation	f_{clk} = 55 MHz; f_i = 20 MHz	-	550	660	mW

5. Ordering information

Table 2. Ordering information

Type number	Package			Sampling frequency (MHz)
	Name	Description	Version	
ADC1006S055H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	55
ADC1006S070H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	70

6. Block diagram

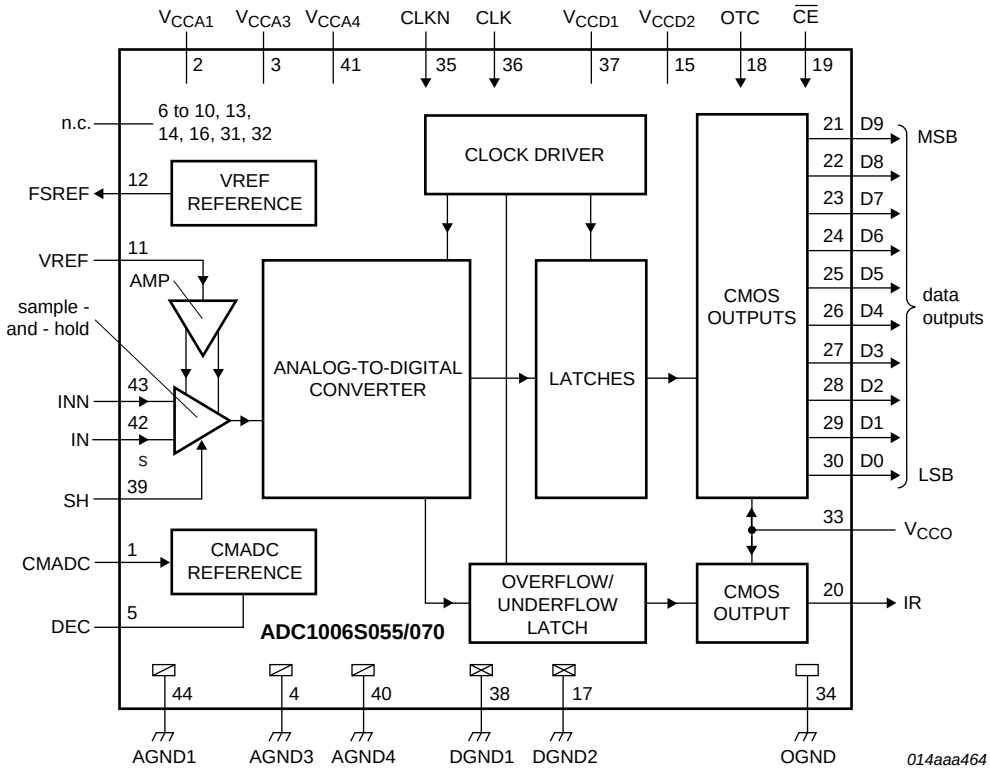


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

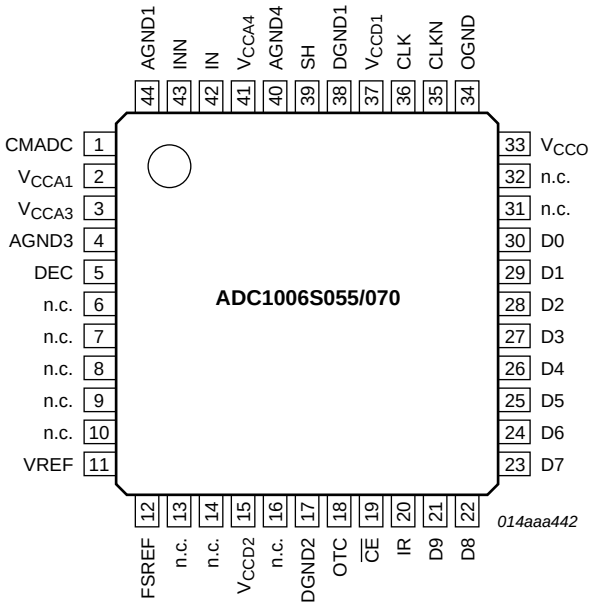


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CMADC	1	regulator output common mode ADC input
V_{CCA1}	2	analog supply voltage 1 (5 V)
V_{CCA3}	3	analog supply voltage 3 (5 V)
AGND3	4	analog ground 3
DEC	5	decoupling node
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
VREF	11	reference voltage input
FSREF	12	full-scale reference output
n.c.	13	not connected
n.c.	14	not connected
V_{CCD2}	15	digital supply voltage 2 (5 V)
n.c.	16	not connected
DGND2	17	digital ground 2

Table 3. Pin description *…continued*

Symbol	Pin	Description
OTC	18	control input two's complement output; active HIGH
$\overline{CE}$	19	chip enable input (CMOS level; active LOW)
IR	20	in-range output
D9	21	data output; bit 9 (Most Significant Bit (MSB))
D8	22	data output; bit 8
D7	23	data output; bit 7
D6	24	data output; bit 6
D5	25	data output; bit 5
D4	26	data output; bit 4
D3	27	data output; bit 3
D2	28	data output; bit 2
D1	29	data output; bit 1
D0	30	data output; bit 0 (Least Significant Bit (LSB))
n.c.	31	not connected
n.c.	32	not connected
V_{CCO}	33	output supply voltage (3.3 V)
OGND	34	output ground
CLKN	35	complementary clock input
CLK	36	clock input
V_{CCD1}	37	digital supply voltage 1 (5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V_{CCA4}	41	analog supply voltage 4 (5 V)
IN	42	analog input voltage
INN	43	complementary analog input voltage
AGND1	44	analog ground 1

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	−0.3	+7.0	V
V_{CCD}	digital supply voltage		[1]	−0.3	+7.0	V
V_{CCO}	output supply voltage		[1]	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$		−1.0	+1.0	V
		$V_{CCD} - V_{CCO}$		−1.0	+4.0	V
		$V_{CCA} - V_{CCO}$		−1.0	+4.0	V
$V_{i(IN)}$	input voltage on pin IN	referenced to AGND		0.3	V_{CCA}	V
$V_{i(INN)}$	input voltage on pin INN			0.3	V_{CCA}	V

Table 4. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage	differential clock drive at pins 35 and 36	-	V_{CCD}	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	150	°C

[1] The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

10. Characteristics

Table 6. Characteristics

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			4.75	5.0	5.25	V
V_{CCD}	digital supply voltage			4.75	5.0	5.25	V
V_{CCO}	output supply voltage			3.0	3.3	3.6	V
I_{CCA}	analog supply current		I	-	78	87	mA
I_{CCD}	digital supply current		I	-	27	30	mA
I_{CCO}	output supply current	f_{clk} = 20 MHz; f_i = 400 kHz	I	-	3	4	mA
		f_{clk} = 55 MHz; f_i = 20 MHz	I	-	9.5	12	mA
P_{tot}	total power dissipation	f_{clk} = 55 MHz; f_i = 20 MHz		-	550	660	mW
Inputs							
CLK and CLKN (referenced to DGND)[2]							
V_{IL}	LOW-level input voltage	PECL mode; V_{CCD} = 5 V	I	3.19	-	3.52	V
		TTL mode	C	0	-	0.8	V

Table 6. Characteristics *…continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	PECL mode; V_{CCD} = 5 V	I	3.83	-	4.12	V
		TTL mode	C	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} or V_{CLKN} = 3.19 V	C	−10	-	-	μA
I_{IH}	HIGH-level input current	V_{CLK} or V_{CLKN} = 3.83 V	C	-	-	10	μA
$V_{i(dif)(p-p)}$	peak-to-peak differential input voltage	AC driving mode; DC voltage level = 2.5 V	C	1	1.5	2.0	V
R_i	input resistance	f_{clk} = 55 MHz	D	2	-	-	kΩ
C_i	input capacitance	f_{clk} = 55 MHz	D	-	-	2	pF
OTC, SH and $\overline{CE}$ (referenced to DGND); see Table 7 and 8							
V_{IL}	LOW-level input voltage		I	0	-	0.8	V
V_{IH}	HIGH-level input voltage		I	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	I	−20	-	-	μA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	I	-	-	20	μA
IN and INN (referenced to AGND); see Table 7, $V_{VREF} = V_{CCA3} - 1.75$ V							
I_{IL}	LOW-level input current	SH = HIGH	C	-	10	-	μA
I_{IH}	HIGH-level input current	SH = HIGH	C	-	10	-	μA
R_i	input resistance	f_i = 20 MHz	D	-	14	-	MΩ
C_i	input capacitance	f_i = 20 MHz	D	-	450	-	fF
$V_{I(cm)}$	common-mode input voltage	$V_{I(IN)} = V_{I(INN)}$ output code 512	C	$V_{CCA3} - 1.7$	$V_{CCA3} - 1.6$	$V_{CCA3} - 1.2$	V
Voltage controlled regulator output CMADC							
$V_{O(cm)}$	common-mode output voltage		I	-	$V_{CCA3} - 1.6$	-	V
I_{load}	load current		I	-	1	2	mA
Voltage input V_{ref}[3]							
V_{ref}	reference voltage	full-scale fixed voltage; f_i = 20 MHz; f_{clk} = 55 MHz	C	-	$V_{CCA3} - 1.75$	-	V
I_{ref}	reference current		C	-	0.3	10	μA
$V_{i(dif)(p-p)}$	peak-to-peak differential input voltage	$V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V	C	-	1.9	-	V

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Voltage controlled regulator output FSREF							
$V_{O(ref)}$	reference output voltage	$V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V	I	-	$V_{CCA3} - 1.75$	-	V
Digital outputs D9 to D0 and IR (referenced to OGND)							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	I	0	-	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = −0.4 mA	I	$V_{CCO} - 0.5$	-	V_{CCO}	V
I_o	output current	3-state output level between 0.5 V and V_{CCO}	I	−20	-	+20	μA
Switching characteristics; Clock frequency f_{clk}; see Figure 3							
$f_{clk(min)}$	minimum clock frequency	SH = HIGH	C	-	-	7	MHz
$f_{clk(max)}$	maximum clock frequency	ADC1006S055H	I	55	-	-	MHz
		ADC1006S070H	C	70	-	-	MHz
$t_{w(clk)H}$	HIGH clock pulse width	f_i = 20 MHz	C	6.8	-	-	ns
$t_{w(clk)L}$	LOW clock pulse width	f_i = 20 MHz	C	6.8	-	-	ns
Analog signal processing; 50 % clock duty factor; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; see Table 7							
Linearity							
INL	integral non-linearity	f_{clk} = 20 MHz; f_i = 400 kHz	I	-	±0.65	±1.12	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; f_i = 400 kHz (no missing code guaranteed)	I	-	±0.12	±0.27	LSB
E_{offset}	offset error	$V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C; output code = 512	C	−25	+5	+25	mV
E_G	gain error	spread from device to device; $V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C	C	−7	-	+7	%FS
Bandwidth (f_{clk} = 55 MHz)[4]							
B	bandwidth	−3 dB; full-scale input	C	220	245	-	MHz

Table 6. Characteristics *…continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Harmonics							
α_{2H}	second harmonic level	ADC1006S055H (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	−77	-	dBFS
		f_i = 10 MHz	C	-	−76	-	dBFS
		f_i = 15 MHz	C	-	−75	-	dBFS
		f_i = 20 MHz	I	-	−73	-	dBFS
		ADC1006S070H (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	−75	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−70	-	dBFS
α_{3H}	third harmonic level	ADC1006S055H (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	−73	-	dBFS
		f_i = 10 MHz	C	-	−73	-	dBFS
		f_i = 15 MHz	C	-	−73	-	dBFS
		f_i = 20 MHz	I	-	−72	-	dBFS
		ADC1006S070H (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	−73	-	dBFS
		f_i = 10 MHz	C	-	−73	-	dBFS
		f_i = 15 MHz	C	-	−72	-	dBFS
Total harmonic distortion[5]							
THD	total harmonic distortion	ADC1006S055H (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−68	-	dBFS
		f_i = 15 MHz	C	-	−68	-	dBFS
		f_i = 20 MHz	I	-	−68	-	dBFS
		ADC1006S070H (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	−67	-	dBFS
		f_i = 10 MHz	C	-	−67	-	dBFS
		f_i = 15 MHz	C	-	−66	-	dBFS
Thermal noise							
$N_{th(RMS)}$	RMS thermal noise	shorted input; SH = HIGH; f_{clk} = 55 MHz	C	-	0.12	-	LSB

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Signal-to-noise ratio[6]							
S/N	signal-to-noise ratio	ADC1006S055H (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	60	-	dBFS
		f_i = 10 MHz	C	-	60	-	dBFS
		f_i = 15 MHz	C	-	60	-	dBFS
		f_i = 20 MHz	I	-	59.5	-	dBFS
		ADC1006S070H (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	60	-	dBFS
		f_i = 10 MHz	C	-	60	-	dBFS
		f_i = 15 MHz	C	-	59	-	dBFS
Spurious free dynamic range; see Figure 7, 13 and 14							
SFDR	spurious free dynamic range	ADC1006S055H (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	71	-	dBFS
		f_i = 10 MHz	C	-	70	-	dBFS
		f_i = 15 MHz	C	-	70	-	dBFS
		f_i = 20 MHz	I	-	70	-	dBFS
		ADC1006S070H (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	70	-	dBFS
		f_i = 10 MHz	C	-	69	-	dBFS
		f_i = 15 MHz	C	-	68	-	dBFS
Effective number of bits[7]							
ENOB	effective number of bits	ADC1006S055H (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	9.5	-	bit
		f_i = 10 MHz	C	-	9.5	-	bit
		f_i = 15 MHz	C	-	9.5	-	bit
		f_i = 20 MHz	I	-	9.5	-	bit
		ADC1006S070H (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	9.5	-	bit
		f_i = 10 MHz	C	-	9.5	-	bit
		f_i = 15 MHz	C	-	9.4	-	bit
Intermodulation; (f_{clk} = 55 MHz; f_i = 20 MHz)[8]							
α_{IM}	intermodulation suppression		C	-	−69	-	dBFS
IMD3	third-order intermodulation distortion		C	-	−79	-	dBFS
Bit error rate (f_{clk} = 55 MHz)							
BER	bit error rate	f_i = 20 MHz; V_I = ±16 LSB at code 512	C	-	10^{-14}	-	times/ sample

Table 6. Characteristics *…continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to +85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{VREF} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Timing (C_L = 10 pF)[9]							
$t_{d(s)}$	sampling delay time		C	-	0.25	1	ns
$t_{h(o)}$	output hold time		C	4	6.4	-	ns
$t_{d(o)}$	output delay time		C	-	9.0	13	ns
3-state output delay times; see Figure 4							
t_{dZH}	float to active HIGH delay time		C	-	5.1	9.0	ns
t_{dZL}	float to active LOW delay time		C	-	7.0	11	ns
t_{dHZ}	active HIGH to float delay time		C	-	9.7	14	ns
t_{dLZ}	active LOW to float delay time		C	-	9.5	13	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] The circuit has two clock inputs: CLK and CLKN. There are 5 modes of operation:

a) PECL mode 1: (DC level vary 1 : 1 with V_{CCD}) CLK and CLKN inputs are at differential PECL levels.

b) PECL mode 2: (DC level vary 1 : 1 with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on CLKN decoupled to GND via a 100 nF capacitor.

c) PECL mode 3: (DC level vary 1 : 1 with V_{CCD}) CLKN input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.

d) Differential AC driving mode 4: When driving the CLK input directly and with any AC signal of minimum 1 V (p-p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal. When driving the CLKN input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the CLKN or CLK input to DGND via a 100 nF capacitor.

e) TTL mode 1: CLK input is at TTL level and sampling is taken on the falling edge of the clock input signal. In that case CLKN pin has to be connected to the ground.

[3] The ADC input range can be adjusted with an external reference connected to VREF pin. This voltage has to be referenced to V_{CCA}; see Figure 12.

[4] The −3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.

[5] Total Harmonic Distortion (THD) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \sqrt{\frac{(\alpha_{2H})^2 + (\alpha_{3H})^2 + (\alpha_{4H})^2 + (\alpha)^2 + (\alpha_{6H})^2}{(a_{1H})^2}}$$

where α_{1H} is the fundamental harmonic referenced at 0 dB for a full-scale sine wave input; see Figure 6.

[6] Signal-to-noise ratio (S/N) takes into account all harmonics above five and noise up to Nyquist frequency; see Figure 8.

[7] Effective number of bits are obtained via a Fast Fourier Transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to SIgnal-to_Noise_Distortion ratio (SINAD) is given by SINAD = ENOB × 6.02 + 1.76 dB; see Figure 5.

[8] Intermodulation measured relative to either tone with analog input frequencies of 20 MHz and 20.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (−6 dB below full scale for each input signal). IMD3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.

[9] Output data acquisition: the output data is available after the maximum delay of $t_{d(o)}$; see Figure 3.

11. Additional information relating to Table 6

Table 7. Output coding with differential inputs (typical values to AGND); $V_{i(IN)(p-p)} - V_{i(INN)(p-p)}$ = 1.9 V, $V_{VREF} = V_{CCA3} - 1.75$ V

Code	$V_{i(a)(p-p)}$ (V)	$V_{i(a)(p-p)}$ (V)	IR	Binary outputs D9 to D0	Two's complement outputs[1] D9 to D0
Underflow	< 3.125	> 4.075	0	00 0000 0000	10 0000 0000
0	3.125	4.075	1	00 0000 0000	10 0000 0000
1	-	-	1	00 0000 0001	10 0000 0001
↓	-	-	↓	↓	↓
511	3.6	3.6	1	01 1111 1111	11 1111 1111
↓	-	-	↓	↓	↓
1022	-	-	1	11 1111 1110	01 1111 1110
1023	4.075	3.125	1	11 1111 1111	01 1111 1111
Overflow	> 4.075	< 3.125	0	11 1111 1111	01 1111 1111

[1] Two's complement reference is inverted MSB.

Table 8. Mode selection

OTC	$\overline{CE}$	D0 to D9 and IR
0	0	binary; active
1	0	two's complement; active
X[1]	1	high-impedance

[1] X = don't care.

Table 9. Sample-and-hold selection

SH	Sample-and-hold
1	active
0	inactive; tracking mode

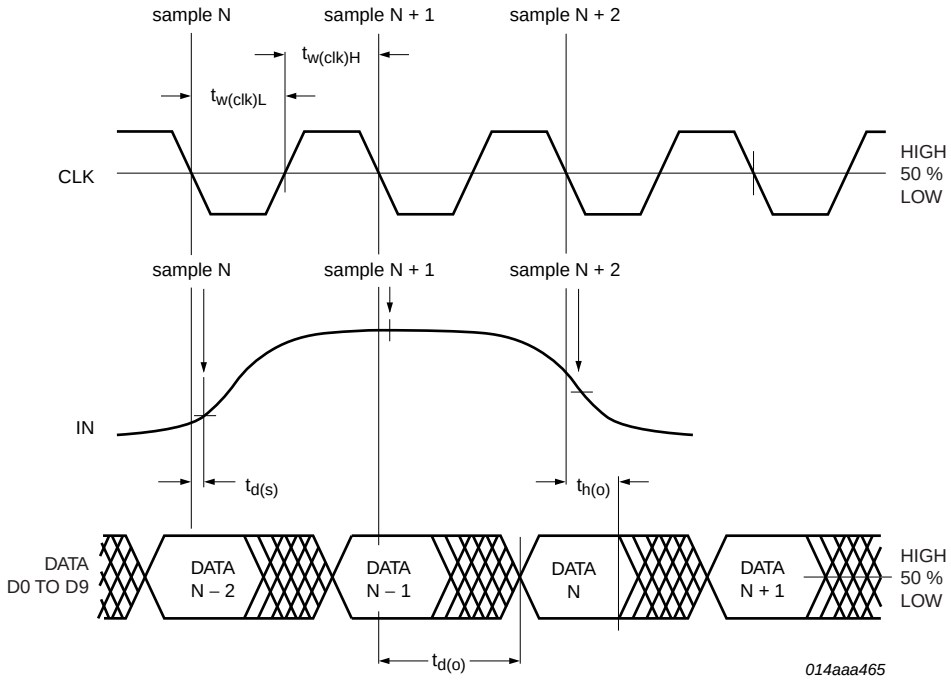
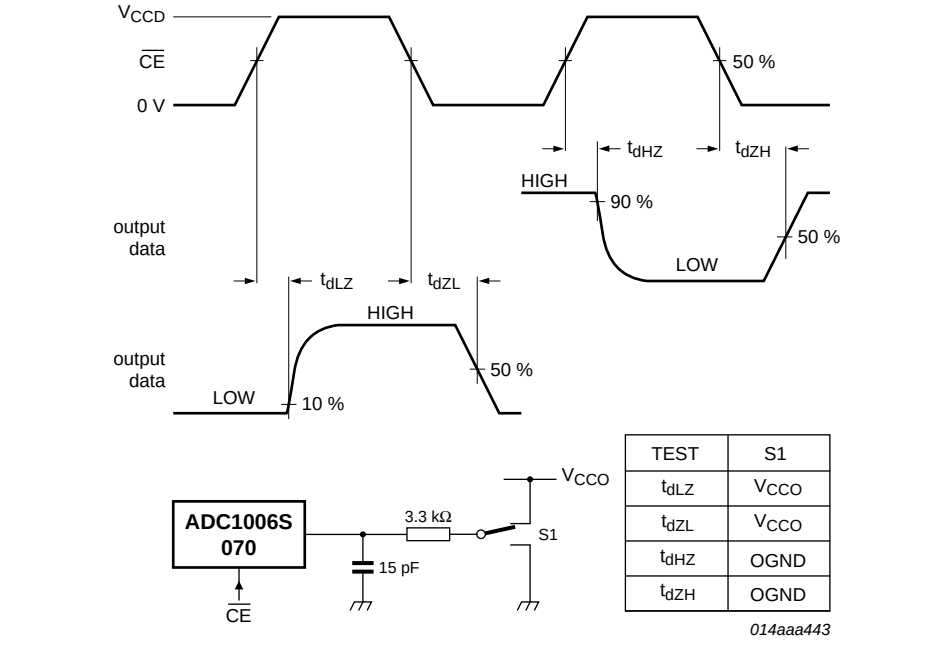
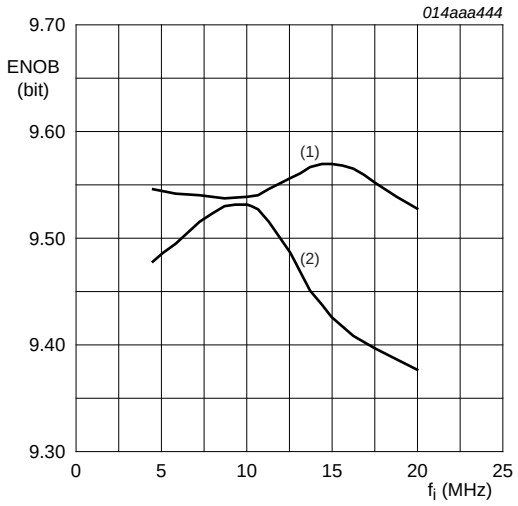


Fig 3. Timing diagram



(1) frequency on pin $\overline{CE}$ = 100 kHz.

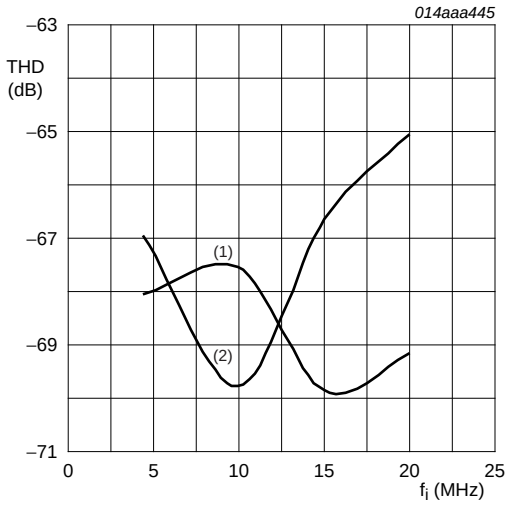
Fig 4. Timing diagram and test conditions of 3-state output delay time



(1) 55 MHz.

(2) 70 MHz.

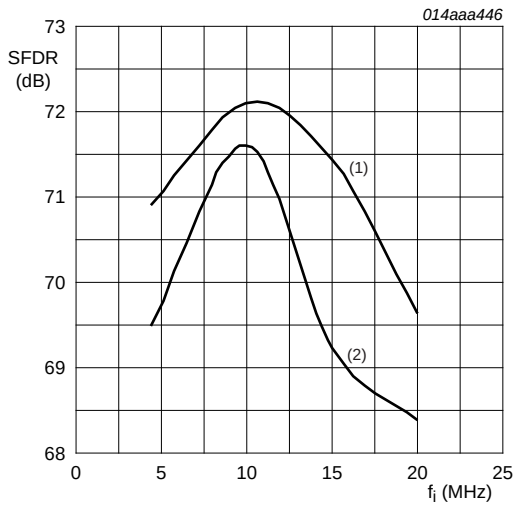
Fig 5. Effective Number Of Bits (ENOB) as a function of input frequency (sample device)



(1) 55 MHz.

(2) 70 MHz.

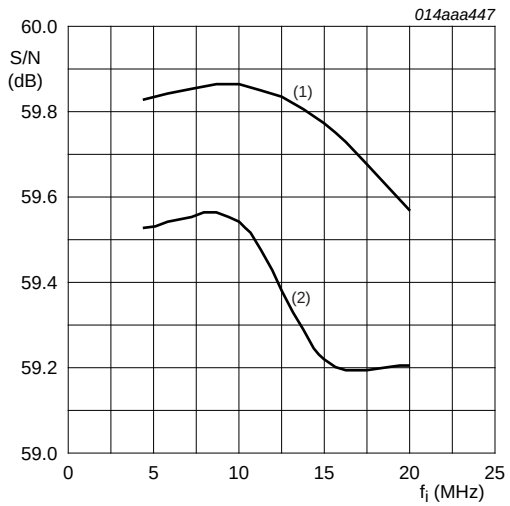
Fig 6. Total Harmonic Distortion (THD) as a function of input frequency (sample device)



(1) 55 MHz.

(2) 70 MHz.

Fig 7. Spurious Free Dynamic Range (SFDR) as a function of input frequency (sample device)



(1) 55 MHz.

(2) 70 MHz.

Fig 8. Signal-to-Noise Ratio (S/N) as a function of input frequency (sample device)

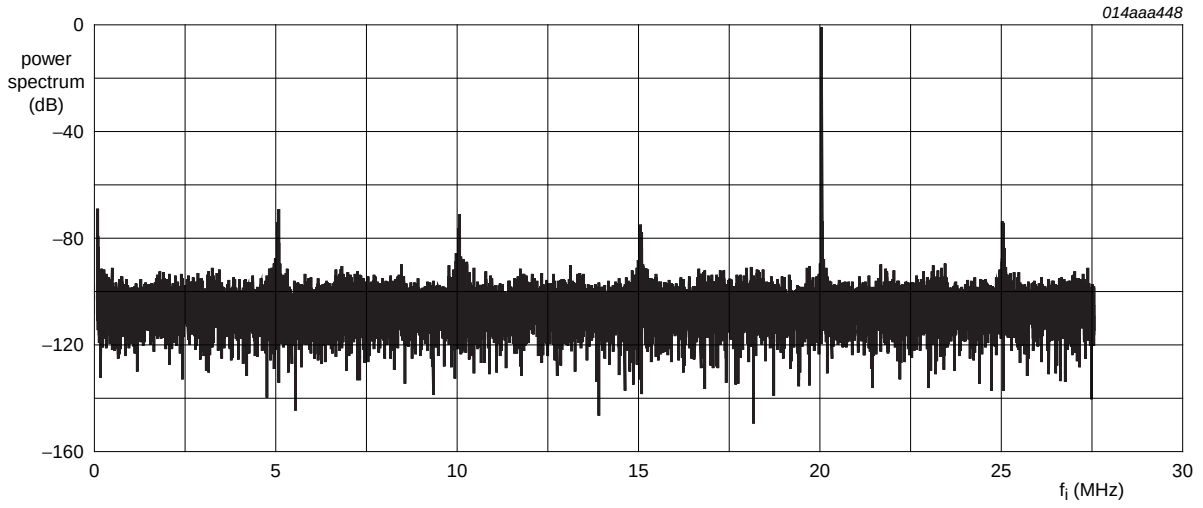


Fig 9. Single-tone; f_i = 20 MHz; f_{clk} = 55 MHz

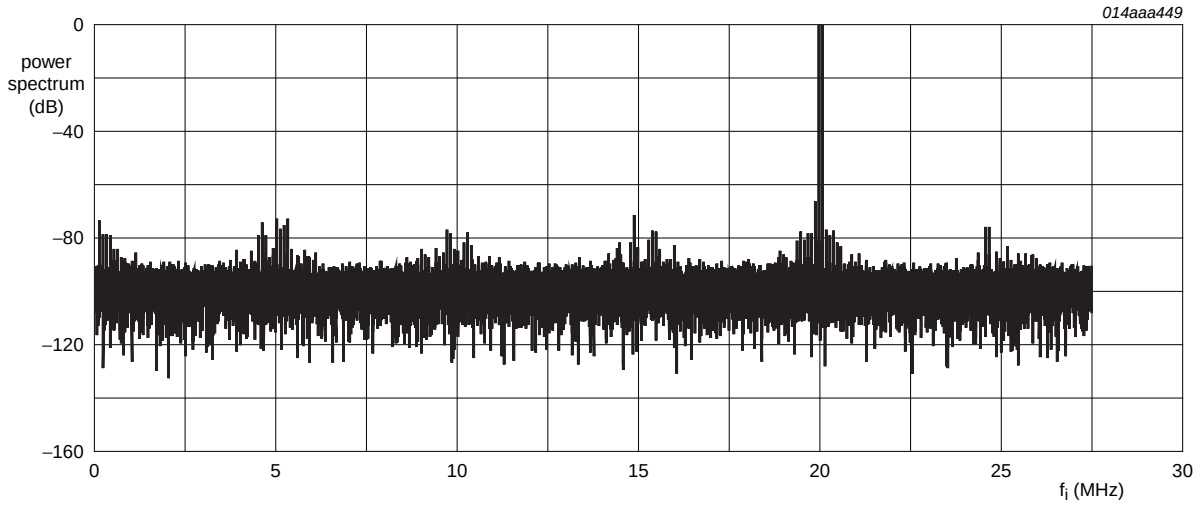


Fig 10. Two-tone; f_i 1 = 20 MHz; f_i 2 = 20.1 MHz; f_{clk} = 55 MHz

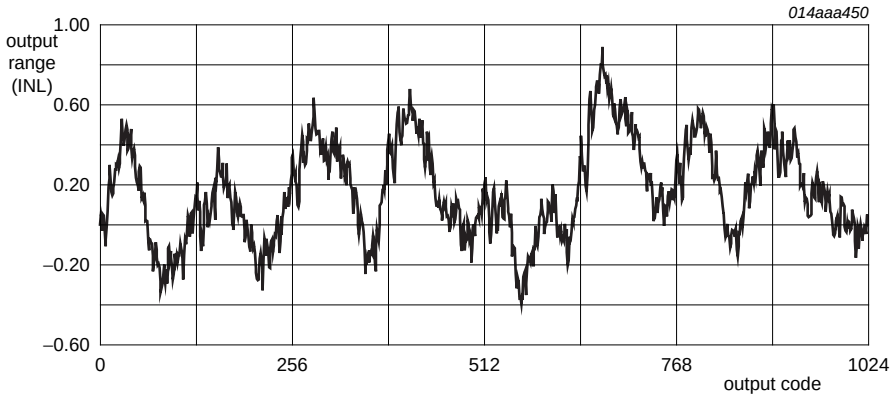


Fig 11. Integral Non-Linearity (INL)

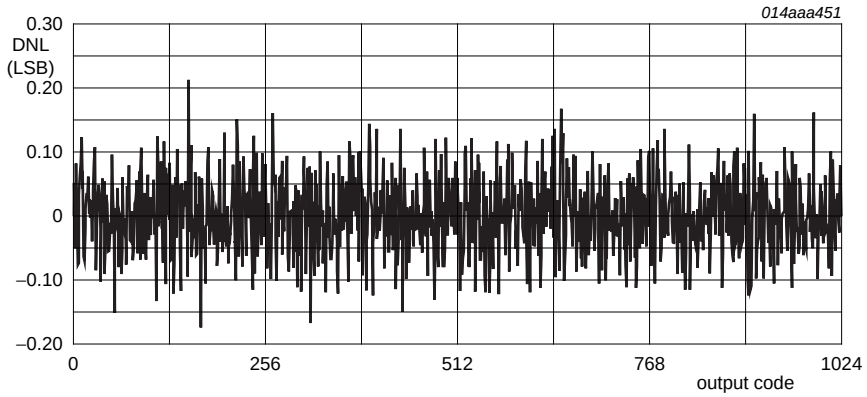
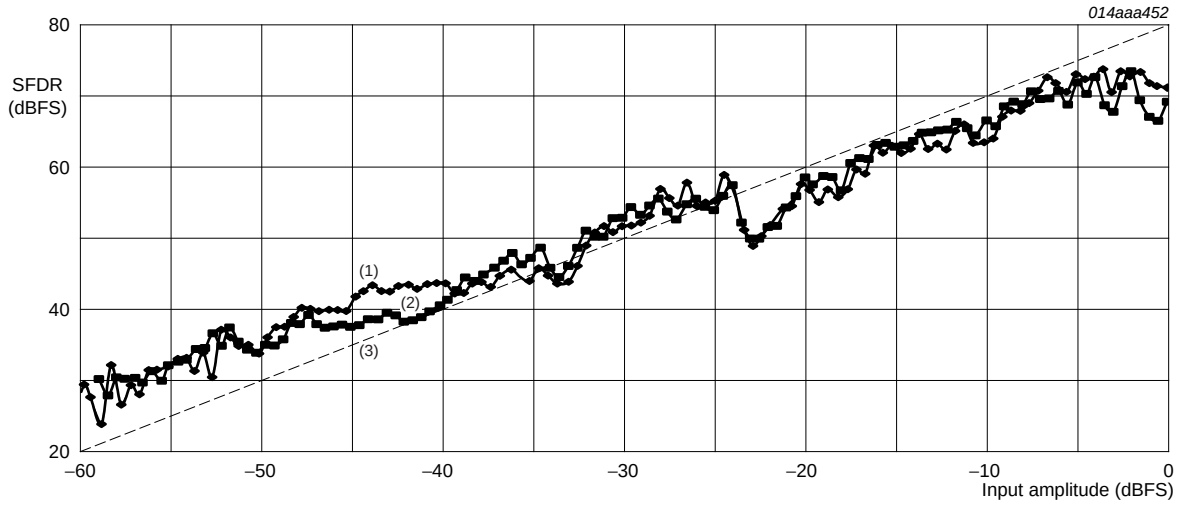


Fig 12. Differential Non-Linearity (DNL)

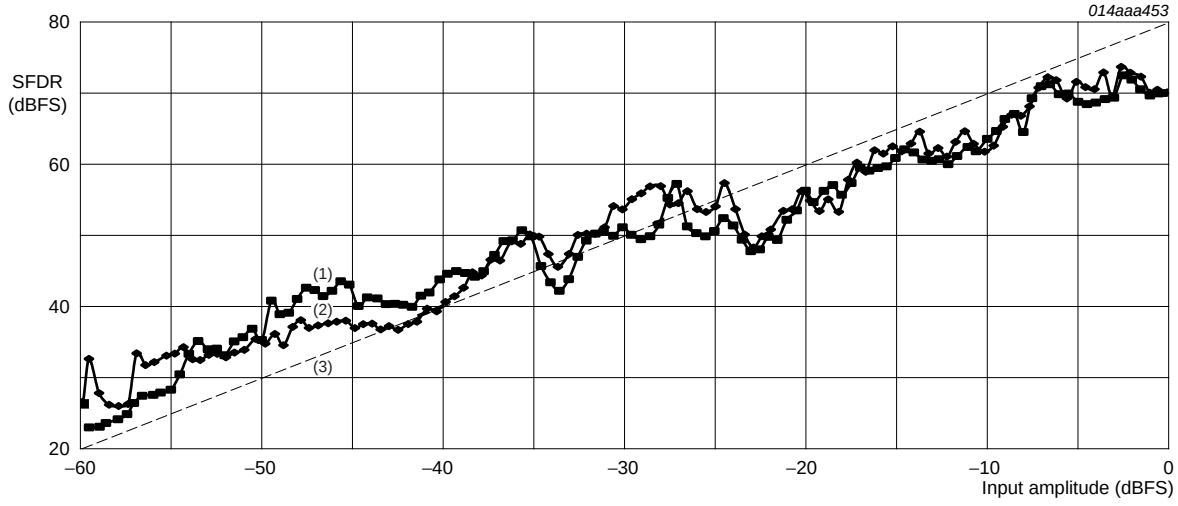


(1) f_i = 4.43 MHz.

(2) f_i = 20 MHz.

(3) SFDR = 80 dB.

Fig 13. SFDR as a function of input amplitude; $V_{i(IN)(p-p)} - V_{i(INN)(p-p)}$ = 1.9 V; f_{clk} = 40 MHz

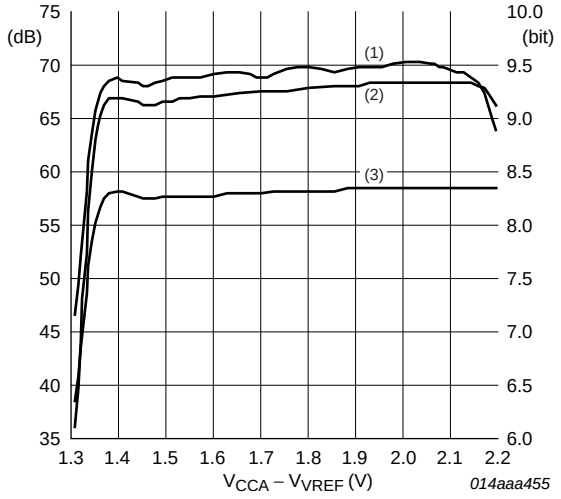


(1) f_i = 4.43 MHz.

(2) f_i = 20 MHz.

(3) SFDR = 80 dB.

Fig 14. SFDR as a function of input amplitude; $V_{i(IN)(p-p)} - V_{i(INN)(p-p)}$ = 1.9 V; f_{clk} = 55 MHz



(1) SFDR.

(2) ENOB.

(3) S/N.

Fig 15. SFDR, ENOB and S/N as a function of $V_{CCA} - V_{VREF}$; f_{clk} = 55 MHz; f_i = 20 MHz

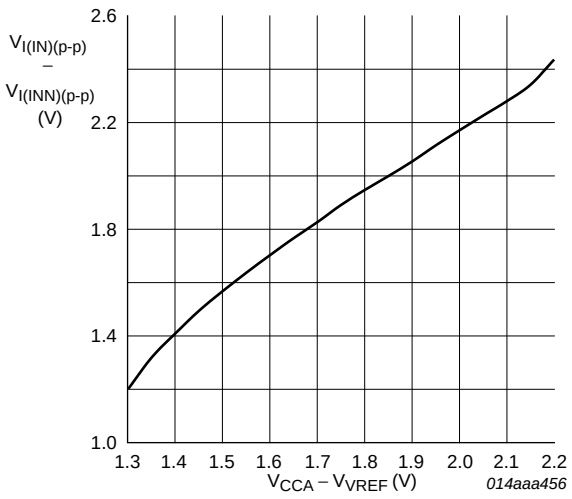
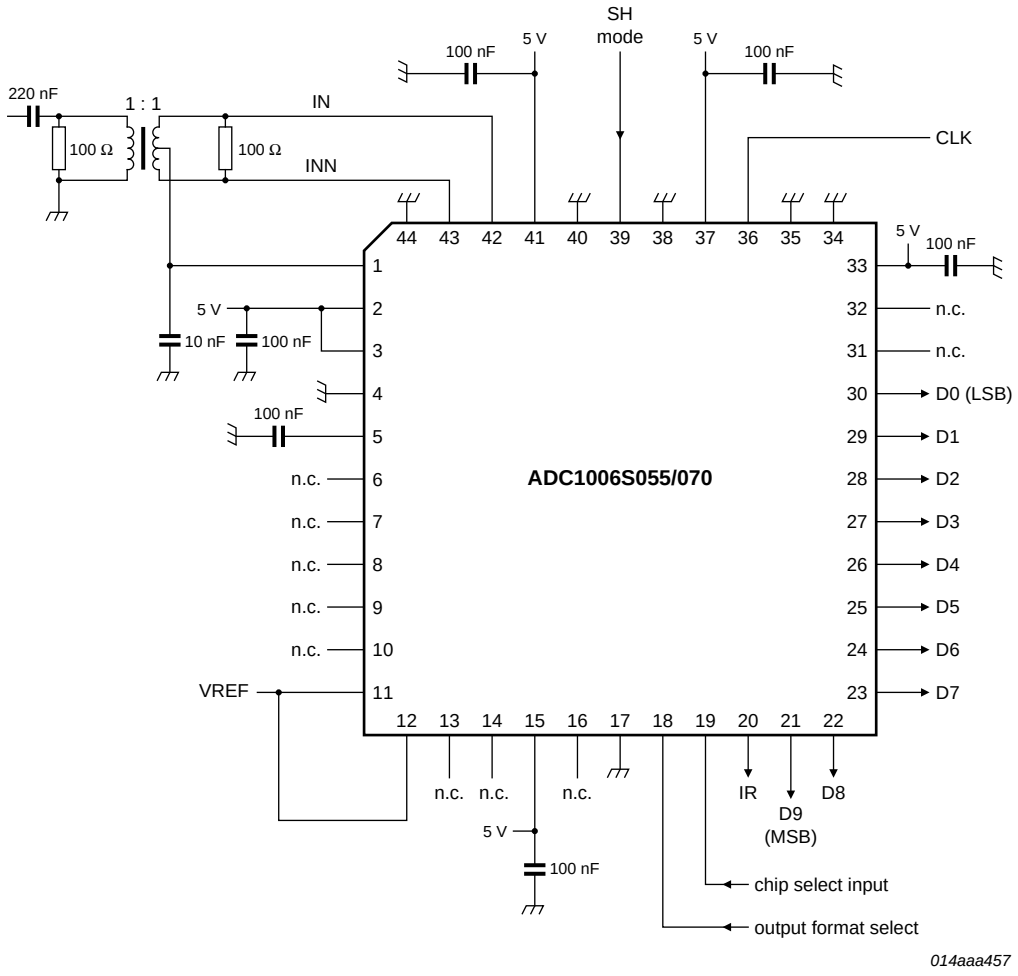


Fig 16. ADC full-scale; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ as a function of $V_{CCA} - V_{VREF}$

12. Application information

12.1 Application diagrams



The analog, digital and output supplies should be separated and decoupled.

Fig 17. Application diagram

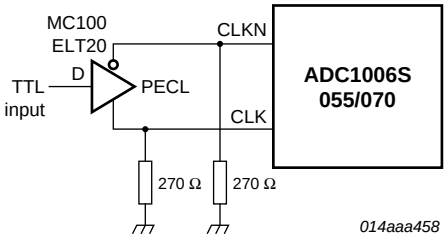


Fig 18. Application diagram for differential clock input PECL compatible using a TTL to PECL translator

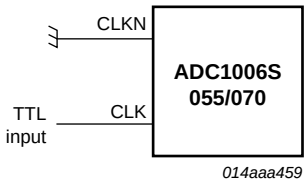
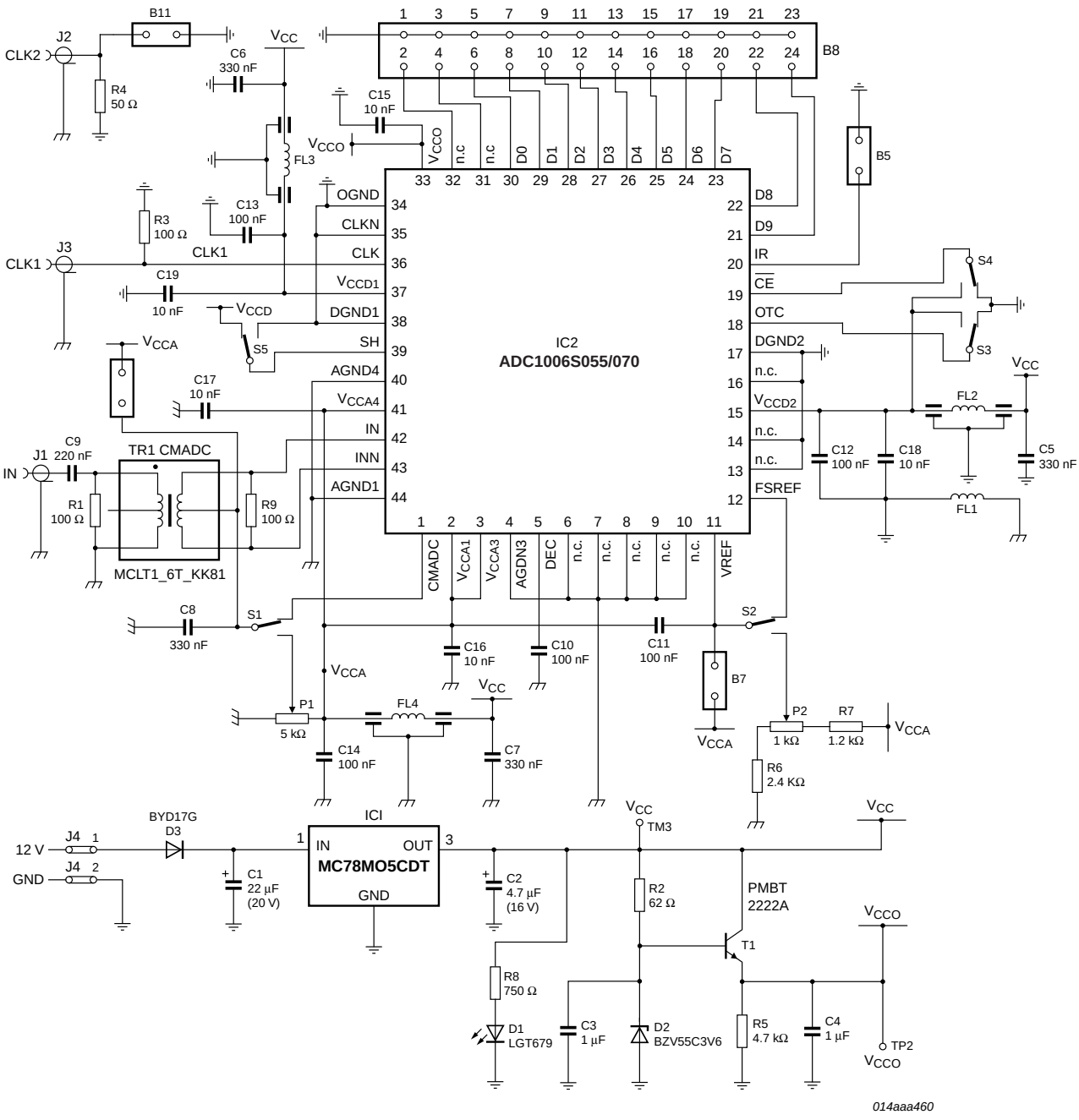


Fig 19. Application diagram for TTL single-ended clock

12.2 Demonstration board



C8 is close to TR1 pin.

Fig 20. Demonstration board schematic

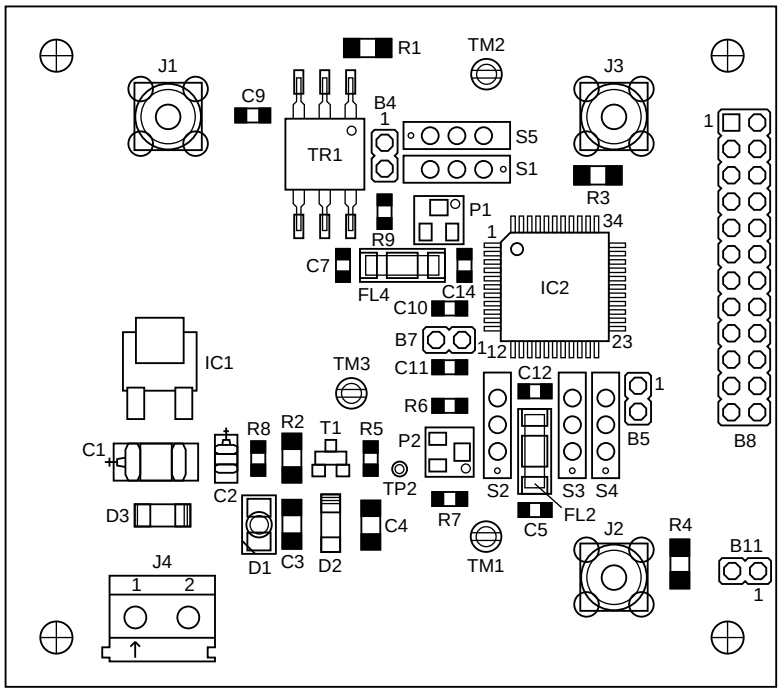


Fig 21. Component placement (top side)

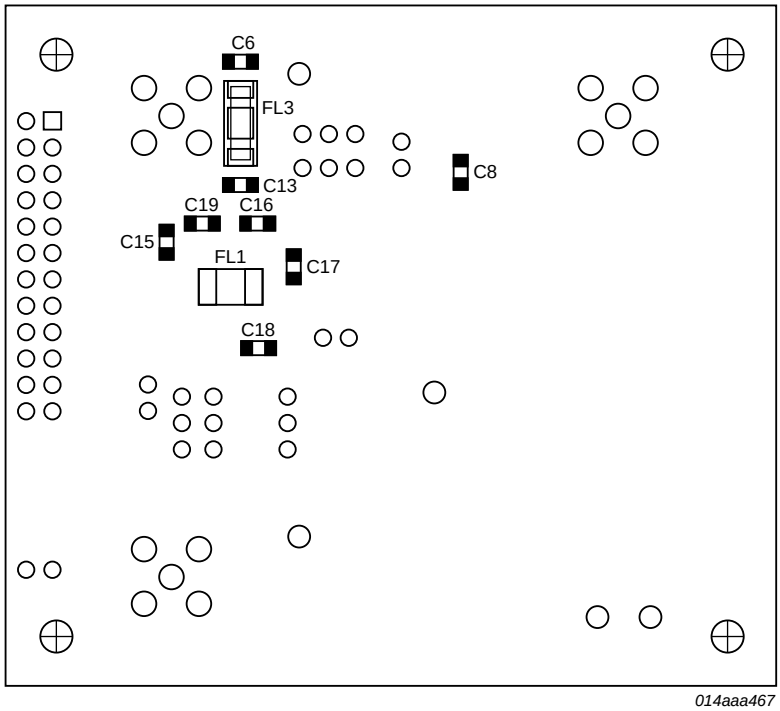


Fig 22. Component placement (underside)

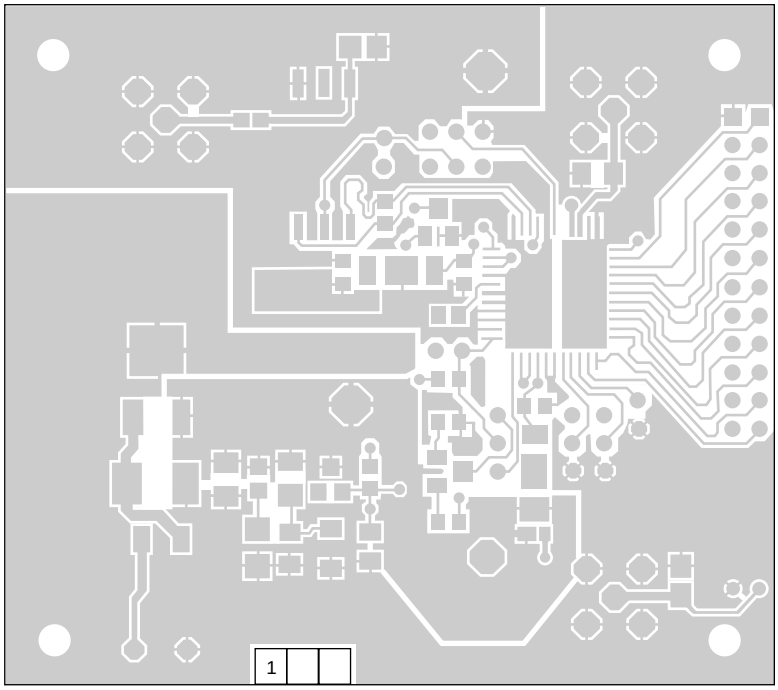


Fig 23. Printed-circuit board layout (top layer)

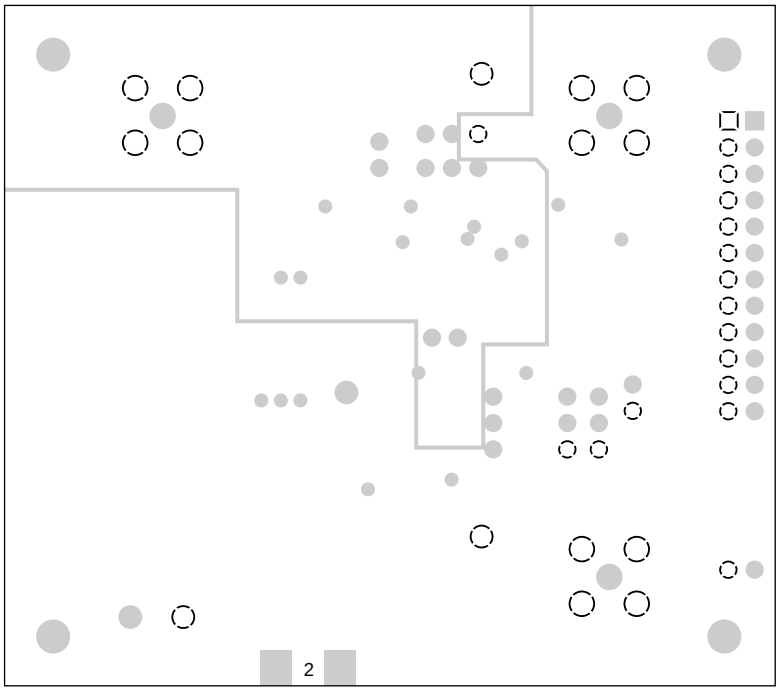


Fig 24. Printed-circuit board layout (ground layer)

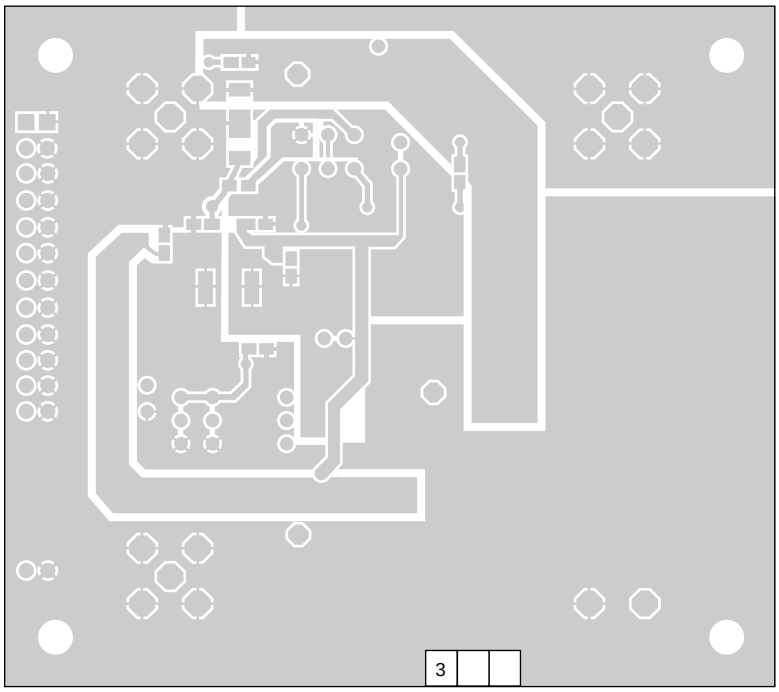


Fig 25. Printed-circuit board layout (power plane)

12.3 Alternative parts

The following alternative parts are also available:

Table 10. Alternative parts

Type number	Description		Sampling frequency
ADC1206S040	Single 12 bits ADC	[1]	40 MHz
ADC1206S055	Single 12 bits ADC	[1]	55 MHz
ADC1206S070	Single 12 bits ADC	[1]	70 MHz

[1] Pin to pin compatible

12.4 Recommended companion chip

The recommended companion chip is the TDA9901 wideband differential digital controlled variable gain amplifier.

13. Support information

13.1 Definitions

13.1.1 Non-linearities

13.1.1.1 Integral Non-Linearity (INL)

It is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of the code i is obtained from the equation:

$$INL(i) = \frac{V_I(i) - V_I(ideal)}{S} \quad (1)$$

where $i = 0 \cdot (2^n - 1)$ and

S = slope of the ideal straight line = code width; i = code value.

13.1.1.2 Differential Non-Linearity (DNL)

It is the deviation in code width from the value of 1 LSB.

$$DNL(i) = \frac{V_I(i+1) - V_I(i)}{S} - 1 \quad (2)$$

where $i = 0 \cdot (2^n - 2)$

13.1.2 Dynamic parameters (single tone)

Figure 26 shows the spectrum of a full-scale input sine wave with frequency f_t, conforming to coherent sampling (f_t / f_s = M / N, where M is the number of cycles and N is number of samples, M and N being relatively prime), and digitized by the ADC under test.

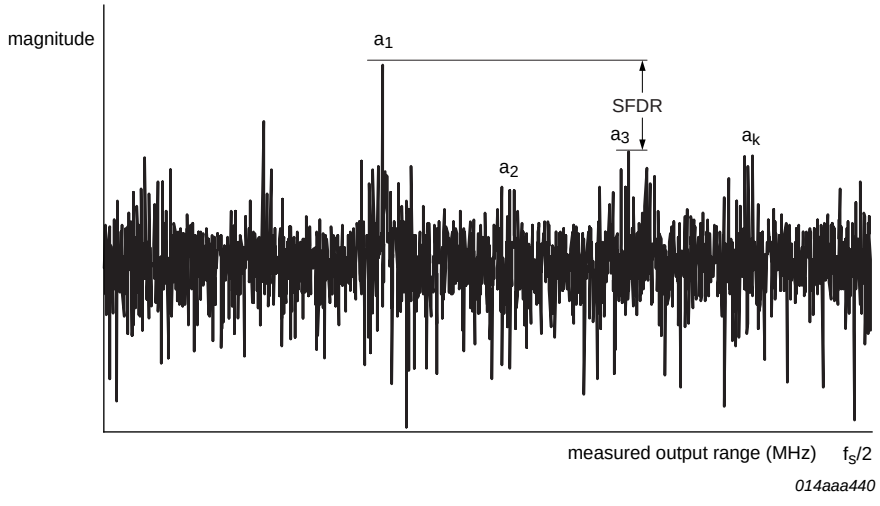


Fig 26. Spectrum of full-scale input sine wave with frequency f_t

Remark: In the following equations, P_{noise} is the power of the terms which include the effects of random noise, non-linearities, sampling time errors, and 'quantization noise'.

13.1.2.1 Signal-to-Noise And Distortion (SINAD)

The ratio of the output signal power to the noise and distortion power for a given sample rate and input frequency, excluding the DC component:

$$SINAD\ [dB] = 10\ log\left[\frac{P_{signal}}{P_{noise+distortion}}\right] \quad (3)$$

13.1.2.2 Effective Number Of Bits (ENOB)

It is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$ENOB = (SINAD\ [dB] - (1.76))/(6.02)$$

13.1.2.3 Total Harmonic Distortion (THD)

The ratio of the power of the harmonics to the power of the fundamental. For k-1 harmonics the THD is:

$$THD\ [dB] = 10\ log\left[\frac{P_{harmonics}}{P_{signal}}\right] \quad (4)$$

where $P_{harmonics} = \alpha|_2^2 + \alpha|_3^2 + \alpha|_k^2$ and $P_{signal} = \alpha|_1^2$

The value of k is usually 6 (i.e. calculation of THD is done on the first 5 harmonics).

13.1.2.4 Signal-to-Noise ratio (S/N)

The ratio of the output signal power to the noise power, excluding the harmonics and the DC component.

$$\text{S/N}\ [dB] = 10\ log\left[\frac{P_{signal}}{P_{noise}}\right] \quad (5)$$

13.1.2.5 Spurious Free Dynamic Range (SFDR)

The number SFDR specifies available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious (harmonic and non-harmonic), excluding DC component.

$$SFDR\ [dB] = 20\ log\frac{\alpha_1}{max(s)} \quad (6)$$

13.1.3 Intermodulation distortion

13.1.3.1 Spectral analysis (dual-tone)

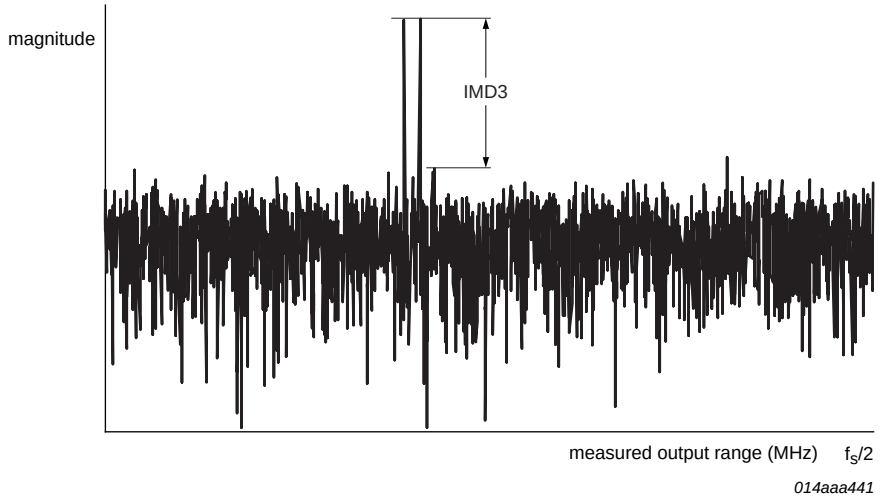


Fig 27. Spectral analysis (dual-tone)

From a dual-tone input sinusoid (f_{t1} and f_{t2}, these frequencies being chosen according to the coherence criterion), the intermodulation distortion products IMD2 and IMD3 (respectively, 2nd and 3rd-order components) are defined, as follows.

13.1.3.2 IMD2 (IMD3)

The ratio of the RMS value of either tone to the RMS value of the worst second (third) order intermodulation product.

The total IMD is given by:

$$IMD\ [dB] = 10\ log\left[\frac{P_{intermod}}{P_{signal}}\right]$$

where,

$$P_{intermod} = a|^2_{im}(f_{t1} - f_{t2}) - a|^2_{im}(f_{t1} + f_{t2}) + a|^2_{im}(f_{t1} - 2f_{t2}) + a|^2_{im}(f_{t1} + 2f_{t2}) + a|^2_{im}(2f_{t1} - f_{t2}) + a|^2_{im}(2f_{t1} + f_{t2})$$

$P_{signal} = a^2(f_{t1}) + a^2(f_{t2})$ and

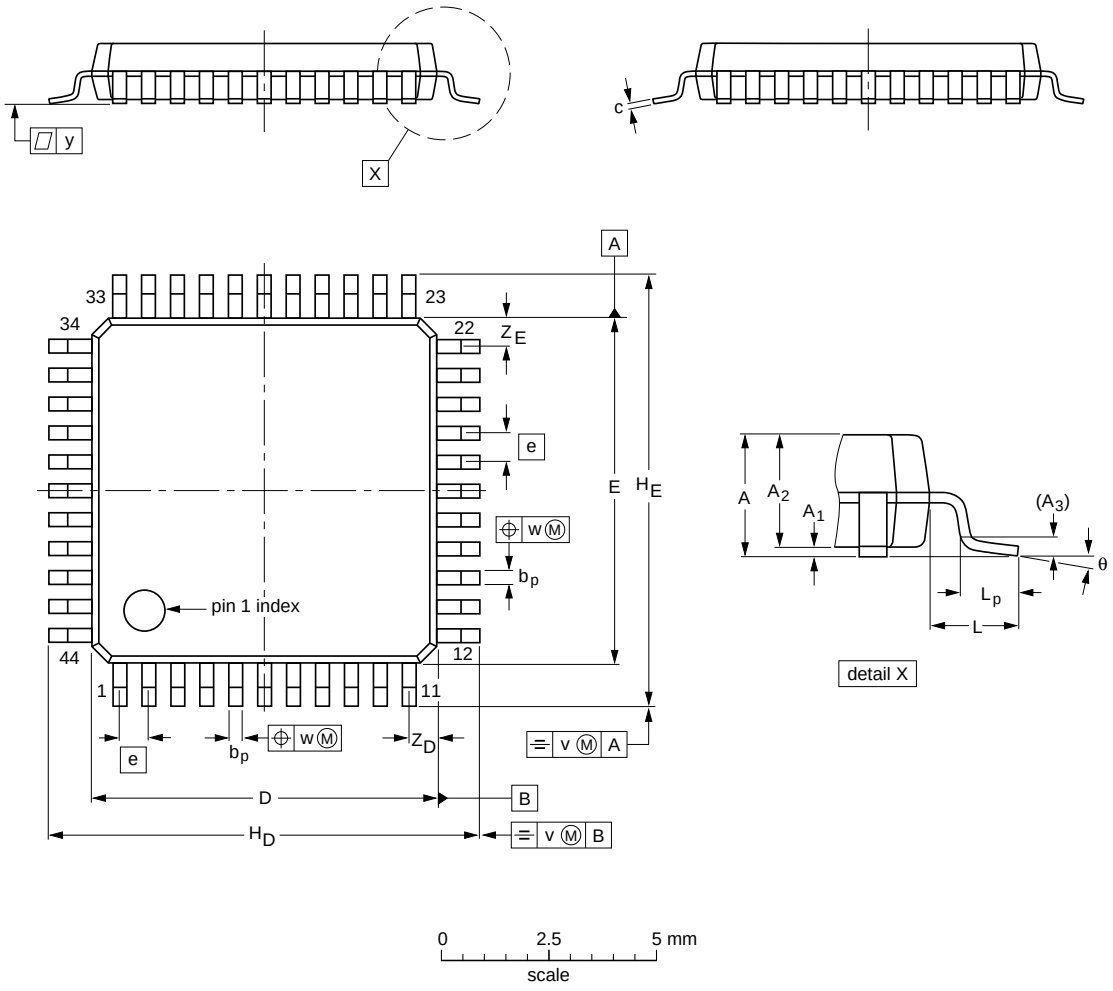
$a|^2_{im}(f_t)$ is the power in the intermodulation component at frequency f_t.

13.1.4 Noise Power Ratio (NPR)

When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the NPR is defined as the ratio of the average out-of-notch to the in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample set.

14. Package outline

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.1	0.25 0.05	1.85 1.65	0.25	0.4 0.2	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT307-2						~~97-08-01~~ 03-02-25

Fig 28. Package outline SOT307-2 (QFP44)

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1006S055_070_3	20120702	Product data sheet	-	ADC1006S055_070_2
ADC1006S055_070_2	20080812	Product data sheet	-	ADC1006S055_070_1
Modifications:	• Corrections made to titles in Figure 13 and 14. • Corrections made to note in Figure 4.			
ADC1006S055_070_1	20080611	Product data sheet	-	-

16. Contact information

For more information or sales office addresses, please visit: http://www.idt.com

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