Li+ Charger Protection IC

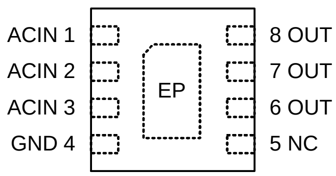
Features

- Input Over-Voltage Protection
- Over-Temperature Protection
- High Immunity of False Triggering
- High Accuracy Protection Thresholds
- Available in TDFN2x2-8 Package
- Lead Free and Green Devices Available (RoHS Compliant)
- Compliance to IEC61000-4-2 (Level 4)
  ±8kV (Contact Discharge)
  ±15kV (Air Discharge)

Applications

- Smart Phones and PDAs
- Digital Still Cameras
- Portable Devices

Pin Configuration

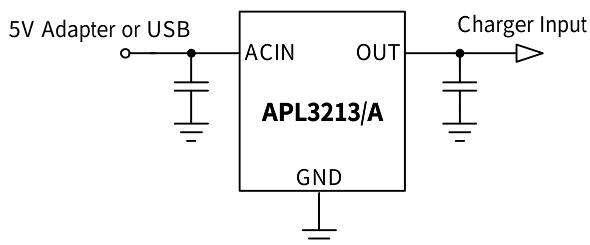


TDFN2x2-8
(Top View)

General Description

The APL3213/A provide Li+ charger protection against over-voltage. The IC is designed to monitor input voltage. When input voltage is over the threshold, the IC removes the power from the charging system by turning off an internal switch. The protection also have deglitch time against false triggering due to voltage spikes. The APL3213/A also provide Power-On-Reset (POR) function and over-temperature protection. The Power-On-Reset circuit monitors supply voltages to prevent wrong operations. The over-temperature protection limits the junction temperature below 140°C in case of short circuit or overload conditions.

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL3213/A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN2x2-8 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3213 QB: 3213 X	X - Date Code
APL3213A QB: 213A X	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{ACIN}	ACIN Input Voltage (ACIN pin to GND)	-0.3 to 20	V
V_{OUT}	OUT, Pin to GND Voltage	-0.3 to 7	V
I_{OUT}	OUT Output Current	2	A
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature,10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance in Free Air (Note 2) TDFN2x2-8	75	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{ACIN}	ACIN Input Voltage	APL3213	4.5 to 5.5	V
		APL3213A	4.5 to 5.25	V
I_{OUT}	OUT Output Current		0 to 1.5	A
T_J	Junction Temperature		-40 to 125	°C
T_A	Ambient Temperature		-40 to 85	°C

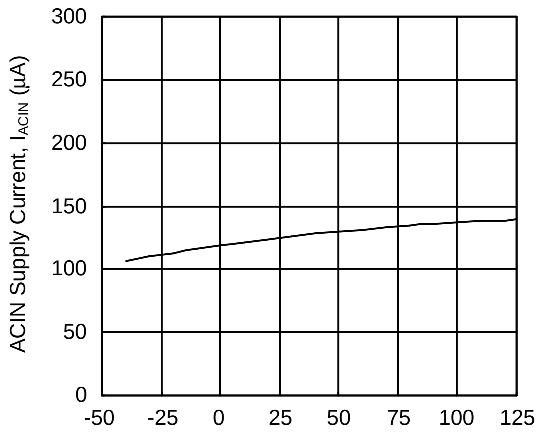
Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{ACIN}=5V, T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

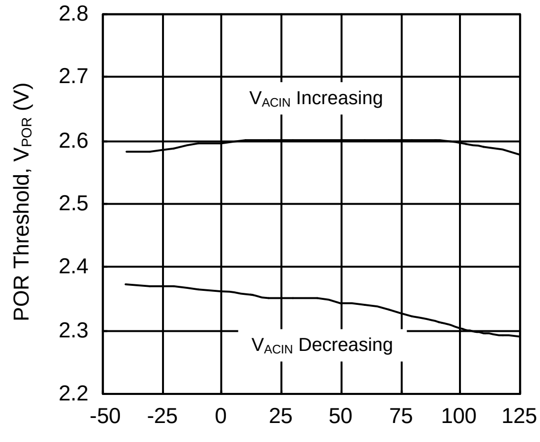
Symbol	Parameter	Test Conditions	APL3213/A			Unit
			Min.	Typ.	Max.	
POWER-ON-RESET (POR) AND SUPPLY CURRENT						
V_{POR}	ACIN POR Threshold	V_{ACIN} rising	2.4	-	2.8	V
	ACIN POR Hysteresis		-	250	-	mV
I_{CC}	ACIN Supply Current		-	125	300	μA
$T_{B(ACIN)}$	Input Power-On Blanking Time	V_{ACIN} rising to V_{OUT} rising	-	8	-	ms
INTERNAL POWER SWITCH AND OUT DISCHARGE RESISTANCE						
	Power Switch On Resistance	I_{OUT} = 0.6A	-	130	-	mΩ
	OUT Discharge Resistance	V_{OUT} = 3V	-	500	-	Ω
INPUT OVER-VOLTAGE PROTECTION (OVP)						
V_{OVP}	Input OVP Threshold	V_{ACIN} rising, APL3213	5.70	5.85	6.00	V
		V_{ACIN} rising, APL3213A, T_A=25°C	5.285	5.33	5.38	V
		V_{ACIN} rising, APL3213A, T_A = -20~60°C	5.28	5.33	5.4	V
	Input OVP Recovery Hysteresis		150	250	350	mV
	Input OVP Propagation Delay		-	1	-	μs
$T_{ON(OVP)}$	Input OVP Recovery Time		-	8	-	ms
OVER-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold		-	140	-	°C
	Over-Temperature Hysteresis		-	20	-	°C

Typical Operating Characteristics

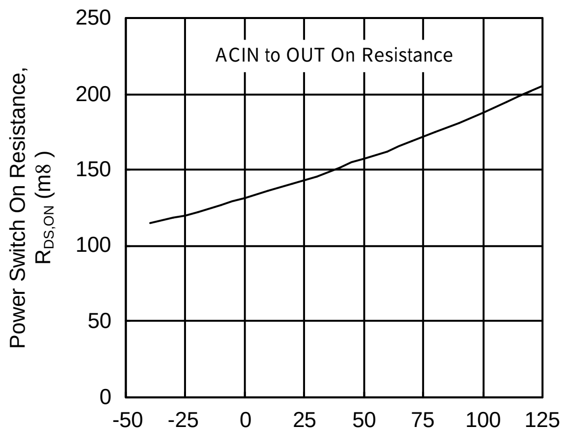
ACIN Supply Current vs. Junction Temperature



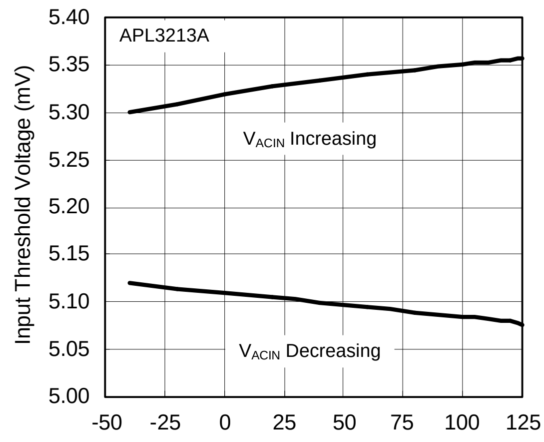
POR Threshold vs. Junction Temperature



Power Switch On Resistance vs. Junction Temperature



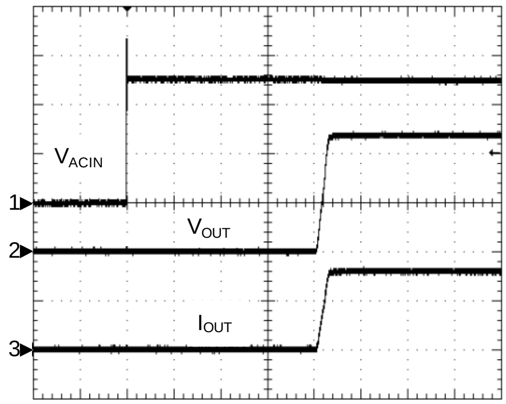
Input OVP Threshold vs. Junction Temperature



Operating Waveforms

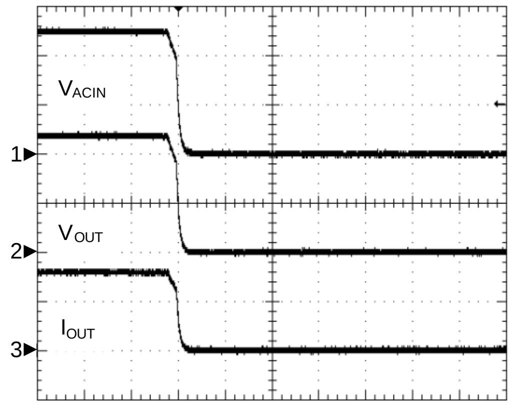
Refer to the typical application circuit. The test condition is V_{ACIN}= 5V, C_{ACIN}= 1µF, C_{OUT}=1µF, T_A= 25°C unless otherwise specified.

Normal Power On



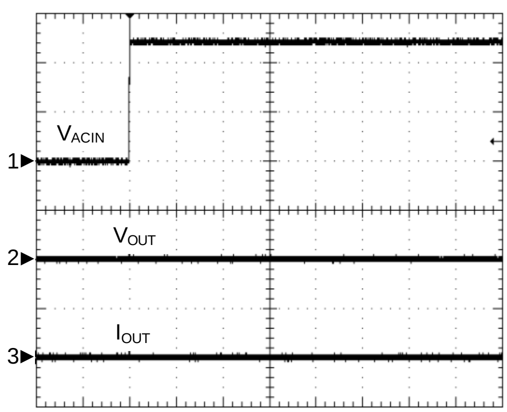
R_{OUT}=3Ω
CH1: V_{ACIN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2ms/Div

Normal Power Off



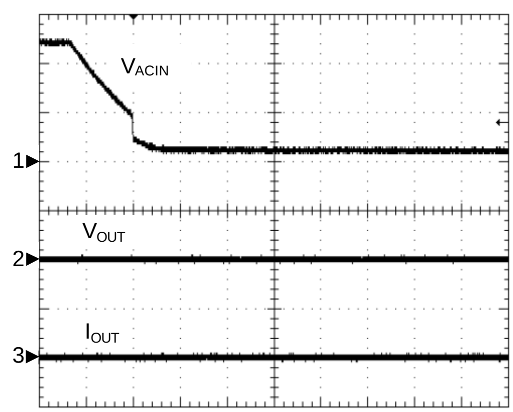
R_{OUT}= 3Ω
CH1: V_{ACIN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 100µs/Div

OVP at Power On



V_{ACIN}= 0 to 12V
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2ms/Div

OVP at Power Off



V_{ACIN}= 12 to 0V
CH1: V_{DD}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 40ms/Div

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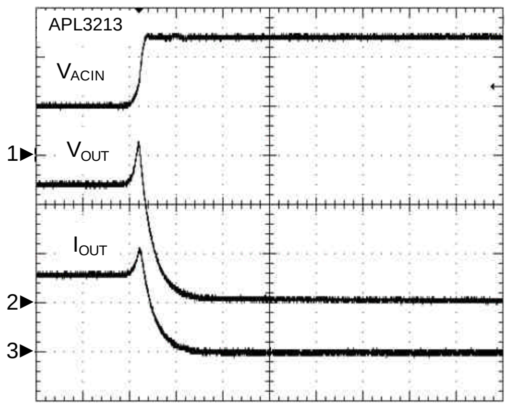
Operating Waveforms

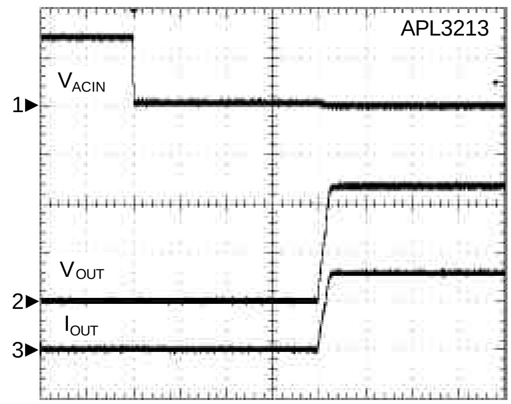
Refer to the typical application circuit. The test condition is V_{ACIN}= 5V, C_{ACIN}= 1μF, C_{OUT}=1μF, T_A= 25°C unless otherwise specified.

Input Over-Voltage Protection



V_{ACIN} = 5 to 12V, R_{OUT} = 3Ω
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{CHRIN}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 10μs/Div

Recovery from Input OVP

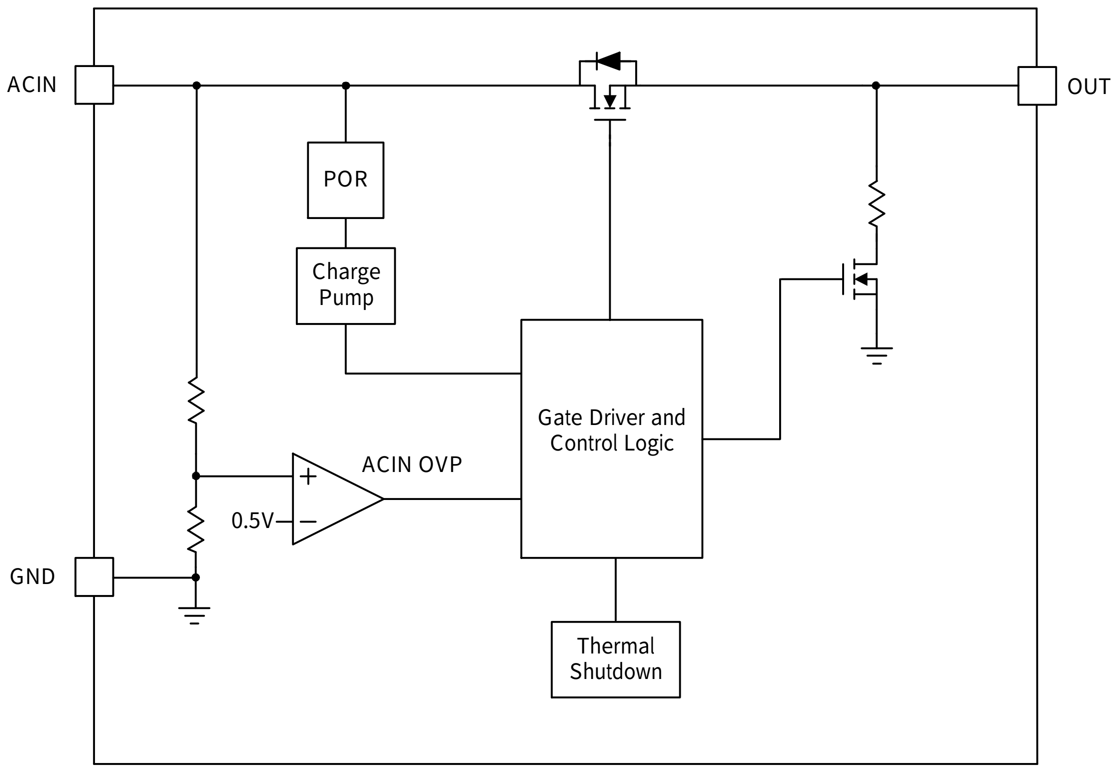


V_{ACIN}= 12 to 5V, R_{OUT} = 3Ω
CH1: V_{ACIN}, 5V/Div, DC
CH2: V_{CHRIN}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2ms/Div

Pin Description

PIN		FUNCTION
NO.	NAME	
1, 2, 3	ACIN	Power Supply Input.
4	GND	Ground.
5	NC	No Connection.
6, 7, 8	OUT	Output Voltage Pin. The output voltage follows the input voltage when no fault is detected.
-	EP	Exposed Thermal Pad. Must be electrically connected to the GND pin.

Block Diagram



Typical Application Circuit

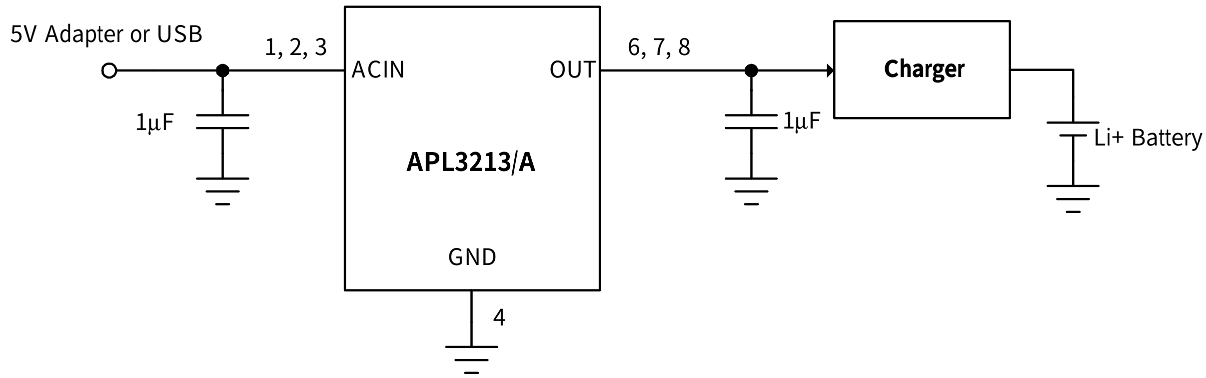


Figure 1. The Typical Protection Circuit for Charger Systems.

Function Description

Power-Up

The APL3213/A have a built-in power-on-reset circuit to keep the output shutting off until internal circuitry is operating properly. The POR circuit has hysteresis and a deglitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the POR threshold and after 8ms blanking time, the output voltage starts a soft-start to reduce the inrush current.

Input Over-Voltage Protection (OVP)

The input voltage is monitored by the internal OVP circuit. When the input voltage rises above the input OVP threshold, the internal FET will be turned off within 1μs to protect connected system on OUT pin. When the input voltage returns below the input OVP threshold minus the hysteresis, the FET is turned on again after 8ms recovery time. The input OVP circuit has a 200mV hysteresis and a recovery time of $T_{ON(OVP)}$ to provide noise immunity against transient conditions.

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over-temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

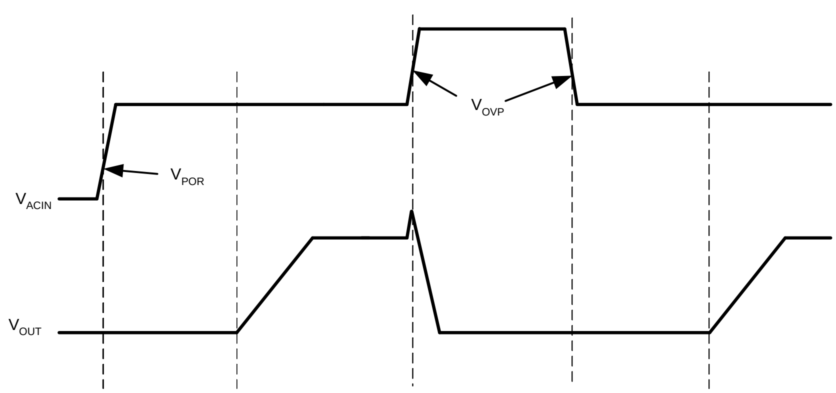


Figure 2. OVP Timing Chart

Application Information

Capacitor Selection

The input capacitor is for decoupling and prevents the input voltage from overshooting to dangerous levels. In the AC adapter hot plug-in applications or load current step-down transient, the input voltage has a transient spike due to the parasitic inductance of the input cable. A 25V, X5R, dielectric ceramic capacitor with a value between 1μF and 4.7μF placed close to the ACIN pin is recommended.

The output capacitor is for output voltage decoupling, and also the input capacitor of the charging circuit.

At least, a 1μF, 10V, X5R capacitor is recommended.

Layout Consideration

In some failure modes, a high voltage may be applied to the device. Make sure the clearance constraint of the PCB layout must satisfy the design rule for high voltage.

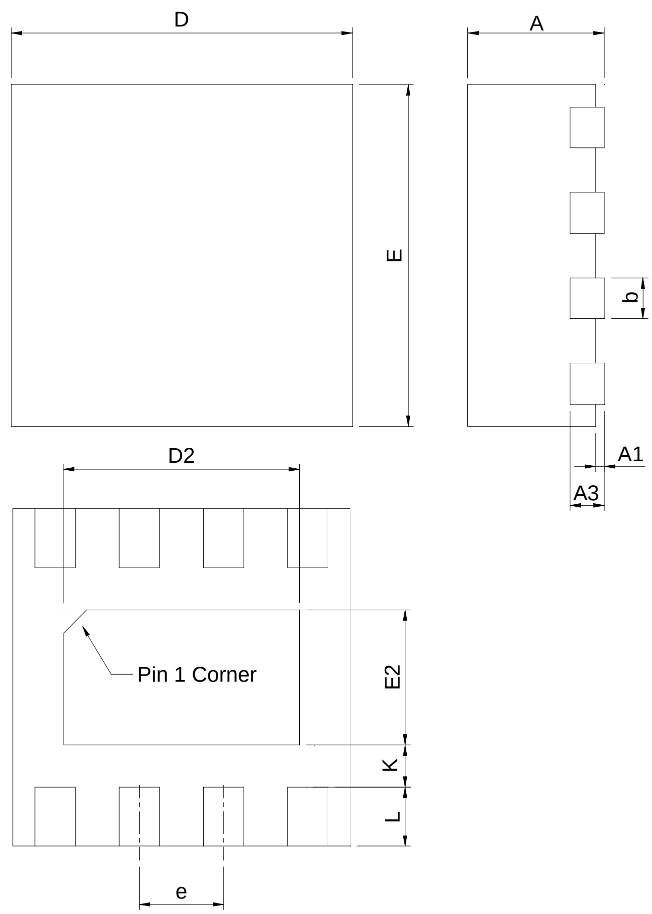
The exposed pad of the TDFN2x2-8 performs the function of channeling heat away. It is recommended that connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias to improve heat dissipation.

The input and output capacitors should be placed close to the IC.

The high current traces like input trace and output trace must be wide and short.

Package Information

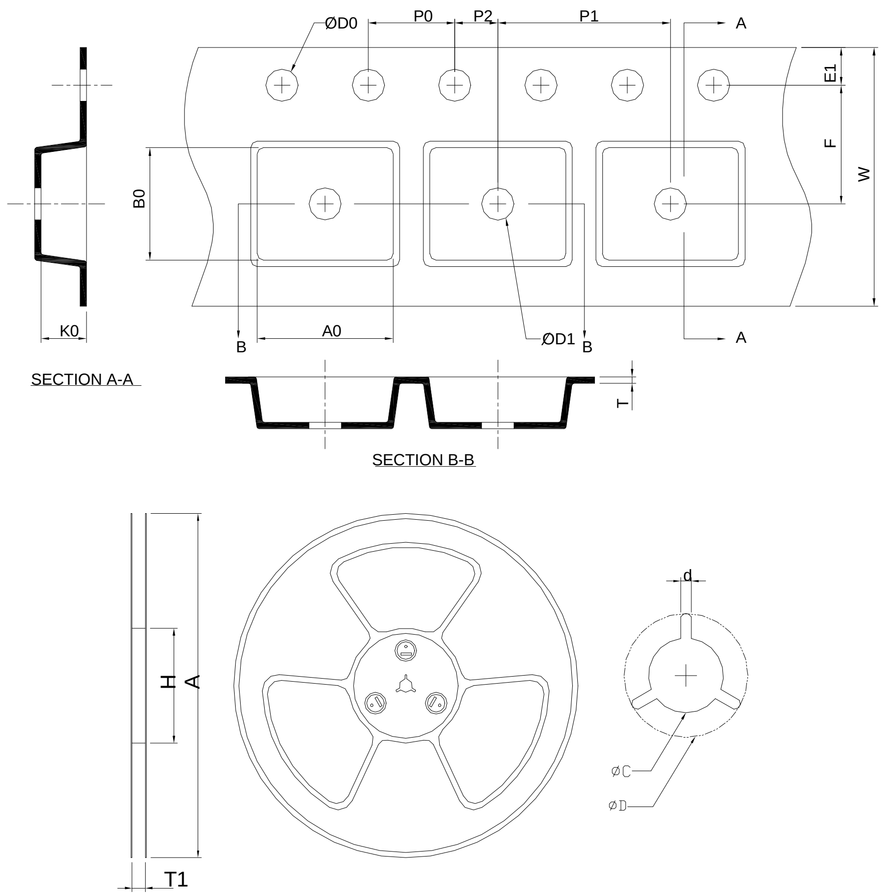
TDFN2x2-8



SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20

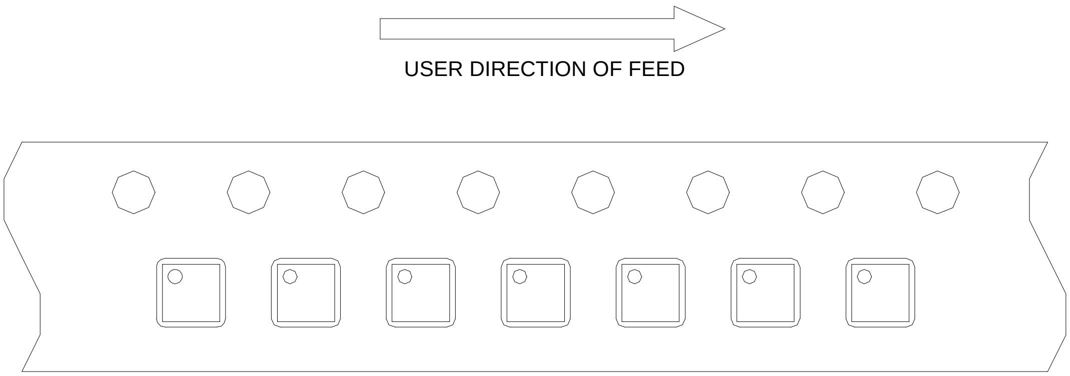
(mm)

Devices Per Unit

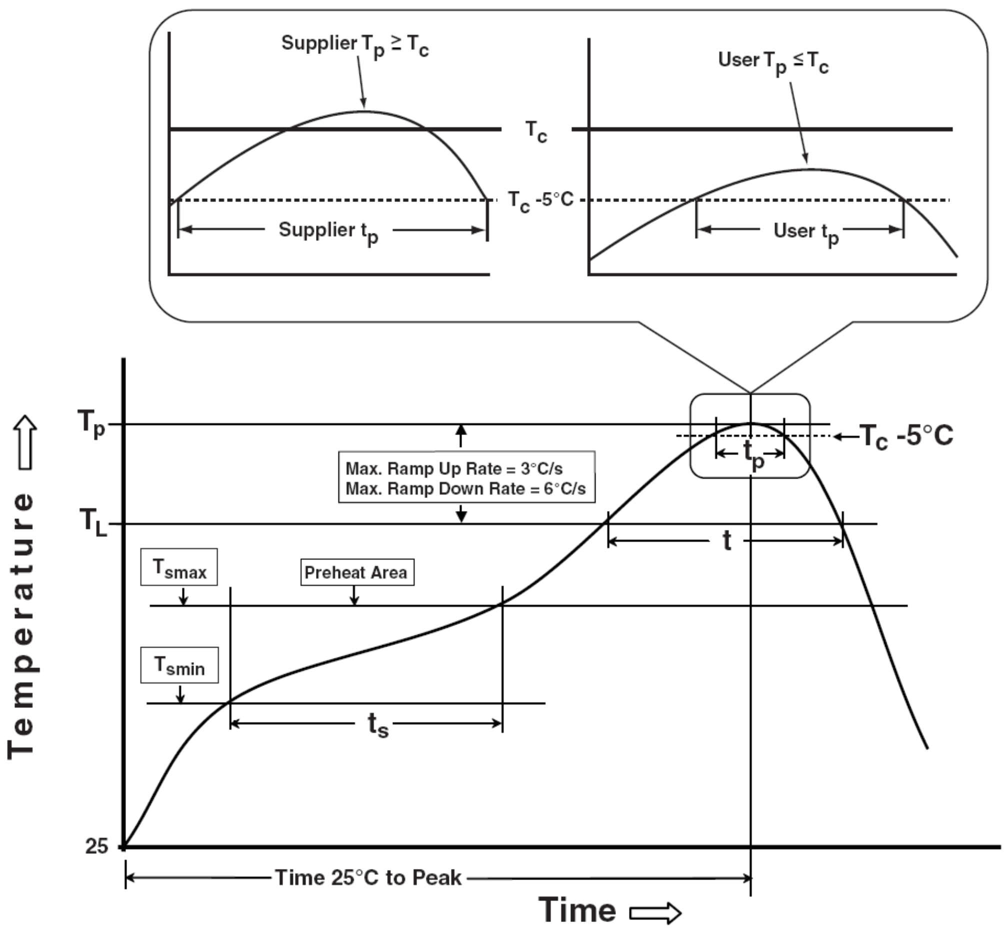
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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