N-Channel 80-V (D-S) MOSFET

Key Features:

- Low r_{DS(on)} trench technology
- · Low thermal impedance
- · Fast switching speed

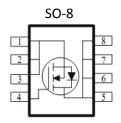
Typical Applications:

- · White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)}(m\Omega)$	I _D (A)	
80	36 @ V _{GS} = 10V	7.6	
	$43 @ V_{GS} = 4.5V$	7.0	







ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter		Symbo	ol Limit	Units	
Drain-Source Voltage			80	V	
Gate-Source Voltage	V_{GS}	±20	V		
Continuous Drain Course at 8	T _A =25		7.6		
Continuous Drain Current a	T _A =70)°C I _D	6.4	Α	
Pulsed Drain Current ^b	I _{DM}	50			
Continuous Source Current (Diode Conduction) a	I _S	4	Α		
Down Dissipation 8	T _A =25	5°C P _D	3.1	W	
Power Dissipation ^a	T _A =70)°C	2.2	V V	
Operating Junction and Storage Temperature Range		T_J, T_{st}	_a -55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	40	°C/W	
IMAXIMUM JUNCTION-TO-AMBIENT	Steady State	IΛθJA	80	C/VV	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Electrical Characteristics

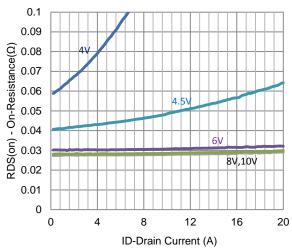
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$				V	
Gate-Body Leakage	I _{GSS}	1 2/ 02/2/ 002/			±100	nA	
Zero Gate Voltage Drain Current	1	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zelo Gate Voltage Dialii Current	I _{DSS}	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			25		
On-State Drain Current	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-Resistance	r	$V_{GS} = 10 \text{ V}, I_D = 6.1 \text{ A}$			36	mΩ	
Dialii-Source Off-Resistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 5.6 \text{ A}$			43		
Forward Transconductance	g _{fs}	$V_{DS} = 15 \text{ V}, I_D = 6.1 \text{ A}$		40		S	
Diode Forward Voltage	V_{SD}	$I_{S} = 2 \text{ A}, V_{GS} = 0 \text{ V}$		0.74		V	
	Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V},$		19		nC	
Gate-Source Charge	Q_gs	$V_{DS} = 40 \text{ V}, V_{GS} = 4.3 \text{ V},$ $I_{D} = 6.1 \text{ A}$		4.9			
Gate-Drain Charge	Q_gd	ID = 0.1 A		13			
Turn-On Delay Time	t _{d(on)}	$V_{DS} = 40 \text{ V}, R_1 = 6.6 \Omega,$		9			
Rise Time	t _r	$V_{DS} = 40 \text{ V}, \text{ K}_{L} = 0.0 \Omega,$ $I_{D} = 6.1 \text{ A},$		20		no	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 10 \text{ V}, R_{GEN} = 6 \Omega$		49		ns	
Fall Time	t _f	VGEN = 10 V, NGEN = 0 22		20			
Input Capacitance	C _{iss}			1318			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		147		pF	
Reverse Transfer Capacitance	C_{rss}			143			

Notes

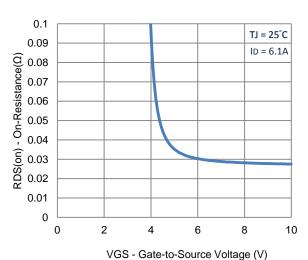
- Pulse test: PW <= 300us duty cycle <= 2%.
- Guaranteed by design, not subject to production testing. b.

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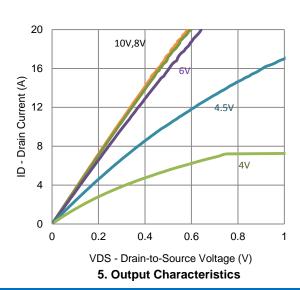
Typical Electrical Characteristics

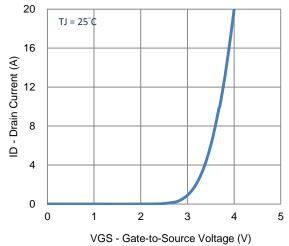


1. On-Resistance vs. Drain Current

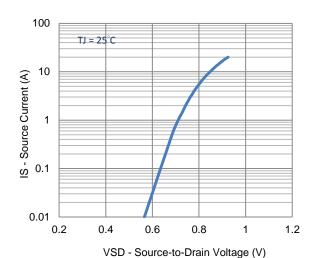


3. On-Resistance vs. Gate-to-Source Voltage

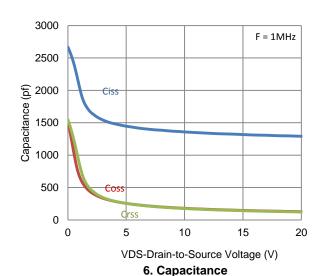




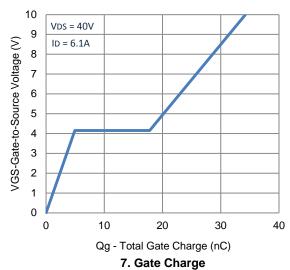
2. Transfer Characteristics

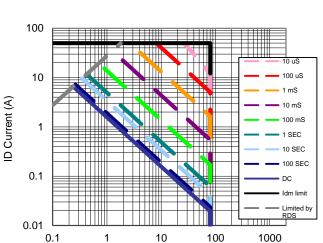


4. Drain-to-Source Forward Voltage



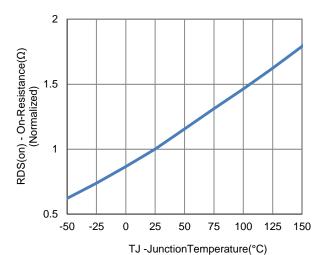
Typical Electrical Characteristics



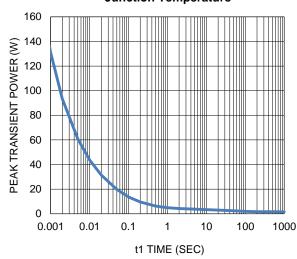


VDS Drain to Source Voltage (V)

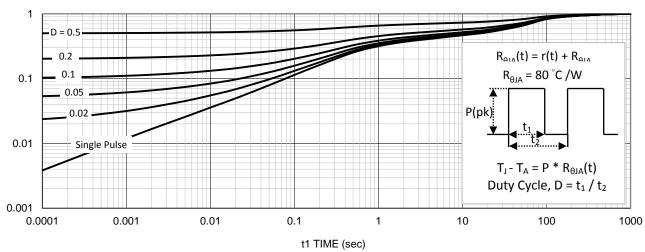
9. Safe Operating Area



8. Normalized On-Resistance Vs Junction Temperature



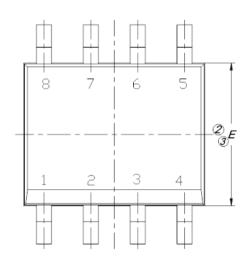
10. Single Pulse Maximum Power Dissipation

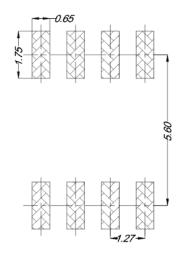


11. Normalized Thermal Transient Junction to Ambient

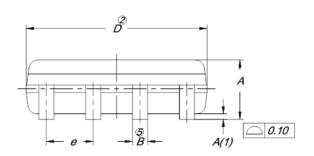
Package Information

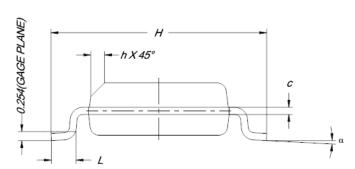
Land Pattern (Only for Reference)





DIM.	MILLIMETERS					
	MIN.	NOM.	MAX.			
Α	1.35	1.55	1.75			
A(1)	0.10	0.18	0.25			
В	0.38	0.45	0.51			
С	0.19	0.22	0.25			
D	4.80	4.90	5.00			
Е	3.80	3.90	4.00			
е	1.27 BSC					
Н	5.80	6.00	6.20			
L	0.50	0.72	0.93			
α	0°	4°	8°			
h	0.25	0.38	0.50			





Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- 5. Dimension B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.