

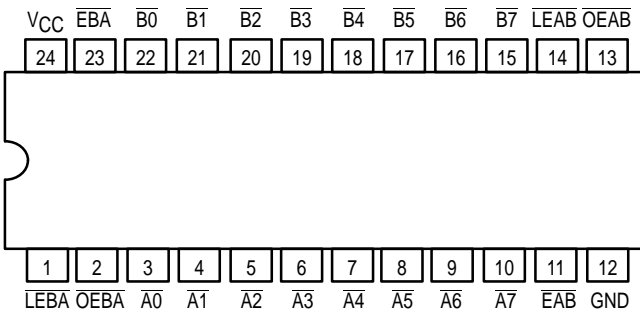


OCTAL REGISTERED TRANSCEIVER, INVERTING, 3-STATE

The MC74F544 Octal Registered Transceivers contain two sets of D-Type latches for temporary storage of data flowing in either direction. Separate Latch Enable (\overline{LEAB} , \overline{LEBA}) and Enable (\overline{OEAB} , \overline{OEBA}) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The MC74F544 has an inverting data path. The A outputs are guaranteed to sink 24 mA while the B outputs are rated for 64 mA.

- Combines 74F245 and 74F373 Type Functions in One Chip
- 8-Bit Octal Transceiver
- Inverting
- Back-to-Back Registers for Storage
- Separate Controls for Data Flow in Each Direction
- Glitchless Outputs During 3-State Power Up or Power Down Operation
- High Impedance Outputs in Power Off State
- A Outputs Sink 24 mA and Source 3.0 mA
- B Outputs Sink 64 mA and Source 15 mA
- See F543 for Noninverting Version
- ESD Protection > 4000 Volts

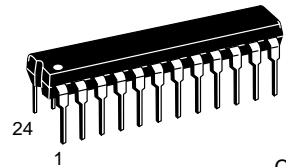
PIN ASSIGNMENT



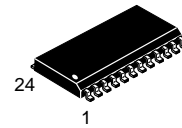
MC74F544

**OCTAL REGISTERED
TRANSCEIVER, INVERTING,
3-STATE**

FAST™ SCHOTTKY TTL



**N SUFFIX
PLASTIC
CASE 724-03**



**DW SUFFIX
SOIC
CASE 751E-03**

ORDERING INFORMATION

MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

| Symbol | Parameter | 74 | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|----|-----|-----|----------|------|
| V _{CC} | DC Supply Voltage | 74 | 4.5 | 5.0 | 5.5 | V |
| T _A | Operating Ambient Temperature Range | 74 | 0 | 25 | 70 | °C |
| I _{OH} | Output Current — High | 74 | — | — | -3.0/-15 | mA |
| I _{OL} | Output Current — Low | 74 | — | — | 24/64 | mA |

MC74F544

FUNCTION TABLE

| Inputs | | | | Outputs | Status |
|------------------------------|-----------------------------|------------------------------|------|---------|------------------|
| $\overline{OE}X\overline{X}$ | $\overline{E}X\overline{X}$ | $\overline{LE}X\overline{X}$ | Data | | |
| H | X | X | X | Z | Outputs disabled |
| X | H | X | X | Z | Outputs disabled |
| L | ↑ | L | l | Z | Outputs disabled |
| L | ↑ | L | h | Z | Data latched |
| L | L | ↑ | l | H | Data latched |
| L | L | ↑ | h | L | |
| L | L | L | L | H | Transparent |
| L | L | L | H | L | |
| L | L | H | X | NC | Hold |

H = HIGH voltage level; h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}X\overline{X}$ or $\overline{E}X\overline{X}$ (XX = AB or BA); L = LOW voltage level; l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}X\overline{X}$ or $\overline{E}X\overline{X}$ (XX = AB or BA); X = Don't care; Z = HIGH impedance state; NC = No Change.

FUNCTIONAL DESCRIPTION

The MC74F544 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{EAB}) input must be LOW in order to enter data from $\overline{A0}-\overline{A7}$ or take data from $\overline{B0}-\overline{B7}$, as indicated in the Function Table. With \overline{EAB} LOW, a LOW signal on the A-to-B latch enable (\overline{LEAB}) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH

transition of the \overline{LEAB} signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{EAB} and \overline{OEAB} both LOW, the 3-State B output buffers are active and reflect the inverted data present at the output of the A latches. Control of data flow from B to A is similar, but using the \overline{EBA} , \overline{LEBA} , and \overline{OEBA} inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | | Limits | | | Unit | Test Conditions (Note 1) | | |
|-----------|---|-------------------------------------|--------|-------|------|---------------|---|---|---------------------------|
| | | | Min | Typ | Max | | | | |
| V_{IH} | Input HIGH Voltage | | 2.0 | — | — | V | Guaranteed Input HIGH Voltage | | |
| V_{IL} | Input LOW Voltage | | — | — | 0.8 | V | Guaranteed Input LOW Voltage | | |
| V_{IK} | Input Clamp Diode Voltage | | — | -0.73 | -1.2 | V | $V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$ | | |
| V_{OH} | Output HIGH Voltage | $A0-A7$ | 74 | 2.4 | — | — | V | $I_{OH} = -3.0 \text{ mA}$ | $V_{CC} = 4.5 \text{ V}$ |
| | | $\overline{B0}-\overline{B7}$ | 74 | 2.0 | — | — | | | $V_{CC} = 4.75 \text{ V}$ |
| V_{OL} | Output LOW Voltage | $A0-A7$ | 74 | — | 0.35 | 0.5 | V | $I_{OL} = 24 \text{ mA}$ | $V_{CC} = \text{MIN}$ |
| | | $\overline{B0}-\overline{B7}$ | 74 | — | 0.4 | 0.55 | | | |
| I_{IH} | Input HIGH Current | I/O Pins | — | — | 1.0 | mA | $V_{CC} = \text{MAX}$, $V_{IN} = 5.5 \text{ V}$ | | |
| | | Control Pins | — | — | 100 | μA | $V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$ | | |
| | | Control Pins | — | — | 20 | μA | $V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$ | | |
| | | I/O Pins | — | — | 70 | μA | | | |
| I_{IL} | Input LOW Current | \overline{EAB} , \overline{EBA} | — | — | -1.2 | mA | $V_{CC} = \text{MAX}$, $V_{IN} = 0.5 \text{ V}$ | | |
| | | Other Inputs | — | — | -0.6 | | | | |
| I_{OZH} | Off-State Output Current | | — | — | 70 | μA | $V_{CC} = \text{MAX}$, $V_{OUT} = 2.7 \text{ V}$ | | |
| I_{OZL} | Off-State Output Current, Low-Level Voltage Applied | | — | — | -600 | μA | $V_{CC} = \text{MAX}$, $V_{OUT} = 0.5 \text{ V}$ | | |
| I_{OS} | Output Short Circuit Current (Note 2) | \overline{A}_n Outputs | — | -60 | — | -150 | mA | $V_{CC} = \text{MAX}$, $V_{OUT} = 0 \text{ V}$ | |
| | | \overline{B}_n Outputs | — | -100 | — | -225 | | | |
| I_{CC} | Total Supply Current | I_{CCH} | — | 70 | 105 | mA | $V_{CC} = \text{MAX}$ | | |
| | | I_{CCL} | — | 95 | 130 | | | | |
| | | I_{CCZ} | — | 95 | 125 | | | | |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F544

AC ELECTRICAL CHARACTERISTICS

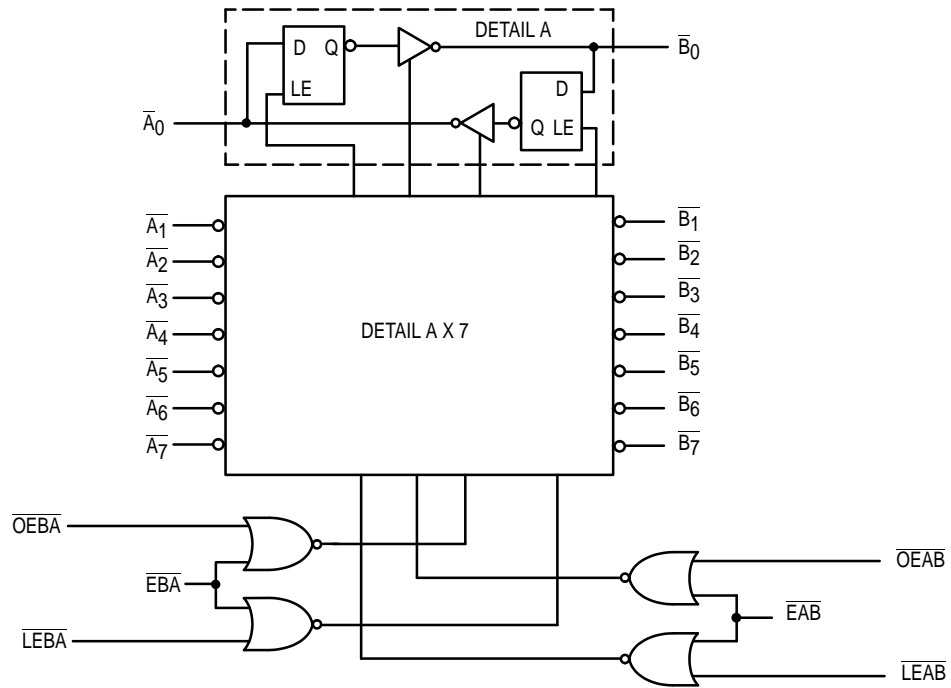
| Symbol | Parameter | 74F | | | 74F | | Unit |
|--------------------------------------|---|--|--------|-------------|---|--------------|------|
| | | T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF | | | T _A = 0 °C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF | | |
| | | Min | Typ | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay Transparent Mode \overline{A}_n to \overline{B}_n or \overline{B}_n to \overline{A}_n | 2.0 2.0 | — — | 9.5 6.5 | 2.0 2.0 | 10.5 7.5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay \overline{LEBA} to \overline{A}_n | 6.0 4.0 | — — | 13 9.5 | 6.0 4.0 | 14.5 10.5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay \overline{LEAB} to \overline{B}_n | 6.0 4.0 | — — | 13 9.5 | 6.0 4.0 | 14.5 10.5 | ns |
| t _{PZH} t _{PZL} | Output Enable Time \overline{OEBA} or \overline{OEAB} to \overline{A}_n or \overline{B}_n \overline{EBA} or \overline{EAB} to \overline{A}_n or \overline{B}_n | 3.0 4.0 | — — | 9.0 10.5 | 3.0 4.0 | 10 12 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time \overline{OEBA} or \overline{OEAB} to \overline{A}_n or \overline{B}_n \overline{EBA} or \overline{EAB} to \overline{A}_n or \overline{B}_n | 1.5 1.5 | — — | 8.0 7.5 | 1.5 1.5 | 9.0 8.5 | ns |

AC OPERATING REQUIREMENTS

| Symbol | Parameter | 74F | | | 74F | | | Unit |
|--|---|--|--------|--------|--|--------|--------|------|
| | | T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| t _{s(H)} t _{s(L)} | Setup Time, HIGH or LOW \overline{A}_n or \overline{B}_n to \overline{LEBA} or \overline{LEAB} | 3.0 3.0 | — — | — — | 3.0 3.0 | — — | — — | ns |
| t _{h(H)} t _{h(L)} | Hold Time, HIGH or LOW \overline{A}_n to \overline{B}_n to \overline{LEBA} or \overline{LEAB} | 3.0 3.0 | — — | — — | 3.0 3.0 | — — | — — | ns |
| t _{w(L)} | Latch Enable, B to A Pulse Width, LOW | 6.0 | — | — | 7.5 | — | — | ns |

MC74F544

LOGIC DIAGRAM



NOTE:

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.