October 1989
Edition 1.0

FUJITSU

DATA SHEET

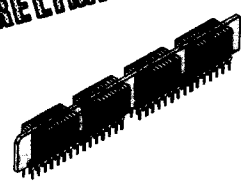
MB85410-30/-40
64K x 8 CMOS SRAM MODULE

CMOS 65,536 WORDS x 8-BIT HIGH SPEED STATIC RANDOM ACCESS MEMORY MODULE

The Fujitsu MB85410 is a fully decoded, CMOS static random access memory module consists of eight MB81C71A devices mounted on a 60-pin plastic board.
Organized as eight 64K x 1 devices, the MB85410 is optimized for those applications requiring high speed, high performance, large memory storage, and high density.

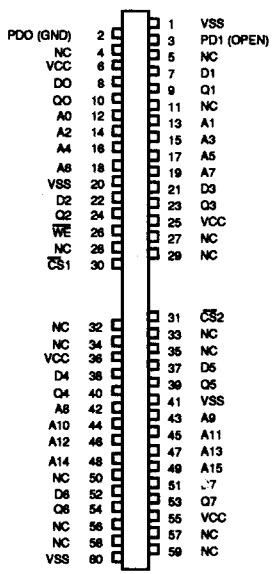
- Organized as 65,536 x 8-bit Words
- Memory: MB81C71A, 8 pcs
- Access Time: 30 ns max (MB85410-30)
  40 ns max (MB85410-40)
- Low Power Dissipation
  Standby : 440 mW max (CMOS level)
  880 mW max (TTL level)
  Active : 3200 mW max
- Single +5V Power Supply, ±10% Tolerance
- Automatic Power Down
- Dual Chip Select (x8 or x4 organization)
- TTL Compatible Input/Output Pins
- 3-State Output
- Decoupling Capacitor: .22µF, 8pcs
- 60-Pin Plastic(FR-4) ZIP

PRELIMINARY



PLASTIC PACKAGE
MZP-60P-P02

PIN ASSIGNMENT
TOP VIEW



ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.5 to +7.0	V
Ouput Voltage	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	8.0	W
Temperature under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−45 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

Fig. 1 — BLOCK DIAGRAM

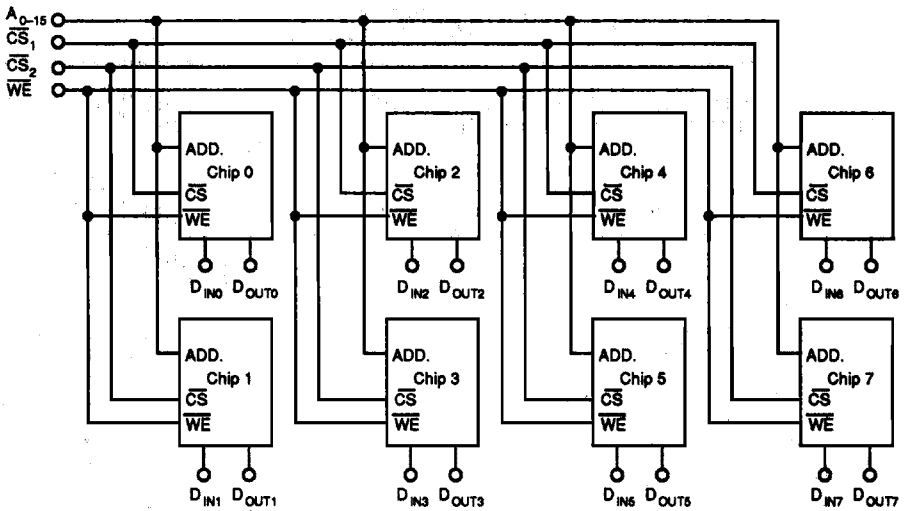
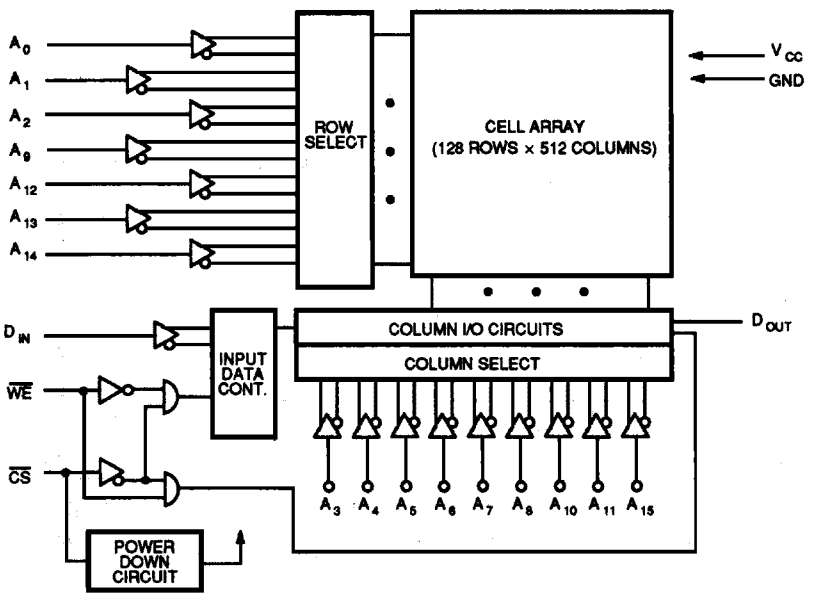


Fig. 2 – BLOCK DIAGRAM FOR EACH MEMORY



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CAPACITANCE

(T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, Address and $\overline{WE}$	C_{IN1}		80	pF
Input Capacitance, $\overline{CS}_1$ and $\overline{CS}_2$	C_{IN2}		40	pF
Input Capacitance, D_{IN}	C_{IN3}		10	pF
Output Capacitance, D_{OUT}	C_{OUT}		10	pF

FUNCTIONAL TRUTH TABLE

Mode	Address	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	Input	Output	Power
Standby	Don't Care	V_{IH}	V_{IH}	Don't Care	High–Z	High –Z	Standby
Write	Valid	V_{IL}	V_{IL}	V_{IL}	D_{IN}	High–Z	Active
Read	Valid	V_{IL}	V_{IL}	V_{IH}	High–Z	D_{OUT}	Active

6

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	GND		0		V
Operating Temperature Range	T_A	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

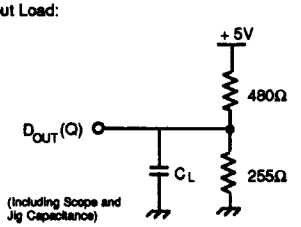
Parameter (conditions)		Symbol	Values			Unit
			Min	Typ	Max	
Input Leakage Current (V_{IN} = 0V to V_{CC})		I_{LI}	–80		80	µA
Output Leakage Current ($\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC})		I_{LO}	–10		10	µA
Standby Power Supply Current	CMOS level	I_{SB1}			80	mA
	TTL level	I_{SB2}			160	mA
Active Power Suppry Current ($\overline{CS}$ = V_{IL} , I_{OUT} = 0mA)		I_{CC}			640	mA
Peak Power on Supply Current ($\overline{CS}$ = Lower of V_{CC}, or V_{IH})		I_{PO}			240	mA
Input High Level		V_{IH}	2.2		6.0	V
Input Low Level *1		V_{IL}	–0.5		0.8	V
Output High Level (I_{OH} = – 4mA)		V_{OH}	2.4			V
Output Low Level (I_{OL} = 16mA)		V_{OL}			0.4	V

Note : *1 – 2.0V min. for pulse width less than 20ns.

6

Fig. 3 – AC TEST CONDITIONS

- Input Pulse Levels : 0.6V to 2.4V
- Input Rise and Fall Times : 5ns(Transient between 0.8V and 2.2V)
- Timing Reference Levels : 1.5V (Input and Output)
- Output Load:



	C_L
Load I	30pF
Load II	5pF

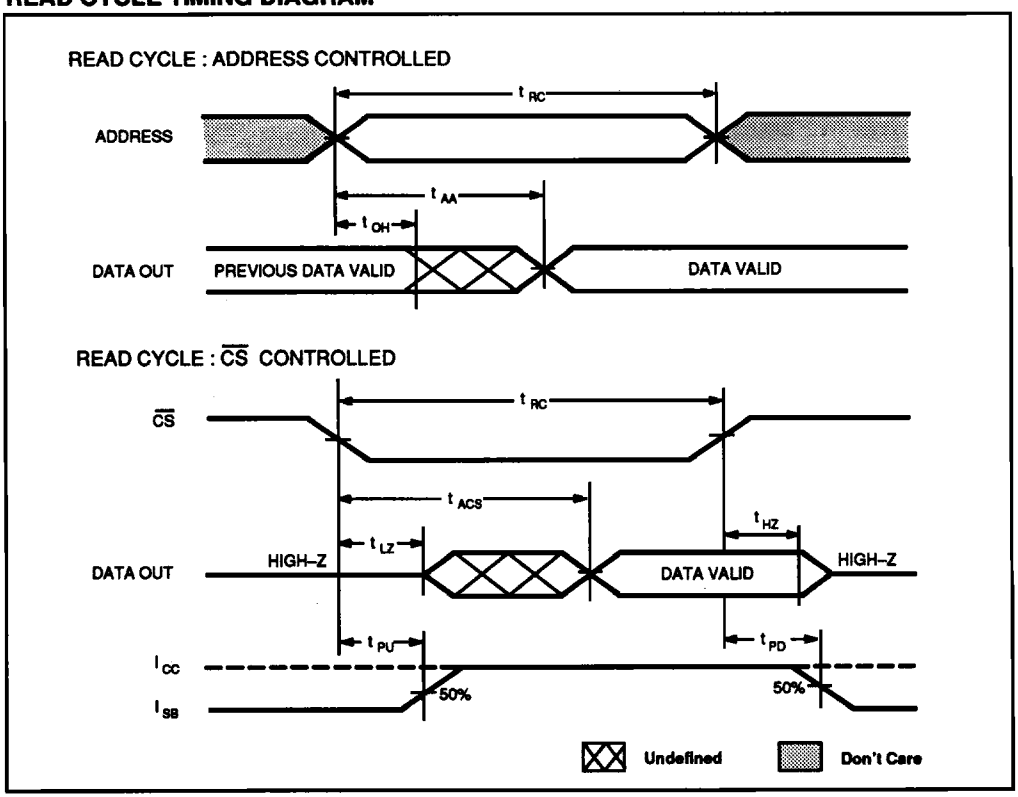
AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB85410-30		MB85410-40		Unit
		Min	Max	Min	Max	
Read Cycle Time *1	t_{RC}	30		40		ns
Address Access Time	t_{AA}		30		40	ns
$\overline{CS}$ Access Time *2	t_{ACS}		30		40	ns
Output Hold from Address Change	t_{OH}	5		5		ns
$\overline{CS}$ to Output Low-Z *3*4	t_{LZ}	5		5		ns
$\overline{CS}$ to Output High-Z *3*4	t_{HZ}	0	10	0	15	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		20		30	ns

READ CYCLE TIMING DIAGRAM



Note: *1 Device is continuously selected, $\overline{CS} = V_{IL}$.

*2 Address valid prior to or coincident with $\overline{CS}$ transition low.

*3 Transition is measured at the point of ± 500mV from steady state voltage.

*4 This parameter is specified with Load II in Fig. 3.

6

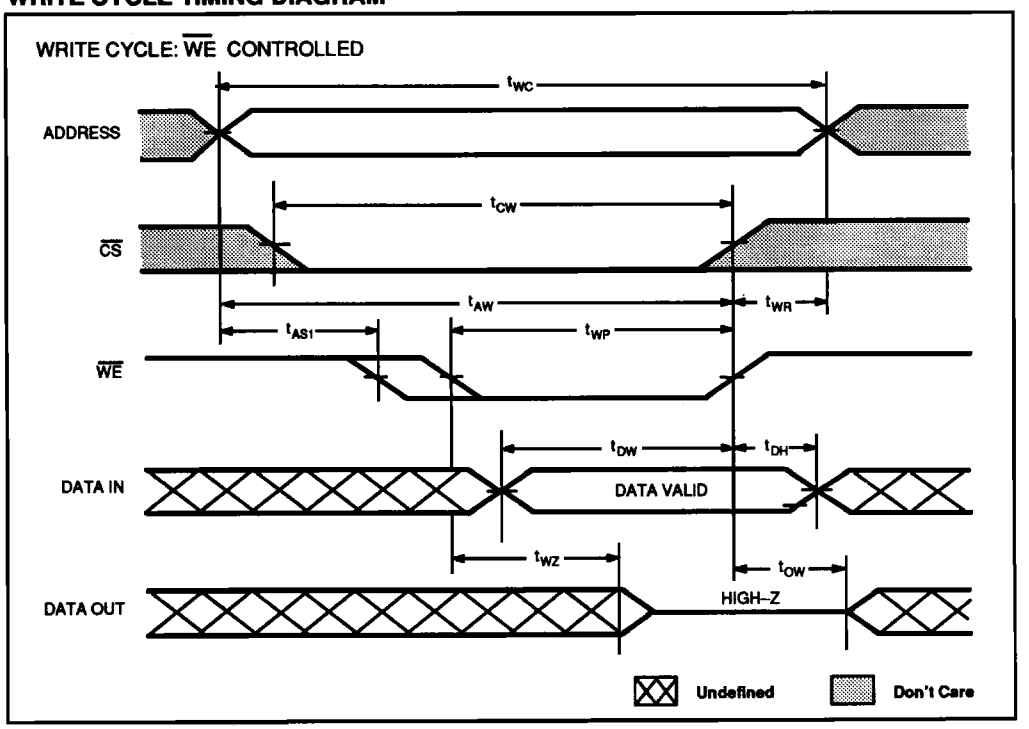
AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	MB85410-30		MB85410-40		Unit
		Min	Max	Min	Max	
Write Cycle Time *2	t_{WC}	30		40		ns
Address Valid to End of Write	t_{AW}	25		35		ns
$\overline{CS}$ to End of Write	t_{CW}	25		35		ns
Data Hold Time	t_{DH}	2		2		ns
Write Pulse Width	t_{WP}	20		30		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Address Setup Time	t_{AS1}	0		0		ns
	t_{AS2}	0		0		ns
Write Recovey Time	t_{WR}	2		2		ns
Output High-Z from $\overline{WE}$ *3*4	t_{WZ}	0	10	0	15	ns
Output Low-Z from $\overline{WE}$ *3*4	t_{OW}	0		0		ns

WRITE CYCLE TIMING DIAGRAM



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

*2 All write cycle are determined from last address transition to the first address transition of the next address.

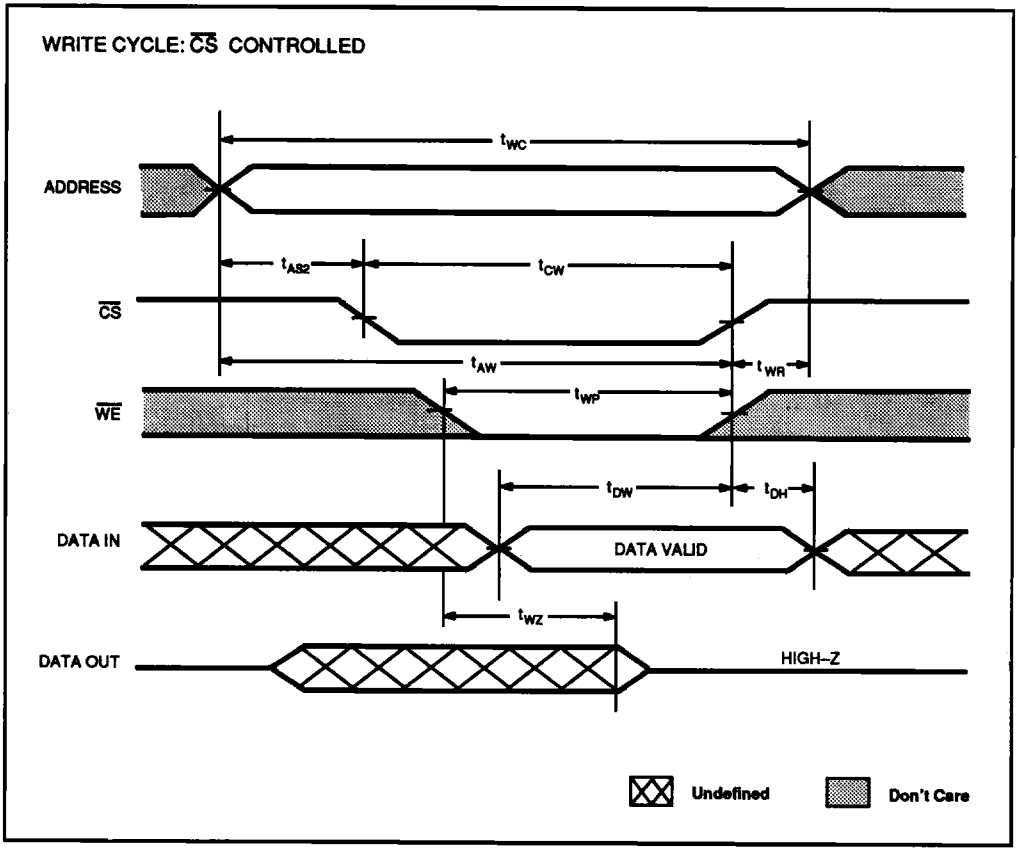
*3 Transition is measured at the point of ±500mV from steady state voltage.

*4 This parameter is specified with Load Π in Fig. 3.

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM



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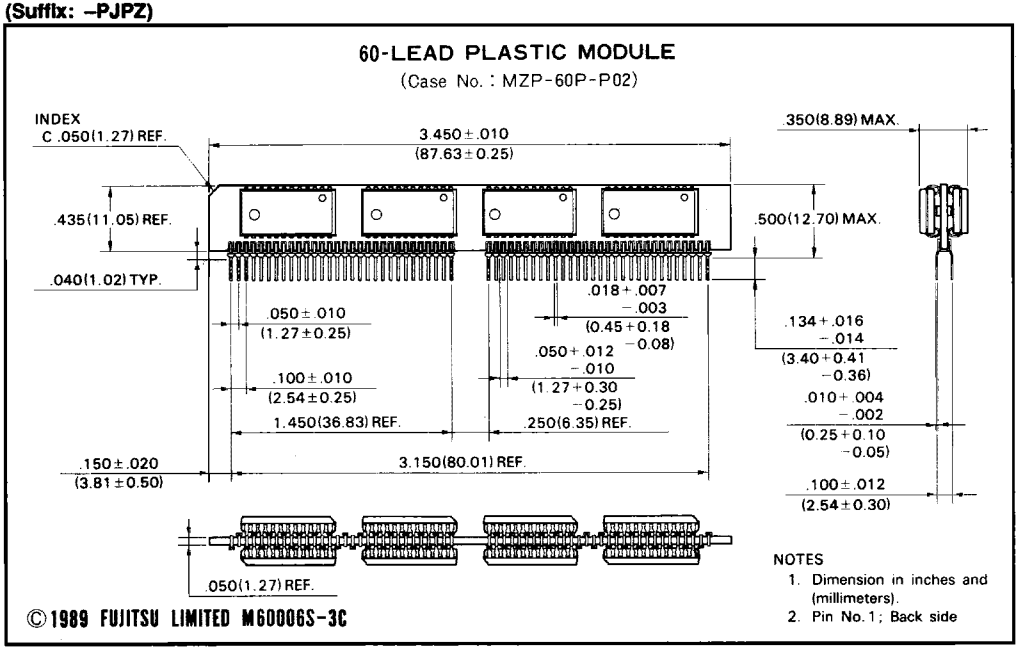
PACKAGE DIMENSIONS

(Suffix: –PJPZ)



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