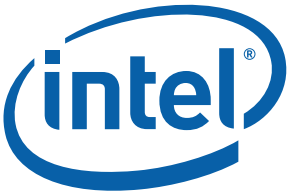

Intel® 82577 GbE PHY Specification Update

January 2012
Revision 1.7

Revision History

Date	Revision	Description
January 2012	1.7	Added Specification Change #1. Added Sofware Clarification #1. Added Specification Clarification 2.
February 2010	1.6	Added Thailand as a Country Of Origin (COO) to Figure 1.
January 2010	1.5	Added Specification Clarification #1. Removed Erratum #2.
November 2009	1.4	Removed Specification Change #1. Added Erratum #2.
September 2009	1.3	Initial Public Release.

1.1 Introduction and Scope

This document applies to the 82577 GbE PHY.

This document is an update to a published specification, the *Intel® 82577 GbE PHY Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.2 Product Code and Device Identification

Table 1 and Figure 1 describe the various identifying markings on each lead-free device package:

Table 1. Markings

Device	Stepping	Top Marking	MM #	Description	Tray/Tape and Reel
82577LM	A3	WG82577LM	903235	Corporate Mobile and Workstation	Tape and Reel
82577LM	A3	WG82577LM	903236	Corporate Mobile and Workstation	Tray
82577LC	A3	WG82577LC	903237	Consumer Mobile	Tape and Reel
82577LC	A3	WG82577LC	903238	Consumer Mobile	Tray

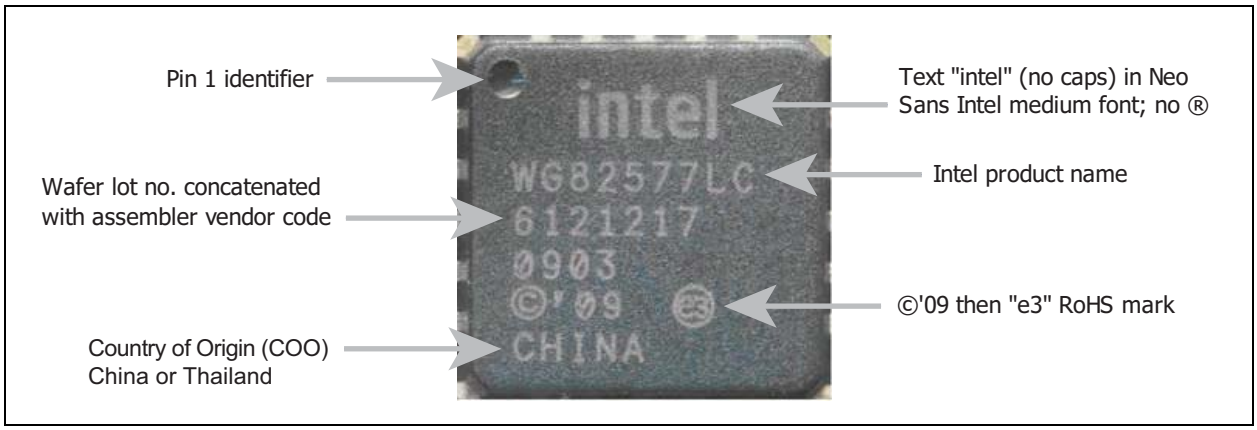

Figure 1. Typical Top Marking Example With Identifying Marks (82577LC Shown)

Table 2. Device IDs

Device ID Code	Vendor ID	Device ID	Revision ID
82577LM	0x8086	0x10EA	N/A
82577LC	0x8086	0x10EB	N/A

1.3 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata, sightings and/or clarifications that apply to silicon/steppings. See Table 3 for a description.

Table 3. Terms, Codes, Abbreviations

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Yes or No	If the errata applies to a stepping, "Yes" is indicated for the stepping (for example: "A0=Yes" indicates errata applies to stepping A0). If the errata does not apply to stepping, "No" is indicated (for example: "A0=No" indicates the errata does not apply to stepping A0).
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Red Change Bar / or Bold	This Item is either new or modified from the previous version of the document.
DS	Datasheet
PDG	Platform Design Guide
EDS	External Data Specification

1.4 Changes, Errata, Clarifications

See Section 1.3 for an explanation of terms, codes, and abbreviations used in the following tables and discussions.

Table 4. Summary of Changes

1.4.1 Specification Changes

1. Updates to PXE/iSCSI EEPROM Words

Word 0x30 (bits 2:0) is now defined as follows:

Bit(s)	Value	Port Status	CLP (Combo) Executes	iSCSI Boot Option ROM CTRL-D Menu	FCoE Boot Option ROM CTRL-D Menu
2:0	0	PXE	PXE	Displays port as PXE. Allows changing to Boot Disabled, iSCSI Primary or Secondary.	Displays port as PXE. Allows changing to Boot Disabled, FCoE enabled.
	1	Boot Disabled	NONE	Displays port as Disabled. Allows changing to iSCSI Primary/Secondary.	Displays port as Disabled. Allows changing to FCoE enabled.
	2	iSCSI Primary	iSCSI	Displays port as iSCSI Primary. Allows changing to Boot Disabled, iSCSI Secondary.	Displays port as iSCSI. Allows changing to Boot Disabled, FCoE enabled.
	3	iSCSI Secondary	iSCSI	Displays port as iSCSI Secondary. Allows changing to Boot Disabled, iSCSI Primary.	Displays port as iSCSI Allows changing to Boot Disabled, FCoE enabled.
	4	FCoE	FCOE	Displays port as FCoE. Allows changing port to Boot Disabled, iSCSI Primary or Secondary.	Displays port as FCoE Allows changing to Boot Disabled.
	7:5	Reserved	Same as disabled.	Same as disabled.	Same as disabled.
4:3	Same a before.				
5	Bit 5: formerly used to indicate iSCSI enable / disable, is no longer valid and is not checked by software.				
15:7	Same a before.				

1.4.2 Specification Clarifications

1. PHY Does Not Maintain Gigabit Link in Low Power States

Clarification: While operating in power states less than D0 or operating system states other than S0, the PHY is designed to negotiate to the lowest speed possible, and maintains a link in those states only at 10 Mb/s or 100 Mb/s. If the PHY is connected to a link partner that is only capable of gigabit connections, the link is lost in these lower power states. This limitation is due to power requirements imposed by energy saving initiatives (such as Energy Star), as the additional power required to maintain gigabit connections might cause the system to exceed the level needed to meet the specifications.

Impact: When attached to a port that is limited to gigabit speed connections, the PHY loses link in low power states, and therefore network functions normally available in those states, such as Wake on LAN (WoL) or remote management, is not possible in that environment.

2. Activity LED Functionality

Clarification: If a system based on the 82577 is connected to a hub, the Activity LED blinks for all network traffic present on the hub, not just traffic destined to the local port. Connecting the system to a switch or router filters out most traffic not addressed to the local port.

1.4.3 Software Clarifications

1. While in TCP Segmentation Offload, Each Buffer is Limited to 64 KB

Problem Description:

Clarification: The 82577 supports 256 KB TCP packets; however, each buffer is limited to 64 KB since the data length field in the transmit descriptor is only 16 bits. This restriction increases driver implementation complexity if the operating system passes down a scatter/gather element greater than 64 KB in length. This can be avoided by limiting the offload size to 64 KB.

Investigation has concluded that the increase in data transfer size does not provide any noticeable improvements in LAN performance. As a result, Intel network software drivers limit the data transfer size in all drivers to 64 KB.

Please note that Linux operating systems only support 64 KB data transfers.

For further details about how Intel network software drivers address this issue, refer to Technical Advisory TA-191.

1.4.4 Documentation Changes

None active.

1.4.5 Errata

1. 9 KB Jumbo Frames Not Supported With PCI Express* (PCIe*) Spread Spectrum Clocking (SSC)

Problem: 82577LM is unable to support 9 KB jumbo frames when PCIe SSC is enabled in Intel® 5 Series Express Chipset.

Implication: Enabling 9 KB jumbo frames with PCIe SSC enabled might result in data overflow/ underflow errors resulting in packets transmitted/received with CRC errors.

Workaround: For 9 KB jumbo frames support, PCIe SSC must be disabled.

Status: No fix for 9 KB jumbo frames.

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