YAMAHA LSI

YTM401

MD96DX (9600 bps FAX MODEM LSI with HDLC)

■ OUTLINE

MD96DX is a one-chip MODEM LSI of 9600 bps, which is upper compatible with our FAX MODEM-LSI MD96FX (YM7109) in pin assignment and software. It is also provided with HDLC function, power saving functions, simple UART and external clock synchronization function.
MD96DX can execute HDLC function on hardware for any half-duplex communications mode, realizing high speed data transmission without transmission errors. This is the most suitable modem for G3 facsimile machines using ECM (error correction mode).
MD96DX has hardware power saving mode with an external terminals and software power saving mode with register control. Thus, in addition to low power consumption during operation (300 mW at max.), considerable power saving is enabled when MD96DX is not in use. This makes the product suitable for use in portable machines.
MD96DX is packaged as 40-pin DIP, 64-pin QFP and 68-pin PLCC, and operated by +5V single power supply to provide you a great advantage in board design.

■ FEATURES

- Upper compatible with YM7109 (our FAX MODEM) in software and terminal assignment
- CCITT V.29 (9600/7200 bps) – Half-duplex, synchronous
  V.27ter (4800/2400 bps) – Half-duplex, synchronous
  V.21ch2 (300 bps) – Half-duplex, synchronous
  V.23 backward ch (75 bps) – Transmission only
  V.21 (300 bps) – Full-duplex
- BELL 103 (300 bps) – Full-duplex
- Full-duplex communication of V. 27ter reception and V. 23 (75 bps) transmission is available in CAPTAIN mode.

◎ Incorporated HDLC framing function enables use of ECM mode on G3 facsimile

- Compatible with public switched telephone network (two-wire)
- Dual-tone generation (programmable)
- Tone detection (programmable)
- DTMF detection (programmable)
- V.21 ch2 flag pattern detection
- Transmission level: 0 to – 15 dBm (programmable)

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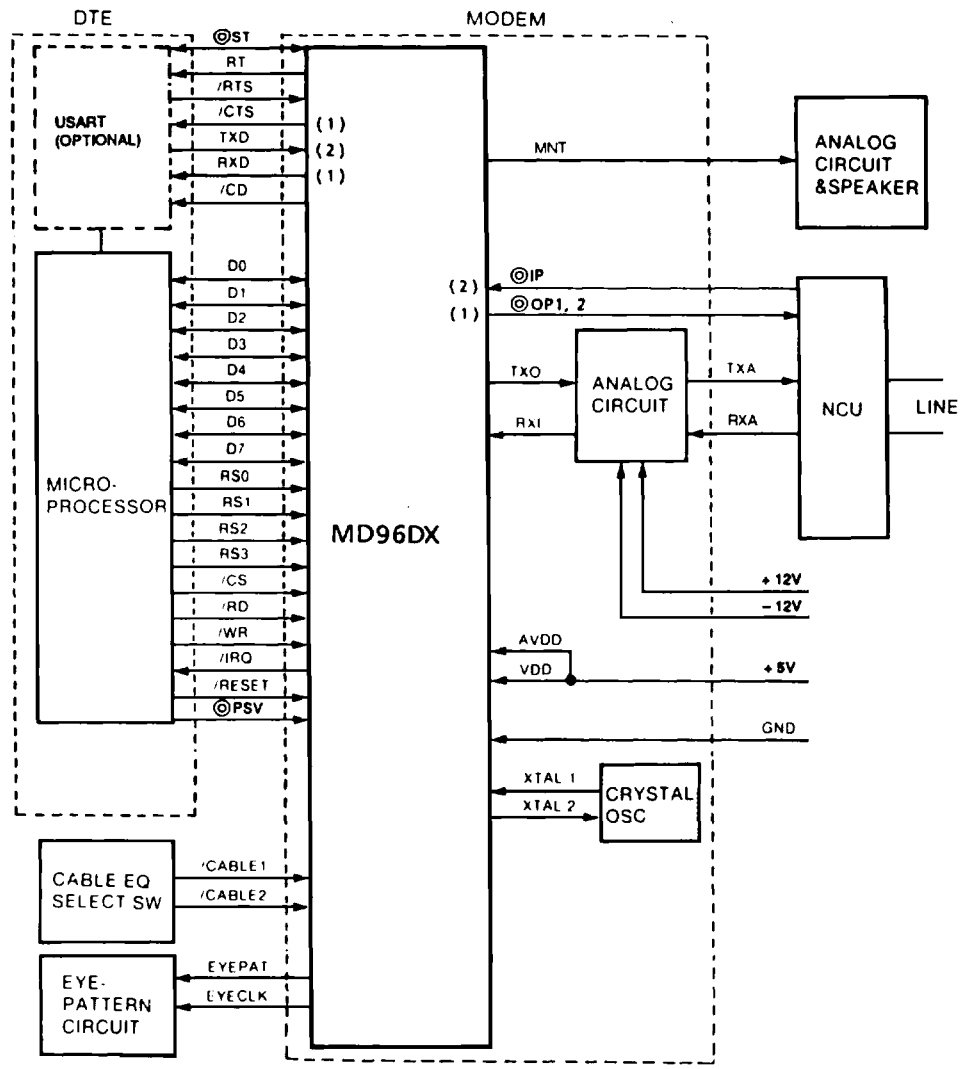
YTM401 CATALOG
CATALOG No.: LSI-4TM4014
1993. 2

- Reception dynamic range: 0 to — 43 dBm (programmable)
- Automatic equalization and subscriber cable equalization
- Built-in bandpass filter for transmission and reception, A/D converter, D/A converter, and automatic gain control (AGC).
- Parallel and serial (CCITT V.24) interfaces
- ◎ Terminals for serial interface can be used as general purpose input/output terminal when serial interface is not in use.
- ◎ External clock synchronization function
- 40-pin DIP, 64-pin QFP, or 68-pin PLCC package
- Low power consumption due to CMOS
- + 5V single power supply
- ◎ Power saving mode with external terminal and interface register (When power saving applied: 5 μA)

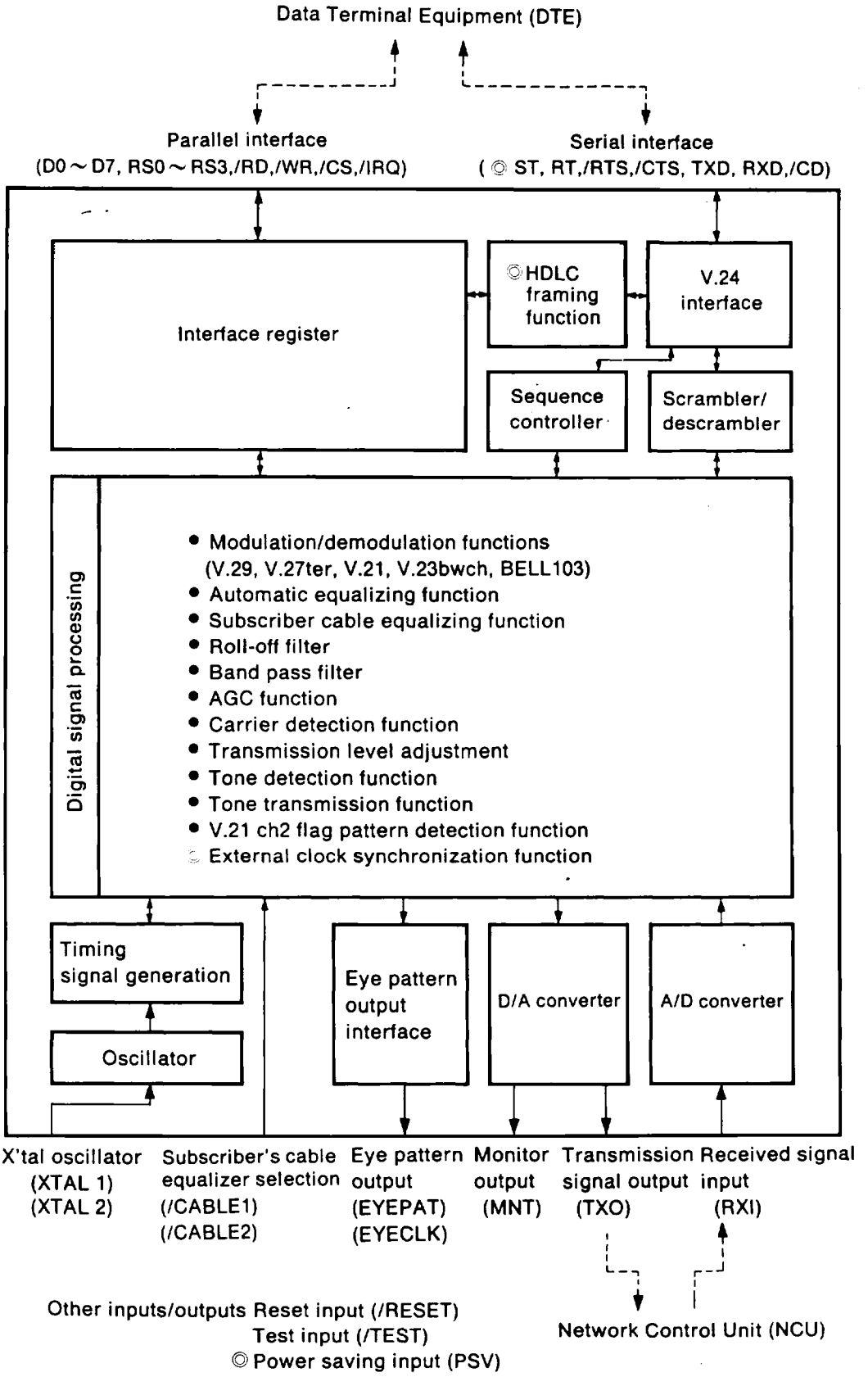
  New features of MD96DX is marked with ◎

■SYSTEM BLOCK DIAGRAM



Note) (1) becomes OP1 and OP2 in parallel mode and/CTS, RXD in serial mode.
(2) becomes IP in parallel mode and TXD in serial mode.
◎ Shows the pin added to or changed for MD96DX from MD96FX.

■ INTERNAL BLOCK DIAGRAM



◎ Shows the function added to or changed for MD96DX from MD96FX

■ OPERATING MODES AND COMMUNICATION PROTOCOLS

The MD96DX has the eight operating modes listed below:

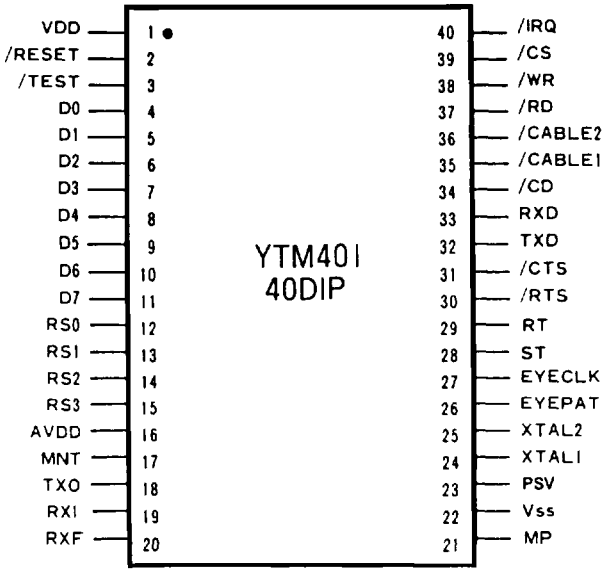
1 9600 bps half-duplex reception/transmission: CCITT V.29
2 7200 bps half-duplex reception/transmission: CCITT V.29
3 4800 bps half-duplex reception/transmission: CCITT V.27ter
4 2400 bps half-duplex reception/transmission: CCITT V.27ter
5 300 bps half-duplex reception/transmission: CCITT V.21 ch2
6 300 bps full-duplex reception/transmission: CCITT V.21 or BELL 103
7 CAPTAIN full-duplex reception/transmission: CCITT V.27ter (4800 bps) and V.23 Backward CH (75 bps)
8 TONE transmission and detection

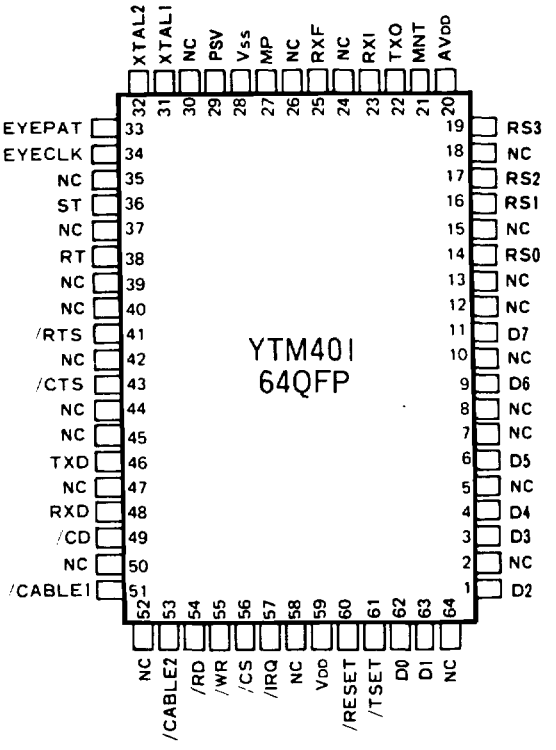
The protocols used in Modes (1) through (7) conform either to the CCITT Recommendation or the BELL Standard. The specifications of these communication protocols are outlined below.

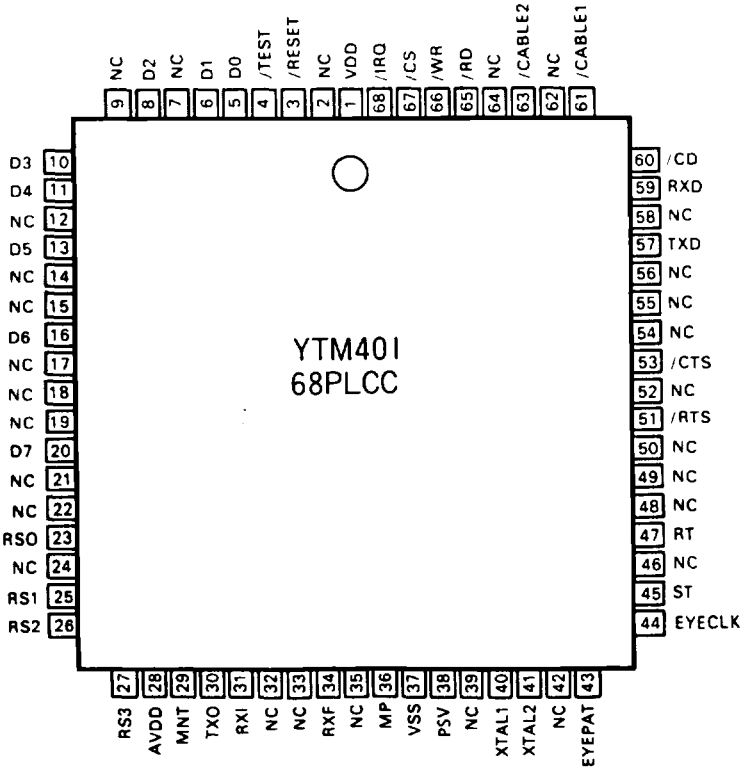
Protocol		Transfer Rate (bps)	Modulation Rate (Baud)	Carrier Frequency (Hz)	Modulation System	Communication Method
CCITT V.29		9600	2400	1700	16-QAM	Two-wire half-duplex synchronous
		7200	2400	1700	8-QAM	
CCITT V.27ter		4800	1600	1800	8-PSK	
		2400	1200	1800	4-PSK	
CCITT V.21	CH 1	300	300	Space 1180 Mark 980	FSK	Two-wire full duplex or Two-wire half duplex synchronous using CH 2
	CH 2	300	300	Space 1850 Mark 1650	FSK	
CCITT V.23 Backward CH		75	75	Space 450 Mark 390	FSK	Transmission only (Two-wire full duplex communication is possible in combination with V.27ter reception)
BELL 103	CH1	300	300	Space 1070 Mark 1270	FSK	Two-wire full duplex
	CH 2	300	300	Space 2025 Mark 2225	FSK	

■ TERMINAL DESCRIPTION

1. Pin Assignment







PIN NAME	40 DIP	64 QFP	68PLCC
VDD	1	59	1
/RESET	2	60	3
/TEST	3	61	4
D0	4	62	5
D1	5	63	6
D2	6	1	8
D3	7	3	10
D4	8	4	11
D5	9	6	13
D6	10	9	16
D7	11	11	20
RS0	12	14	23
RS1	13	16	25
RS2	14	17	26
RS3	15	19	27
AVDD	16	20	28
MNT	17	21	29
TXO	18	22	30
RXI	19	23	31
RXF	20	25	34
MP	21	27	36
VSS	22	28	37
PSV	23	29	38
XTAL1	24	31	40
XTAL2	25	32	41
EYEPAT	26	33	43
EYECLK	27	34	44
ST	28	36	45
RT	29	38	47
/RTS	30	41	51
/CTS	31	43	53
TXD	32	46	57
RXD	33	48	59
/CD	34	49	60
/CABLE1	35	51	61
/CABLE2	36	53	63
/RD	37	54	65
/WR	38	55	66
/CS	39	56	67
/IRQ	40	57	68

NOTE:

NC Pin of 68 PLCC

2, 7, 9, 12, 14, 15, 17, 18, 19, 21, 22, 24, 32, 33, 35, 39, 42, 46, 48, 49, 50, 52, 54, 55, 56, 58, 62, 64

NC Pin of 64 QFP

2, 5, 7, 8, 10, 12, 13, 15, 18, 24, 26, 30, 35, 37, 39, 40, 42, 44, 45, 47, 50, 52, 58, 64

2. Terminal Functions

PIN NAME	TYPE	FUNCTION
VDD	PWR	Digital +5V power supply
PSV	DI	Power save control input
XTAL1	XI	Quartz oscillator input or external clock input (9.8304 MHz)
XTAL2	XO	Quartz oscillator output
/RESET	DI	System Reset input (Reset when LOW)
/TEST	DIP	TEST mode input (normally HIGH or OPEN)
EYEPAT	DO	Eye-pattern serial output
EYECLK	DO	Eye-pattern clock output (4.9152 MHz)
ST	DIO	Transmitter element timing output (external clock input)
RT	DO	Transmitter/receiver element timing output
/RTS	DIP	Request-to-Send input (with built-in pull-up)
/CTS	DO	Clear-to-Send output/General-purpose output terminal
TXD	DIP	Transmit-Data input/General-purpose input terminal (with built-in pull-up)
RXD	DO	Receive-Data output/General-purpose output terminal
/CD	DO	Receive carrier detect output
D0 ~ D7	DIO	Data bus (8 bits)
RS0 ~ RS3	DI	Register selection input (4 bits)
/RD	DI	Read strobe input
/WR	DI	Write strobe input
/CS	DI	Chip select input
/IRQ	DOD	Interrupt-Request output (open drain output)
/CABLE1	DIP	Subscriber cable equalizer selection input
/CABLE2	DIP	(with built-in pull-up)
AVDD	PWR	Analog +5V power supply
VSS	GND	Analog ground
TXO	AO	Transmit signal analog output
RXI	AI	Receive signal analog input
RXF	AO	Capacitor terminal for AD conversion
MP	AO	Reference voltage terminal for AD conversion
MNT	AO	Analog output for the monitor

NOTE: The "/" prefix indicates an active-LOW signal.
General-purpose input and output terminal can be used only in parallel mode.

DI: Digital input
DIP: Built-in pull up digital input
DO: Digital output
DO: Open drain output
DIO: Digital I/O
AI: Analog input
AO: Analog output

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (VSS shall be 0V)

ITEM	SYMBOL	RATING		UNIT
		Min.	Max.	
Supply voltage	V_{DD}	−0.5	7.0	V
Input voltage	V_I	−0.5	V_{DD} + 0.5	V
Output voltage	V_O	−0.5	V_{DD} + 0.5	V
Storage temperature	T_{STG}	−50	+125	°C

2. Recommended Operating Conditions (VSS shall be 0V)

ITEM	SYMBOL	RATING			UNIT
		Min.	Typ.	Max.	
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Ambient operating temperature	Top	0	25	70	°C
Clock frequency	f_{CLK}	9.82942	9.83040	9.83138	MHz

3. DC Characteristics (recommended operating condition applied unless otherwise specified)

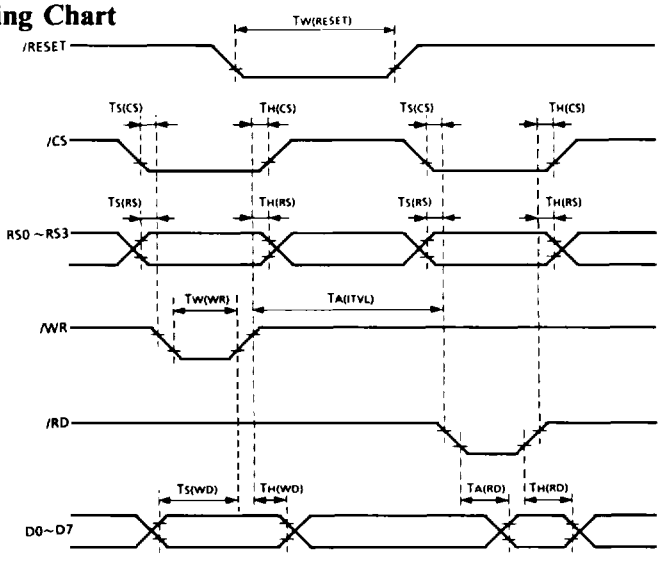
Parameter	Symbol	Applicable pin type and measurement condition	Rating			Unit
			min.	typ.	max.	
High-level input voltage	V_{DIH}	DI, DIP, DIO	2.0	—	—	V
Low-level input voltage	V_{DIL}		—	—	0.8	V
Input leak current	I_{LDIH}	DI	−10	—	+10	μA
High-level output voltage	V_{DOH}	DO, DIO @2.0mA	V_{DD}-1.0	—	—	V
Low-level output voltage	V_{DOL}		—	—	0.4	V
High-level clock input voltage	V_{CLKH}	XI In case of external clock input without crystal oscillation	V_{DD}-1.0	—	—	V
Low-level clock input voltage	V_{CLKL}		—	—	1.0	V
Clock input leak current	I_{LCLK}		−100	—	+100	μA
Analog input voltage range	V_{AI}	AI	0.0	—	V_{DD}	V
Analog input leak current	I_{LAI}		−1	—	+1	mA
Open-drain output current	I_{DOD}	DOD @0.4V	4.0	—	—	mA
Input/output capacitance	C_{IO}	At DIO, DOD, or HI-Z	—	—	12.0	pF
Output leak current	I_{LOUT}		−10	—	+10	μA
Pull-up current	I_{PU}	DIP	10	—	100	μA
Analog output voltage range	V_{AO}	AO	0.0	—	V_{DD}	V
Power current	I_{DD}	PWR, GND	—	40	60	mA
Source current in hardware power save mode	I_{HPSV}	PWR, GND	—	5	50	μA
Source current in software power save mode	I_{SPSV}	PWR, GND	—	200	500	μA

Note) The current of the power I_{HPSV} was measured with the input/output terminals open in hard power save mode.

4. A.C. Characteristics (The recommended operating conditions unless otherwise indicated)

ITEM	SYMBOL	CONDITIONS	RATING			UNIT
			Min.	Typ.	Max.	
Reset input pulse width	TW(RESET)		1.0	—	—	msec
/CS setup time	TS(CS)	For /RD, /WR	0	—	—	nsec
/CS hold time	TH(CS)	Same as above	10	—	—	nsec
/RS setup time	TS(RS)	Same as above	0	—	—	nsec
/RS hold time	TH(RS)	Same as above	10	—	—	nsec
Write data setup time	TS(WD)		30	—	—	nsec
Write data hold time	TH(WD)		10	—	—	nsec
Write pulse width	TW(WR)		75	—	—	nsec
Read data access time	TA(RD)	CL = 100PF	—	—	140	nsec
Read data hold time	TH(RD)		10	—	50	nsec
Read cycle time	TCYC(RD)		1	—	—	μsec
Write cycle time	TCYC(WR)		1	—	—	μsec

AC Characteristics Timing Chart



The specifications of this product are subject to improvement changes without prior notice.

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