GENERAL DESCRIPTION

The XRT83SL28 is a fully integrated 8-channel E1 short-haul LIU which optimizes system cost and performance by offering key design features. The XRT83SL28 operates from a single 3.3V power supply. The LIU features are programmed through a standard serial microprocessor interface or hardware control. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

Additional features include TAOS for transmit and receive, RLOS, LCV, AIS, DMO, and diagnostic loopback modes.

APPLICATIONS

- ISDN Primary Rate Interface
- CSU/DSU E1 Interface
- E1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- E1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA) Wireless Base Stations

FIGURE 1. HOST MODE BLOCK DIAGRAM OF THE XRT83SL28

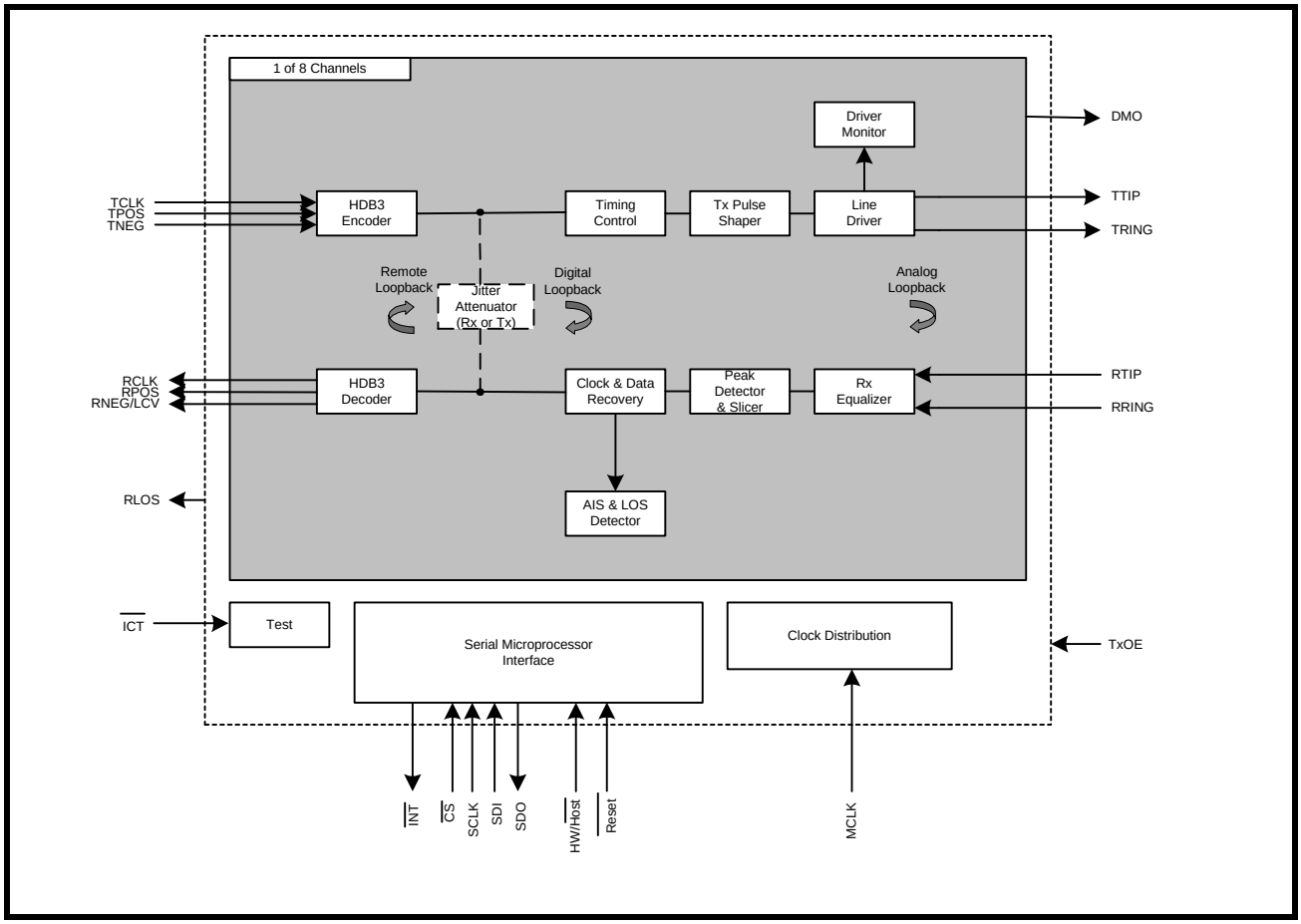
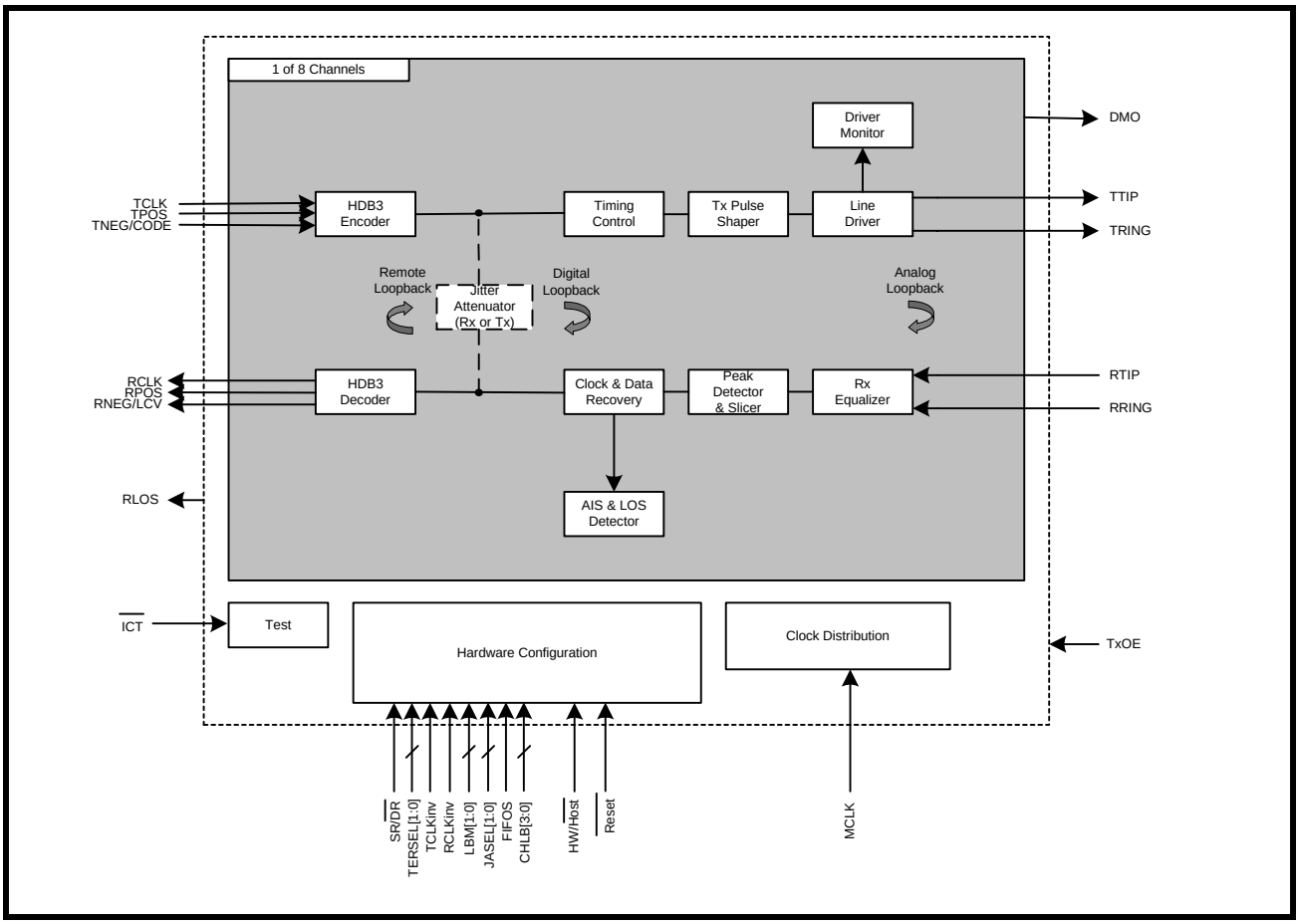


FIGURE 2. HARDWARE MODE BLOCK DIAGRAM OF THE XRT83SL28



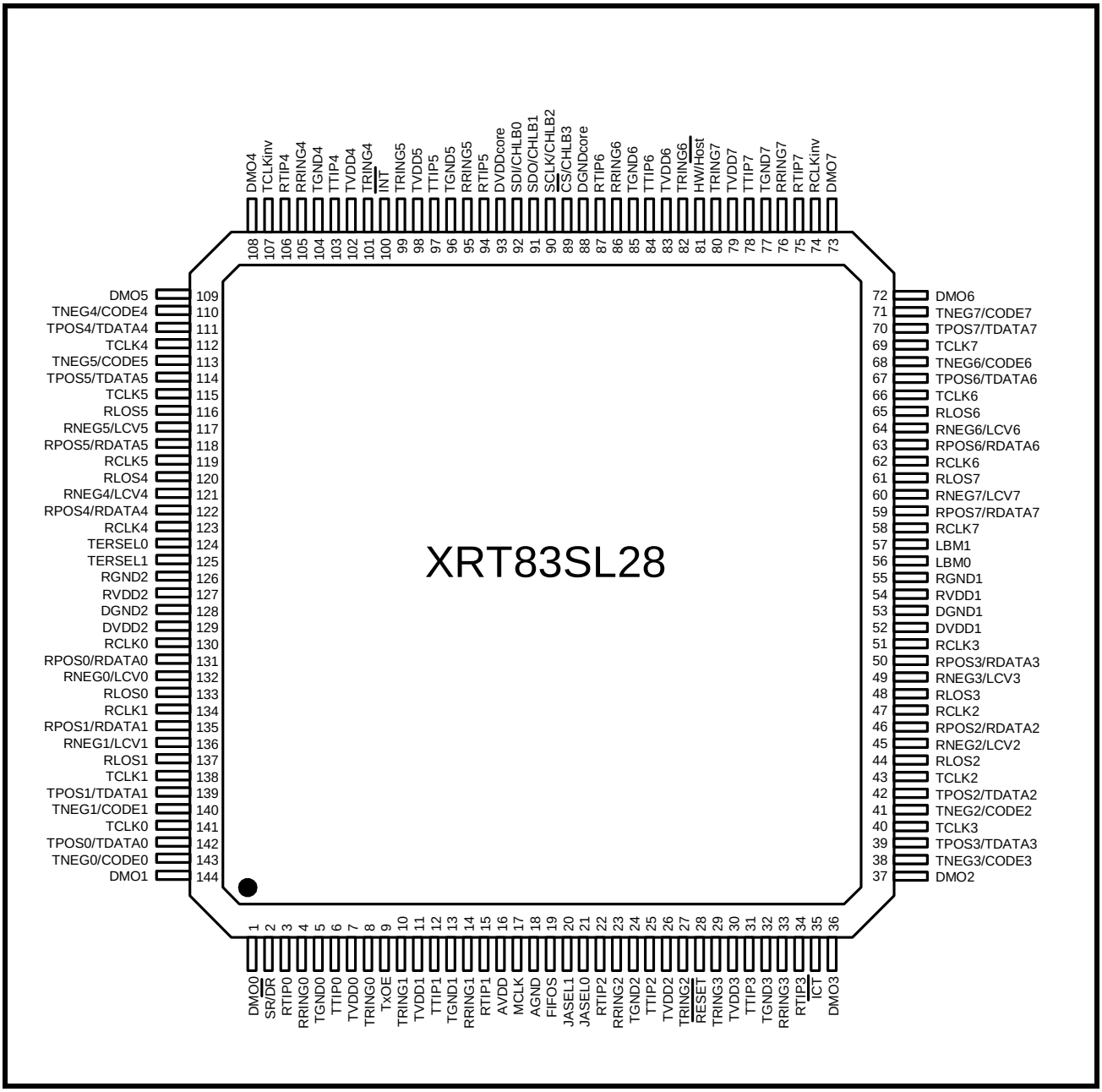
FEATURES

- Fully integrated 8-Channel short haul transceivers for E1 (2.048MHz) applications.
- Internal Impedance matching on both receive and transmit for 75Ω (E1) or 120Ω (E1) applications.
- Tri-State on a per channel basis for the transmit selection.
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis.
- Independent Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit paths
- Driver failure monitor output (DMO) alerts of possible system or external component problems.
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis.
- Support for automatic protection switching.
- 1:1 and 1+1 protection without relays.
- RLOS/AIS according to ITU-T G.775 or ETSI-300-233.
- On-Chip HDB3 encoder/decoder for each channel.
- On-Chip digital clock recovery circuit for high input jitter tolerance.
- Line code error and bipolar violation detection.
- Transmit all ones (TAOS) for the Transmit and Receive Outputs.
- Supports local analog, remote, and digital loopback modes.
- Supports gapped clocks for mapper/multiplexer applications.
- Low Power dissipation
- Single 3.3V supply operation (3V to 5V I/O tolerant).
- 144-Pin TQFP package
- -40°C to +85°C Temperature Range

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83SL28IB	144 Lead TQFP	-40°C to +85°C

FIGURE 3. PIN OUT OF THE XRT83SL28



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PIN DESCRIPTIONS

HOST MODE INTERFACE

SERIAL MICROPROCESSOR INTERFACE

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	89	I	**Chip Select Input** Active low signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial interface is disabled when the chip select signal returns "High".
SCLK	90	I	**Serial Clock Input** The serial clock input samples SDI on the rising edge and updates SDO on the falling edge. See the Serial Microprocessor section of this datasheet for more details.
SDI	92	I	**Serial Data Input** The serial data input pin is used to supply an address and data string to program the internal registers within the device. See the Serial Microprocessor section of this datasheet for more details.
SDO	91	O	**Serial Data Output** The serial data output pin is used to retrieve the internal contents of a selected register in readback mode. See the Microprocessor section of this datasheet for more details.
$\overline{Reset}$	28	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, all internal registers and state machines are set to their default state. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
$\overline{INT}$	100	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is an open-drain output that requires an external 10KΩ pull-up resistor.*
HW/$\overline{Host}$	81	I	**Hardware / Host Mode Select Input** This pin is used to select the mode of operation. By default, the LIU is configured for Hardware mode. To select Host mode, this pin must be pulled "Low". ***NOTE:*** *Internally pulled "High" with a 50kΩ resistor.*

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RLOS7 RLOS6 RLOS5 RLOS4 RLOS3 RLOS2 RLOS1 RLOS0	61 65 116 120 48 44 137 133	O	**Receive Loss of Signal** When a receive loss of signal occurs, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details.
RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	58 62 119 123 51 47 134 130	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent, RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKinv in the appropriate global register. ***NOTE:*** *RCLKinv is a global setting that applies to all 8 channels.*
RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	59 63 118 122 50 46 135 131	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.
RNEG/LCV7 RNEG/LCV6 RNEG/LCV5 RNEG/LCV4 RNEG/LCV3 RNEG/LCV2 RNEG/LCV1 RNEG/LCV0	60 64 117 121 49 45 136 132	O	**RNEG/LCV Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation indicator. If a line code violation or a bipolar violation occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	75 87 94 106 34 22 15 3	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	76 86 95 105 33 23 14 4	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxOE	9	I	**Transmit Output Enable** Upon power up, the transmitters are tri-stated. Enabling the transmitters is selected through the serial microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxOE pin is pulled "Low", all 8 transmitters are tri-stated. ***NOTE:*** *TxOE is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*
DMO7 DMO6 DMO5 DMO4 DMO3 DMO2 DMO1 DMO0	73 72 109 108 36 37 144 1	O	**Digital Monitor Output** When no transmit output pulse is detected for more than 128 TCLK cycles, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse.
TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	69 66 115 112 40 43 138 141	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKinv in the appropriate global register. ***NOTE:*** *TCLKinv is a global setting that applies to all 8 channels.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	70 67 114 111 39 42 139 142	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input.
TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	71 68 113 110 38 41 140 143	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be tied to ground.
TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	78 84 97 103 31 25 12 6	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	80 82 99 101 29 27 10 8	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
$\overline{\text{ICT}}$	35	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
MCLK	17	I	**Master Clock Input** This pin is used as the internal reference to the LIU. This clock must be 2.048MHz +/-50ppm.

POWER AND GROUND (HOST AND HARDWARE MODES)

NAME	PIN	TYPE	DESCRIPTION
TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	79 83 98 102 30 26 11 7	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.
RVDD2 RVDD1	127 54	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1µF capacitor.
DVDD2 DVDD1 DVDDcore	129 52 93	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies except for TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1µF capacitor.
AVDD	16	PWR	**Analog Power Supply (3.3V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1µF capacitor.
TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	77 85 96 104 32 24 13 5	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND2 RGND1	126 55	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND2 DGND1 DGNDcore	128 53 88	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
AGND	18	GND	**Analog Ground** It's recommended that all ground pins of this device be tied together.

HARDWARE MODE INTERFACE

NAME	PIN	TYPE	DESCRIPTION
SR/$\overline{DR}$	2	I	**Single Rail / Dual Rail Select Input** This pin is used to select Single Rail or Dual Rail data formats. By default, Dual Rail is selected. To select Single Rail mode, this pin must be pulled "High". Once this pin is pulled "High", TNEGn/CODEn can be used to select between AMI and HDB3 Encoding/Decoding. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TERSEL1 TERSEL0	125 124	I	**Termination Impedance Select** TERSEL[1:0] are used to set the internal impedance of the LIU for the Receive and Transmit paths. "00" = 75Ω for Tx and "High-Z" for Rx "01" = 120Ω for Tx and "High-Z" for Rx "10" = 75Ω for Tx and Rx "11" = 120Ω for Tx and Rx
TCLKinv	107	I	**Transmit Clock Data** "Low" = TPOS/TNEG data is sampled on the falling edge of TCLK "High" = TPOS/TNEG data is sampled on the rising edge of TCLK ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
RCLKinv	74	I	**Receive Clock Data** "Low" = RPOS/RNEG data is updated on the rising edge of RCLK "High" = RPOS/RNEG data is updated on the falling edge of RCLK ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
LBM1 LBM0	57 56	I	**Loop Back Mode Select** LBM[1:0] are used to configure the LIU into diagnostic loopback modes. To select the channel number, see pins CHLB[3:0]. "00" = None "01" = Local Analog Loop Back "10" = Remote Loop Back "11" = Digital Loop Back ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
JASEL1 JASEL0	20 21	I	**Jitter Attenuator Select** JASEL[1:0] are used to configure the jitter attenuator into the Receive or Transmit path for all eight channels. "00" = JA Disabled "01" = Transmit Path "10" = Receive Path "11" = JA Disabled ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
FIFOS	19	I	**FIFO Bit Depth Select Input** This pin is used to select the depth of the FIFO. By default, the FIFO is set to 32-Bit. To select a 64-Bit FIFO depth, this pin must be pulled "High". To meet TBR12/13 applications, the FIFO size must be set to 64-bit. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
HW/$\overline{Host}$	81	I	***Same as Host Mode.***
$\overline{Reset}$	28	I	***Same as Host Mode.***

NAME	PIN	TYPE	DESCRIPTION
CHLB3 CHLB2 CHLB1 CHLB0	89 90 91 92	I	**Channel Loop Back Select** CHLB[3:0] are used to select a particular channel or all eight channels simultaneously for Loop Back mode. See pins LBM[1:0] for selecting various types of Loop Back diagnostics. "0000" = Channel 0 "0001" = Channel 1 "0010" = Channel 2 "0011" = Channel 3 "0100" = Channel 4 "0101" = Channel 5 "0110" = Channel 6 "0111" = Channel 7 "1111" = All Eight Channels ***NOTE:*** *CHLB3 (Pin 89) is internally pulled "High" with a 50kΩ Resistor.*
RLOS7 RLOS6 RLOS5 RLOS4 RLOS3 RLOS2 RLOS1 RLOS0	61 65 116 120 48 44 137 133	O	***Same as Host Mode.***
RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	58 62 119 123 51 47 134 130	O	***Same as Host Mode.***
RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	59 63 118 122 50 46 135 131	O	***Same as Host Mode.***
RNEG/LCV7 RNEG/LCV6 RNEG/LCV5 RNEG/LCV4 RNEG/LCV3 RNEG/LCV2 RNEG/LCV1 RNEG/LCV0	60 64 117 121 49 45 136 132	O	***Same as Host Mode.***

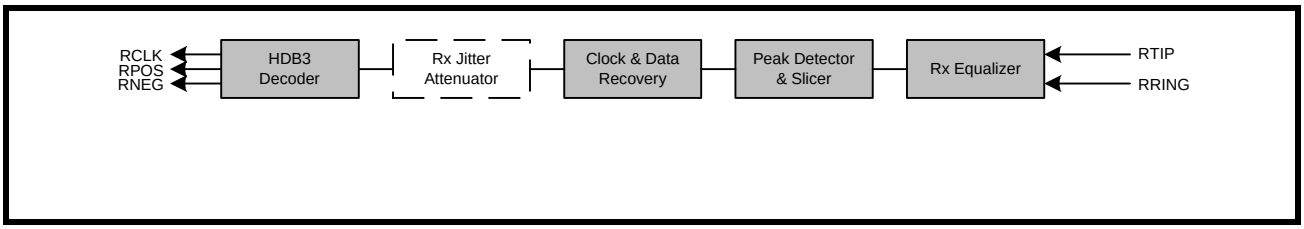
NAME	PIN	TYPE	DESCRIPTION
RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	75 87 94 106 34 22 15 3	I	***Same as Host Mode.***
RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	76 86 95 105 33 23 14 4	I	***Same as Host Mode.***
TXOE	9	I	**Transmit Output Enable (Global Pin for All 8 Channels)** Upon power up, the transmitters are tri-stated. Enabling the transmitters is controlled by pulling the TXOE hardware pin "High". If the TxOE pin is pulled "Low", all 8 transmitters are tri-stated. ***NOTE:*** *TxOE is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50KΩ resistor.*
DMO7 DMO6 DMO5 DMO4 DMO3 DMO2 DMO1 DMO0	73 72 109 108 36 37 144 1	O	***Same as Host Mode.***
TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	69 66 115 112 40 43 138 141	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is pulled "Low" for 16 MCLK cycles, the transmitter outputs at TTIP/TRING are tri-stated. If TCLK is pulled "High" for 16 MCLK cycles, the transmitter outputs at TTIP/TRING will send an All Ones pattern. TPOS/TNEG data can be sampled on either edge of TCLK selected by the TCLKinv pin. ***NOTE:*** *The TCLKinv pin is a global setting that applies to all 8 channels.*

NAME	PIN	TYPE	DESCRIPTION
TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	70 67 114 111 39 42 139 142	I	***Same as Host Mode.***
TNEG7/CODE7 TNEG6/CODE6 TNEG5/CODE5 TNEG4/CODE4 TNEG3/CODE3 TNEG2/CODE2 TNEG1/CODE1 TNEG0/CODE0	71 68 113 110 38 41 140 143	I	**Transmit Negative Data / CODE Select Input** TNEG has the same definition as Host Mode. However, in Hardware mode and Single Rail Data Format, this pin is used to select between AMI and HDB3 Encoder/Decoder. By default, HDB3 is selected. To select AMI, this pin must be pulled "High". ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	78 84 97 103 31 25 12 6	O	***Same as Host Mode.***
TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	80 82 99 101 29 27 10 8	O	***Same as Host Mode.***
$\overline{ICT}$	35	I	***Same as Host Mode.***
MCLK	17	I	***Same as Host Mode.***

1.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83SL28 LIU consists of 8 independent E1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in Figure 4.

FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH LINE TERMINATION (RTIP/RRING)



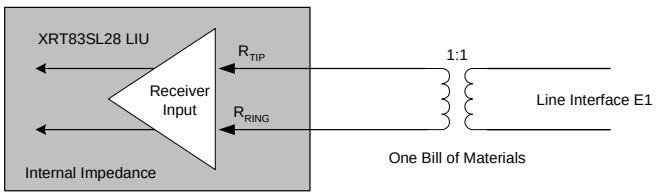
1.1 Internal Termination

The input stage of the receive path accepts standard E1 coaxial cable or E1 twisted pair inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL[1:0] to match the line impedance. The XRT83SL28 has the ability to switch the internal termination to "High" impedance for redundancy applications. See Redundancy in the Applications Section of this datasheet. Selecting the internal impedance is shown in Table 1. A typical connection diagram is shown in Figure 5.

TABLE 1: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	RECEIVE TERMINATION
0h (00)	75Ω for Tx and "High-Z" for Rx
1h (01)	120Ω for Tx and "High-Z" for Rx
2h (10)	75Ω for Tx and Rx
3h (11)	120Ω for Tx and Rx

FIGURE 5. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



1.2 Pead Detector

The main objective of the receiver block is to amplify an input attenuated signal to a pre-determined amplitude that is acceptable to the peak detector circuit. An amplifier will gain the input up to 15dB which is the maximum value specified by the receiver capability, normalizing the signal. Once the signal has reached the pre-determined amplitude, the signal is then processed within the peak detector and slicer circuit.

1.3 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel E1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKinv to "1" in the appropriate global register. Figure 6 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 7 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 2.

FIGURE 6. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

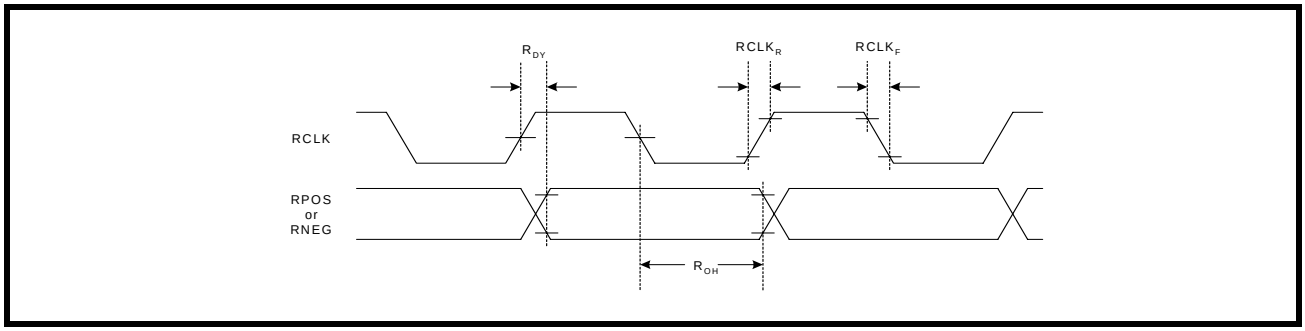


FIGURE 7. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

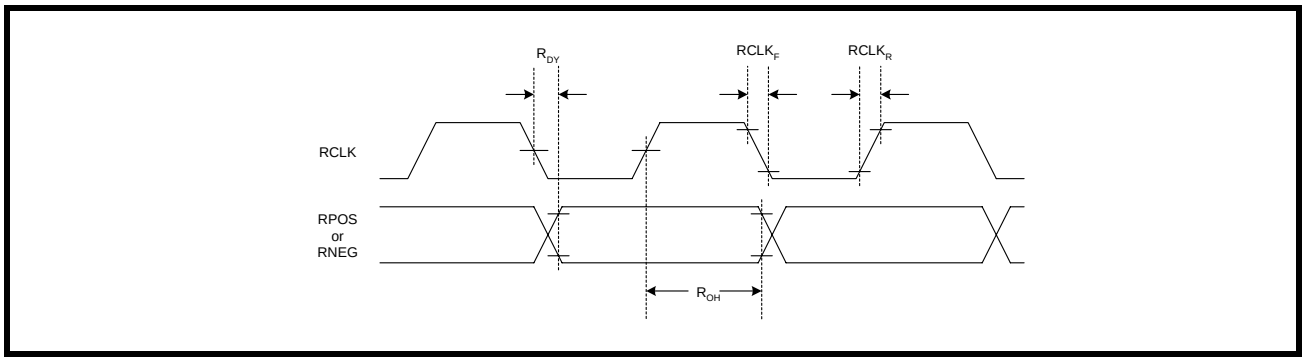


TABLE 2: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

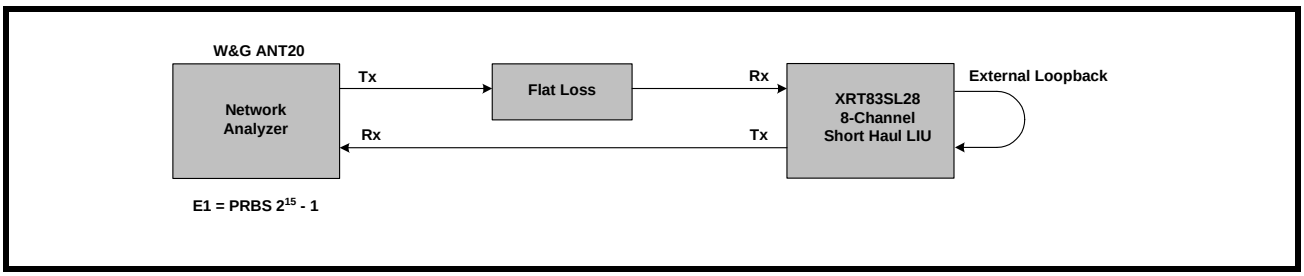
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

1.4 Receive Sensitivity

To meet short haul requirements, the XRT83SL28 can accept E1 signals that have been attenuated by 9dB of flat loss in E1 mode. The test configuration for measuring the receive sensitivity is shown in Figure 8.

FIGURE 8. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



1.5 General Alarm Detection and Interrupt Generation

The receive path detects RLOS and AIS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (if the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the $\overline{INT}$ pin will return "High". The status registers are Reset Upon Read (RUR).

NOTE: *The interrupt pin is an Open-Drain output that requires a 10kΩ pull-up resistor.*

1.5.1 RLOS (Receiver Loss of Signal)

The XRT83SL28 adheres to ITU-T G.775 or ETSI-300-233 specifications for an RLOS condition by programming the appropriate channel register. RLOS is declared if an incoming signal has no transitions for N consecutive pulse intervals, where 10≤N≤255. According to G.775, no transitions in E1 mode is defined between -9dB and -35dB below nominal. According to ETS-300-233, LOS should be declared if the input is attenuated by -20dB for at least 1mS. The XRT83SL28 LIU has a built in analog RLOS so that the user can be notified when the amplitude of the incoming signal has been attenuated -20dB below nominal.

NOTE: *In Hardware mode, RLOS adheres to ITU-T G.775 only.*

1.5.2 AIS (Alarm Indication Signal)

The XRT83SL28 adheres to ITU-T G.775 or ETSI-300-233 specifications for an all ones pattern by programming the appropriate channel register. The alarm indication signal is set to "1" if an all ones pattern is detected. According to G.775, AIS is defined as 2 or less zeros in 2 consecutive double frame (512-bit window) periods . AIS will clear when the incoming signal has 3 or more zeros in the same time period. According to ETSI-300-233, AIS is defined as less than 3 zeros in a 512-bit window.

NOTE: *In Hardware mode, AIS adheres to ITU-T G.775 only.*

1.5.3 LCV (Line Code Violation Detection)

By default, the LCV will be set to a "1" if the receiver is currently detecting line code violations in HDB3. In AMI mode, the LCV will be set to a "1" if the receiver is currently detecting bipolar violations.

1.6 Receive Jitter Attenuator

The jitter attenuator can be configured in the receive path to reduce phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. The bandwidth is set to 2Hz when the JA is configured in the Receive or Transmit path. The JA has a typical clock delay equal to ½ of the FIFO bit depth.

NOTE: *If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the JA can be configured in the transmit path to smooth out the gapped clock. See the Transmit Section of this datasheet.*

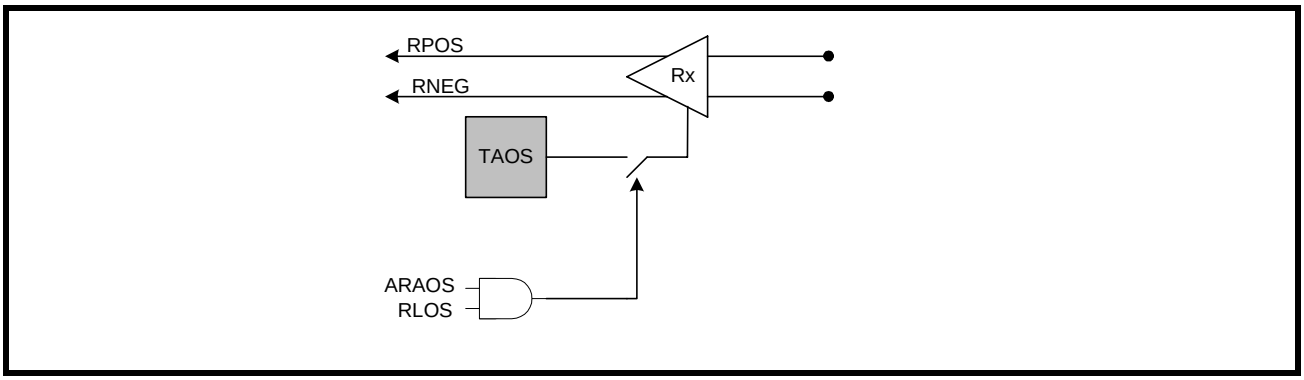
1.7 HDB3 Decoder

In single rail mode, RPOS can decode AMI or HDB3 signals. HDB3 is defined as any block of 4 successive zeros replaced with OOOV or BOOV, so that two successive V pulses are of opposite polarity to prevent a DC component. If the HDB3 decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

1.8 ARAOS (Automatic Receive All Ones)

The XRT83SL28 has the ability to send an All Ones signal to RPOS if ARAOS is enabled in the appropriate channel register. If ARAOS is enabled and an RLOS condition occurs, the Receiver outputs will generate a single rail All Ones pattern. When RLOS clears, the All Ones pattern ends and the Receive path returns to normal operation. For TAOS in the transmit direction, see the Transmit Section of this datasheet. A simplified block diagram of the ATAOS function is shown in Figure 9.

FIGURE 9. IMPLIFIED BLOCK DIAGRAM OF THE ARAOS FUNCTIONRPOS/RNEG/RCLK



1.9 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. Figure 10 is a timing diagram of a repeating "0011" pattern in single-rail mode. Figure 11 is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 10. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

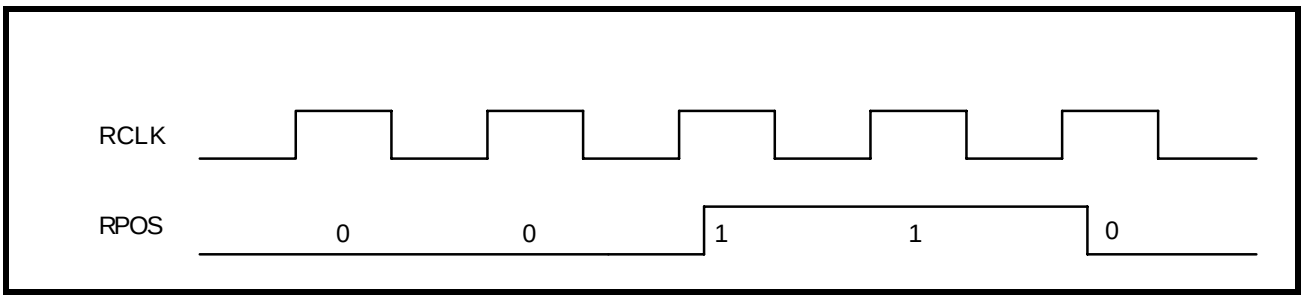
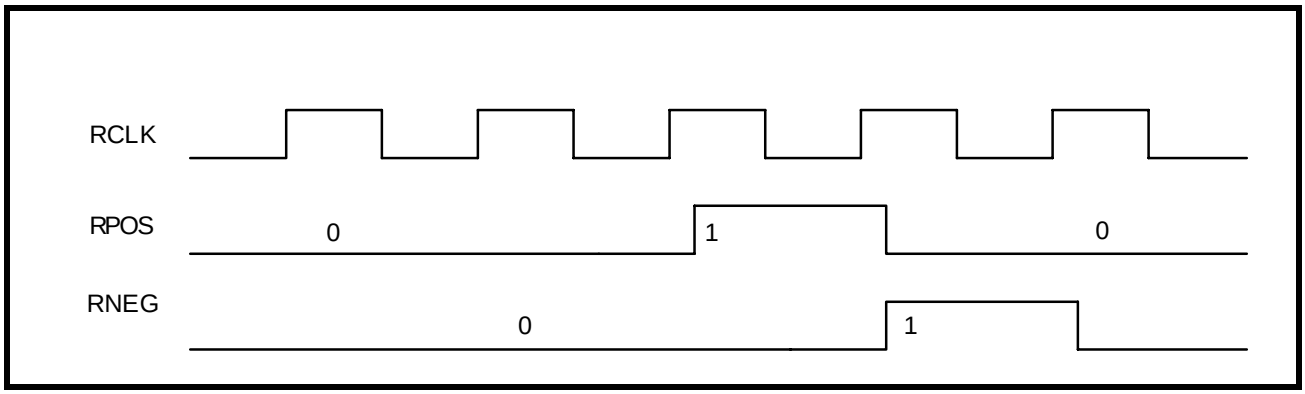


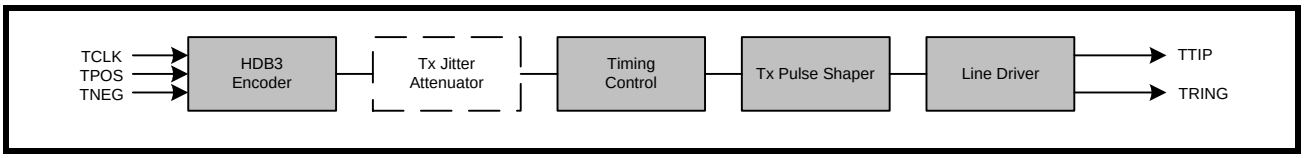
FIGURE 11. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



2.0 TRANSMIT PATH LINE INTERFACE

The transmit path of the XRT83SL28 LIU consists of 8 independent E1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. A simplified block diagram of the transmit path is shown in Figure 12.

FIGURE 12. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



2.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG can be tied to ground unless Hardware mode is selected (see the Hardware Pin Description). The XRT83SL28 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLKinv to "1" in the appropriate global register. Figure 13 is a timing diagram of the transmit input data sampled on the falling edge of TCLK. Figure 14 is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in Table 3.

FIGURE 13. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

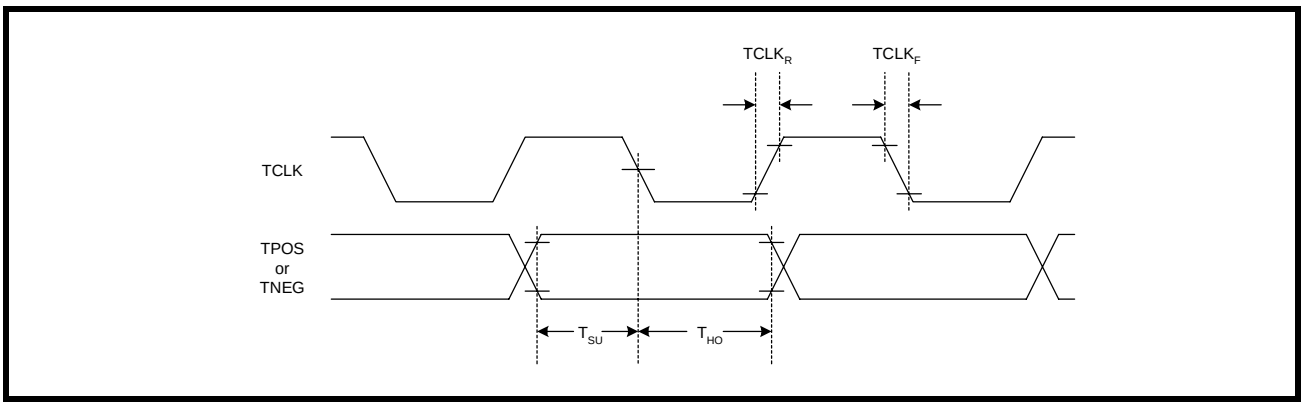


FIGURE 14. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

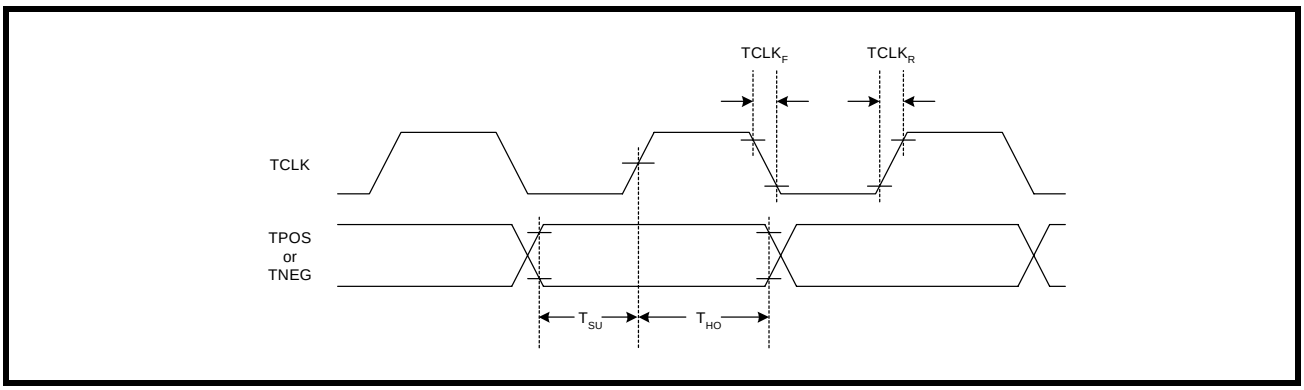


TABLE 3: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TCLK Rise Time (10% to 90%)	$TCLK_R$	-	-	40	ns
TCLK Fall Time (90% to 10%)	$TCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified*

2.2 HDB3 Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3 data. If HDB3 encoding is selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in Table 4.

TABLE 4: EXAMPLES OF HDB3 ENCODING

	NUMBER OF PULSES BEFORE NEXT 4 ZEROS	
Input		0000
HDB3 (Case 1)	Odd	000V
HDB3 (Case 2)	Even	B00V

2.3 Transmit Jitter Attenuator

The XRT83SL28 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed to E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The JA can be configured in the transmit path with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady E1 output. The maximum gap width the JA in the Transmit path can tolerate is shown in Table 5.

TABLE 5: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

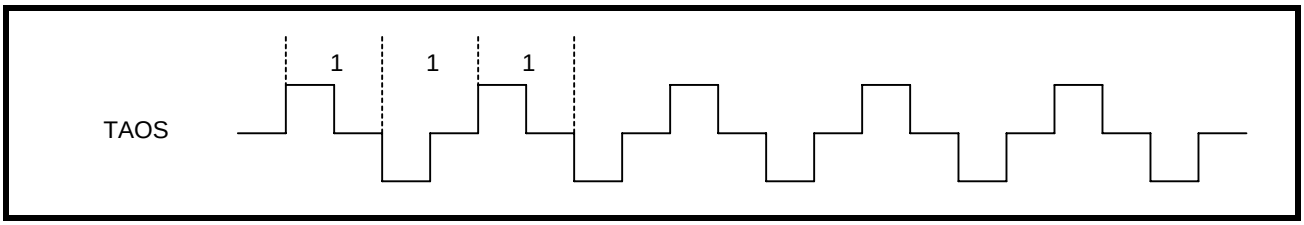
FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the JA should be configured in the receive path. See the Receive Section of this datasheet.*

2.4 TAOS (Transmit All Ones)

The XRT83SL28 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. If TAOS is enabled, the Transmitter outputs will generate an All Ones pattern regardless of the Transmit Input data. The Remote Loop Back mode is the only function that takes priority over TAOS. Figure 15 is a diagram showing the all ones signal at TTIP and TRING.

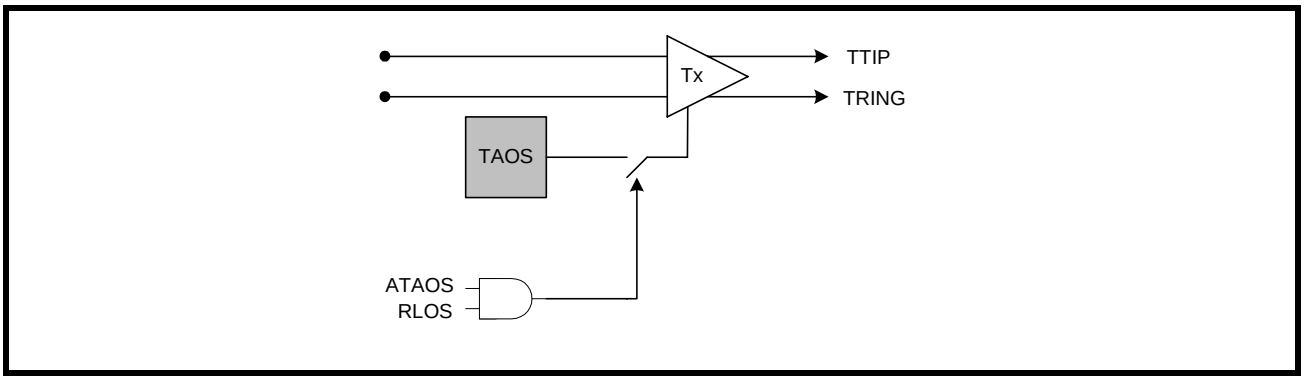
FIGURE 15. TAOS (TRANSMIT ALL ONES)ATAOS (AUTOMATIC TRANSMIT ALL ONES)



2.5 ATAOS (Automatic Transmit All Ones)

Unlike TAOS, ATAOS is used to generate an All Ones signal only when an RLOS condition occurs. If ATAOS is enabled, any channel that experiences an RLOS condition will automatically cause the transmitter on that channel to send an all ones pattern to the line. When RLOS clears, the All Ones pattern ends and the Transmit path returns to normal operation. For TAOS on the receive output pins, see ARAOS in the Receive Section of this datasheet. A simplified block diagram of the ATAOS function is shown in Figure 16.

FIGURE 16. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



2.6 Transmit Pulse Shaper and Filter

If TCLK is pulled "Low" for 16 MCLK cycles the transmitter outputs at TTIP/TRING are tri-stated. If TCLK is pulled "High" for 16 MCLK cycles the transmitter outputs at TTIP/TRING will send an All Ones signal.

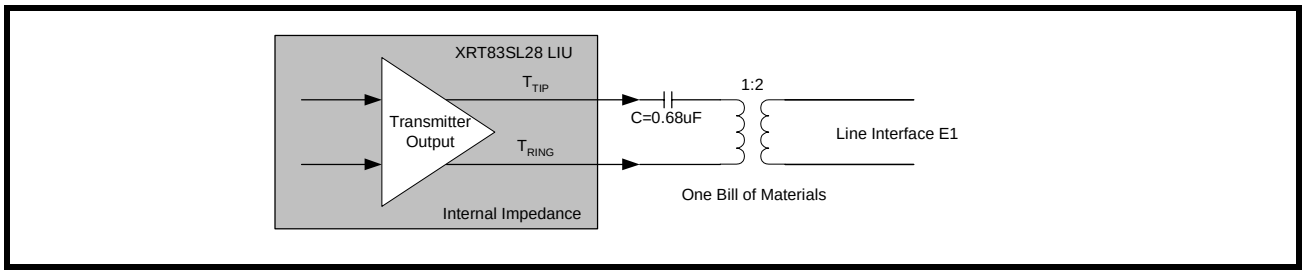
2.7 DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 TCLK cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

2.8 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for E1 coaxial cable or E1 twisted pair. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68μF. A typical transmit interface is shown in Figure 17.

FIGURE 17. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



3.0 E1 APPLICATIONS

This applications section describes common E1 system considerations along with references to application notes available for reference where applicable.

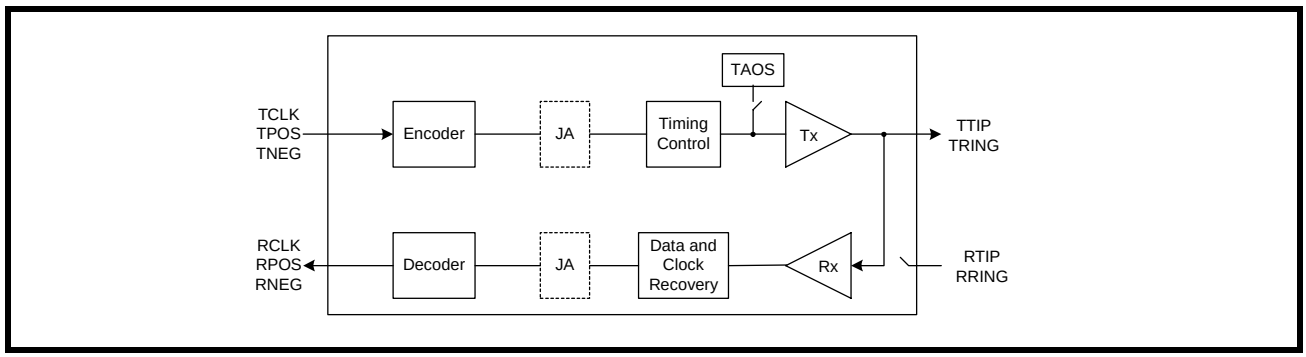
3.1 Loopback Diagnostics

The XRT83SL28 supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, and digital loopback.

3.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTIP/TRING is internally looped back to the analog inputs at RTIP/RRING. External inputs at RTIP/RRING are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in Figure 18.

FIGURE 18. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK

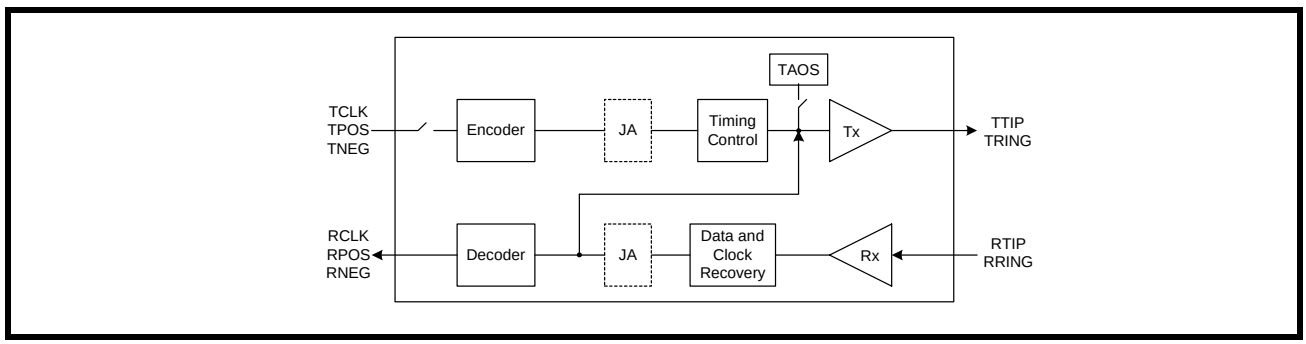


NOTE: *TAOS takes priority over the transmit input data at TPOS/TNEG.*

3.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTIP/RRING is internally looped back to the transmit output data at TTIP/TRING. The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in Figure 19.

FIGURE 19. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK

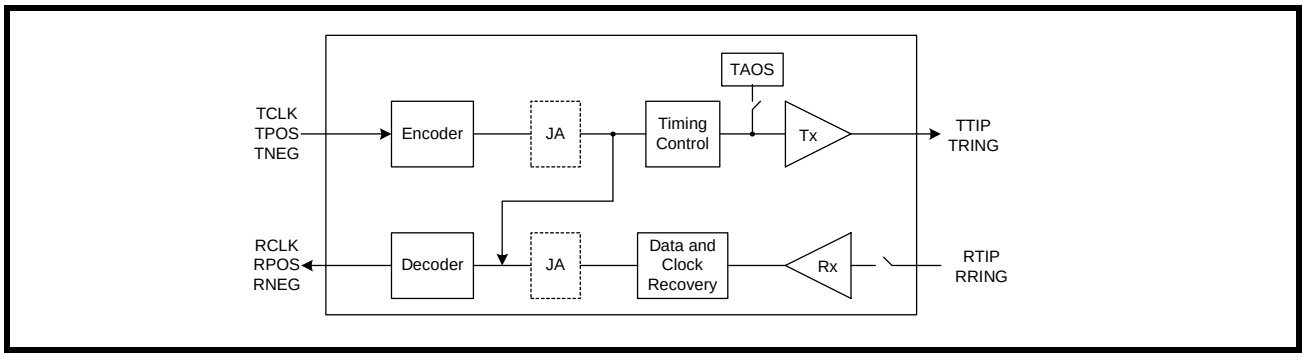


NOTE: *Remote Loop Back takes priority over TAOS.*

3.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG. The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in Figure 20.

FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



3.2 Line Card Redundancy

Telecommunication system design requires signal integrity and reliability. When an E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT83SL28 LIU. EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

RLOS and DMO

If an RLOS or DMO condition occurs, the XRT83SL28 reports the alarm to the individual status registers on a per channel basis. However, for redundancy applications, RLOS and DMO pins can be used to initiate an automatic switch to the back up card.

Typical Redundancy Schemes

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- ·N+1 One backup card for N primary cards

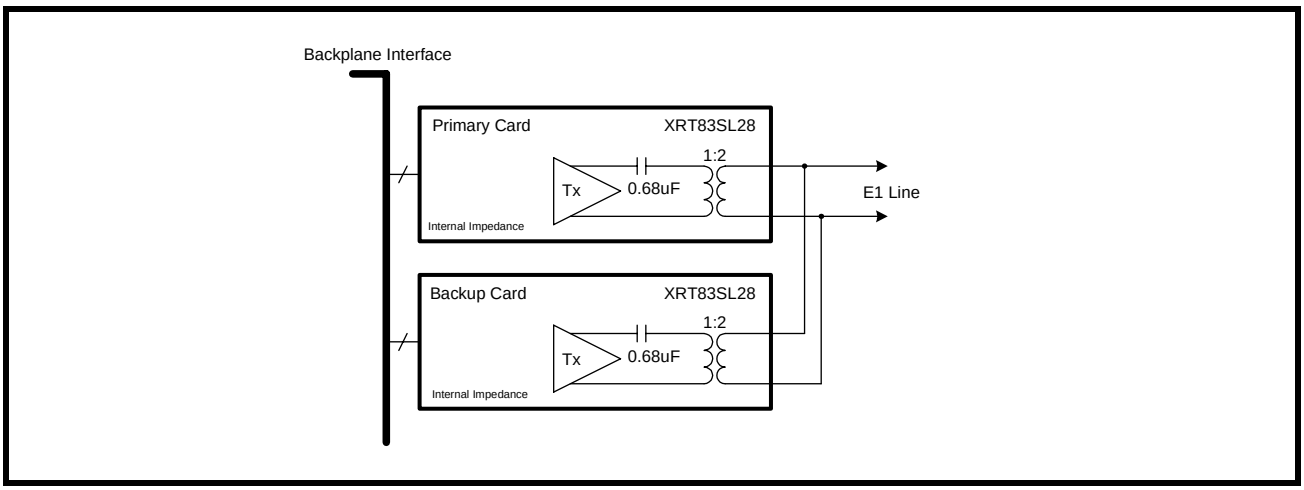
3.2.1 1:1 and 1+1 Redundancy Without Relays

The 1:1 facility protection and 1+1 line protection have one backup card for every primary card. When using 1:1 or 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. For 1+1 line protection, the receiver inputs on the backup card have the ability to monitor the line for bit errors while in high impedance. The transmit and receive sections of the LIU device are described separately.

3.2.2 Transmit Interface with 1:1 and 1+1 Redundancy

The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, E1 75Ω or 120Ω. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 21. for a simplified block diagram of the transmit section for a 1:1 and 1+1 redundancy.

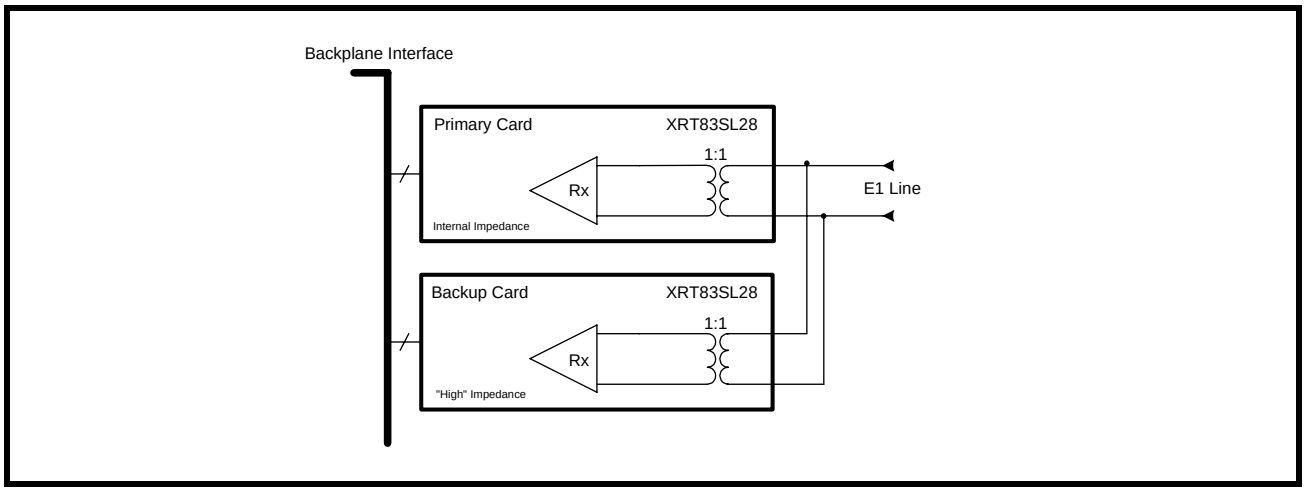
FIGURE 21. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



3.2.3 Receive Interface with 1:1 and 1+1 Redundancy

The receivers on the backup card should be programmed for "High" impedance. Since there is no external resistor in the circuit, the receivers on the backup card will not load down the line interface. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, E1 75Ω or 120Ω. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See Figure 22. for a simplified block diagram of the receive section for a 1:1 redundancy scheme.

FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



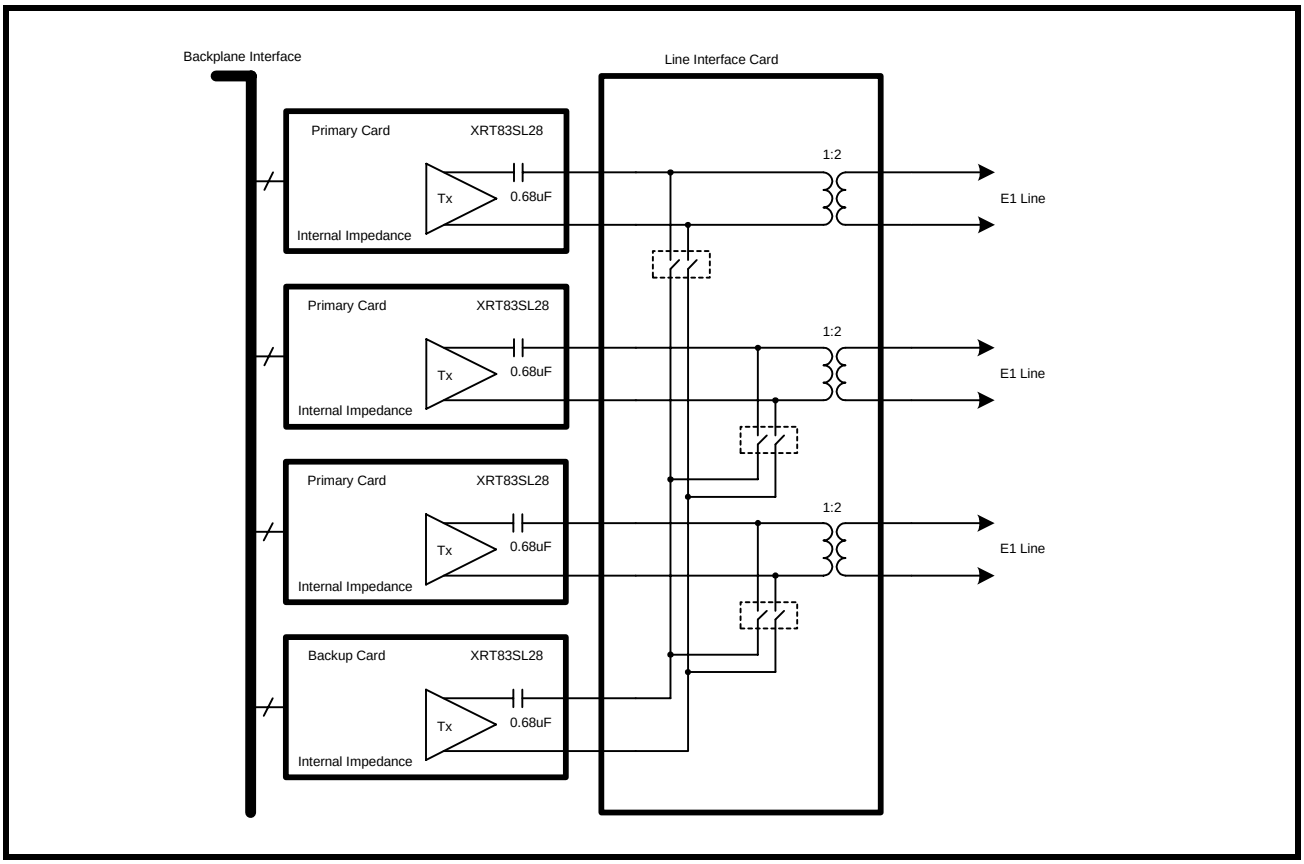
3.2.4 N+1 Redundancy Using External Relays

N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. The relays create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in internal impedance, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

3.2.5 Transmit Interface with N+1 Redundancy

For N+1 redundancy, the transmitters on all cards can be programmed for internal impedance. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 23 for a simplified block diagram of the transmit section for an N+1 redundancy scheme.

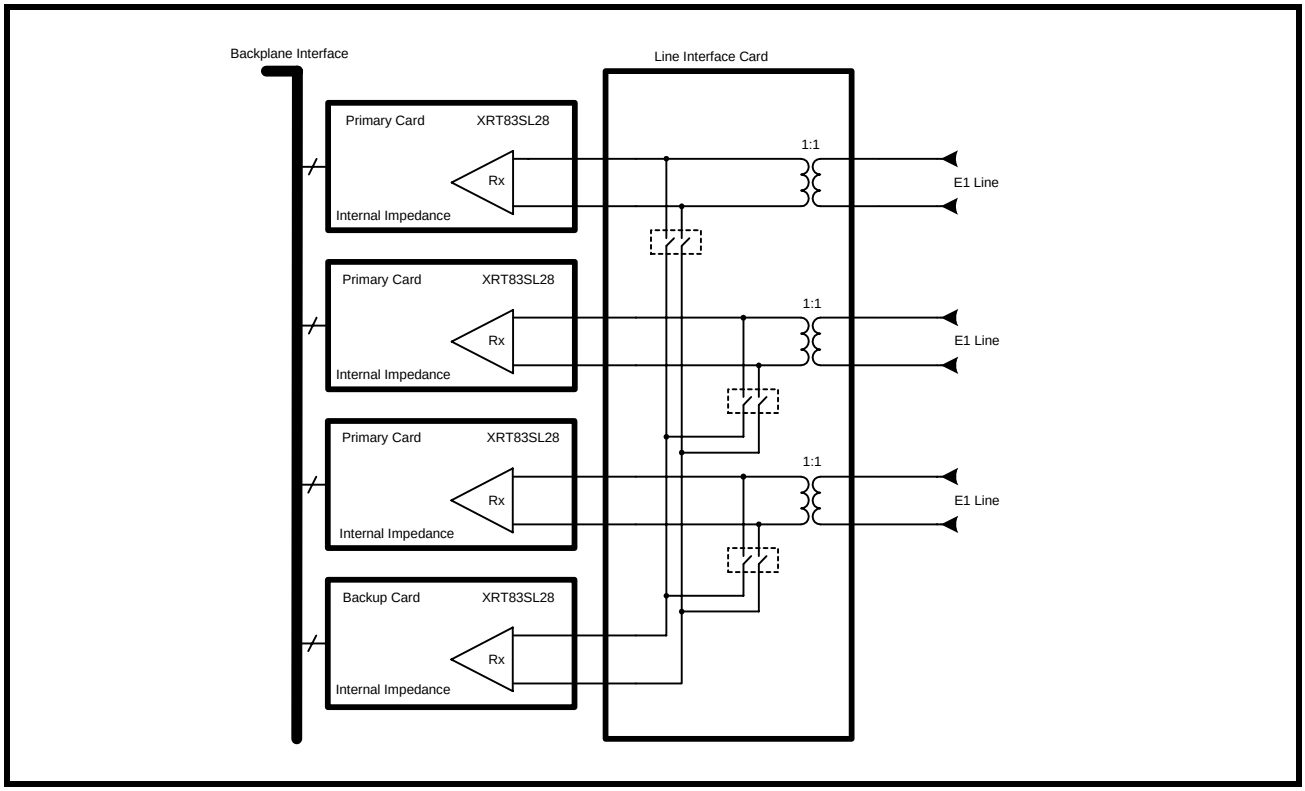
FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY



3.2.6 Receive Interface with N+1 Redundancy

For N+1 redundancy, the receivers on all cards can be programmed for internal impedance. The receivers on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays. See Figure Figure 24 for a simplified block diagram of the receive section for an N+1 redundancy scheme.

FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY



3.3 Power Failure Protection

For 1:1 or 1+1 line card redundancy in E1 applications, power failure could cause a line card to change the characteristics of the line impedance, causing a degradation in system performance. The XRT83SL28 is designed to ensure reliability during power failures. The LIU has patented high impedance circuits that allow the receiver inputs and the transmitter outputs to be in "High" impedance when the LIU experiences a power failure or when the LIU is powered off.

NOTE: *For power failure protection, a transformer must be used to couple to the line interface. See the TAN-56 application note for more details.*

3.4 Overvoltage and Overcurrent Protection

Physical layer devices such as LIUs that interface to telecommunications lines are exposed to overvoltage transients posed by environmental threats. An Overvoltage transient is a pulse of energy concentrated over a small period of time, usually under a few milliseconds. These pulses are random and exceed the operating conditions of CMOS transceiver ICs. Electronic equipment connecting to data lines are susceptible to many forms of overvoltage transients such as lightning, AC power faults and electrostatic discharge (ESD). There are three important standards when designing a telecommunications system to withstand overvoltage transients.

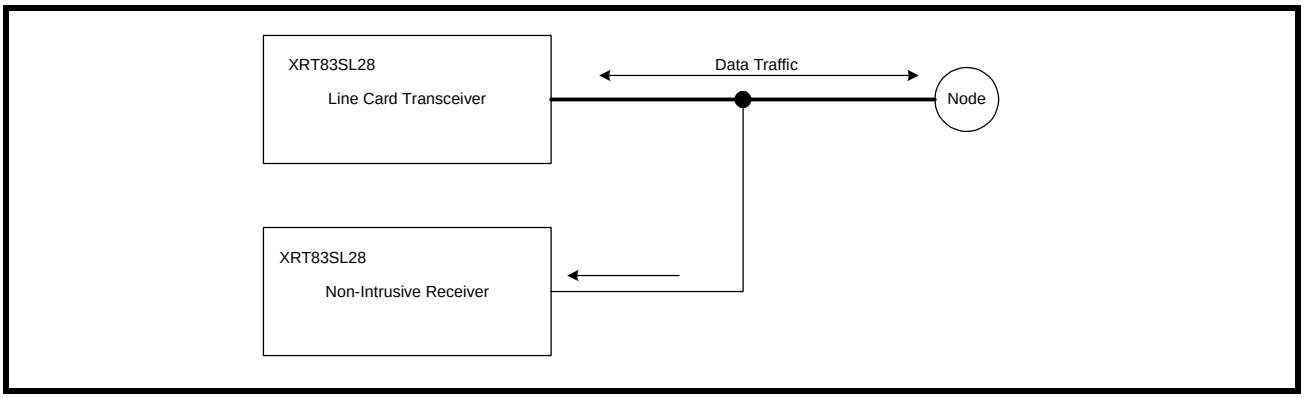
- UL1950 and FCC Part 68
- Telcordia (Bellcore) GR-1089
- ITU-T K.20, K.21 and K.41

NOTE: For a reference design and performance, *see the TAN-54 application note for more details.*

3.5 Non-Intrusive Monitoring

In non-intrusive monitoring applications, the transmitters are shut off by setting TxON "Low". The receivers must be actively receiving data without interfering with the line impedance. The XRT83SL28's internal termination ensures that the line termination meets E1 specifications for 75Ω or 120Ω while monitoring the data stream. System integrity is maintained by placing the non-intrusive receiver in "High" impedance, equivalent to that of a 1+1 redundancy application. A simplified block diagram of non-intrusive monitoring is shown in Figure 25.

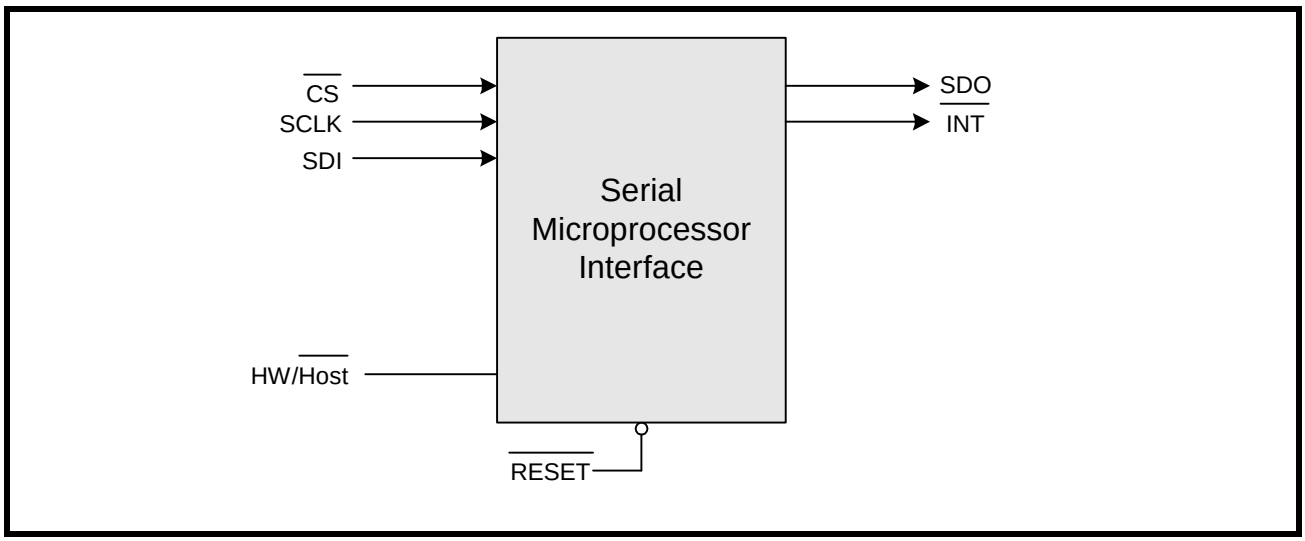
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION



4.0 SERIAL MICROPROCESSOR INTERFACE BLOCK

The serial microprocessor uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the LIU. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the LIU via an interrupt pin, and reset the LIU to its default configuration by pulling reset "Low" for more than 10µS. A simplified block diagram of the Serial Microprocessor is shown in Figure 26.

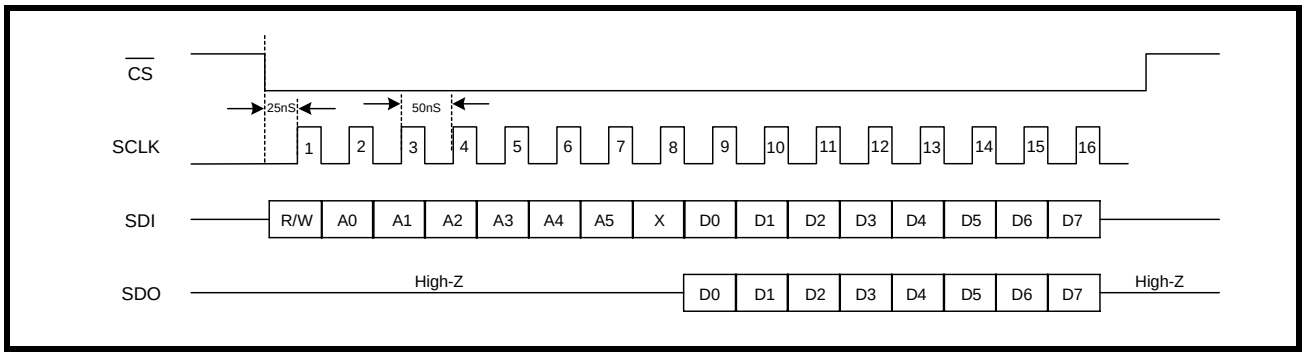
FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



4.1 SERIAL TIMING INFORMATION

The serial port requires 16 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 16 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in Figure 27.

FIGURE 27. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



4.2 16-BIT SERIAL DATA INPUT DESCRITPTION

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the LIU LSB first. The 16 bits of serial data are described below.

4.2.1 R/W (SCLK1)

The first serial bit applied to the LIU informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to "0", the microprocessor is configured for a Write operation. If the R/W bit is set to "1", the microprocessor is configured for a Read operation.

4.2.2 A[5:0] (SCLK2 - SCLK7)

The next 6 SCLK cycles are used to provide the address to which a Read or Write operation will occur. A0 (LSB) must be sent to the LIU first followed by A1 and so forth until all 6 address bits have been sampled by SCLK.

4.2.3 X (Dummy Bit SCLK8)

The dummy bit sampled by SCLK8 is used to allow sufficient time for the serial data output pin to update data if the readback mode is selected by setting R/W = "1". Therefore, the state of this bit is ignored and can hold either "0" or "1" during both Read and Write operations.

4.2.4 D[7:0] (SCLK9 - SCLK16)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. D0 (LSB) must be sent to the LIU first followed by D1 and so forth until all 8 data bits have been sampled by SCLK. Once 16 SCLK cycles have been complete, the LIU holds the data until $\overline{CS}$ is pulled "High" whereby, the serial microprocessor latches the data into the selected internal register.

4.3 8-BIT SERIAL DATA OUTPUT DESCRIPTION

The serial data output is updated on the falling edge of SCLK9 - SCLK16 if R/W is set to "1". D0 (LSB) is provided on SCLK9 to the SDO pin first followed by D1 and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

TABLE 6: MICROPROCESSOR REGISTER DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Global Control Register for All 8 Channels (0x00h)										
0	0x00	R/W	GIE	SR/DR	CODE	RCLKinv	TCLKinv	FIFO	JASEL1	JASEL0
1	0x01	RO	**Revision ID (See Bit Description)**							
2	0x02	RO	**Device ID (See Bit Description)**							
3	0x03	R/W	**For Internal Use Only**							TSTEN
Channel 0 Control Register (0x04h - 0x07h)										
4	0x04	R/W	Reserved	RLAM0	ARAOS0	ATAOS0	TAOS0	TXOE0	TERSEL1	TERSEL0
5	0x05	R/W	Reserved	SRESET0	AISIE0	DMOIE0	RLOSIE0	Reserved	LB1	LB0
6	0x06	RUR	Reserved	Reserved	AISI0	DMOI0	RLOSI0	Reserved	Reserved	Reserved
7	0x07	RO	Reserved	Reserved	AISS0	DMOS0	RLOSS0	Reserved	Reserved	Reserved
Channel 1 Control Register (0x08h - 0x0Bh)										
8	0x08	RO	Reserved	RLAM1	ARAOS1	ATAOS1	TAOS1	TXOE1	TERSEL1	TERSEL0
9	0x09	R/W	Reserved	SRESET1	AISIE1	DMOIE1	RLOSIE1	Reserved	LB1	LB0
10	0x0A	RUR	Reserved	Reserved	AISI1	DMOI1	RLOSI1	Reserved	Reserved	Reserved
11	0x0B	RO	Reserved	Reserved	AISS1	DMOS1	RLOSS1	Reserved	Reserved	Reserved
Channel 2 Control Register (0x0Ch - 0x0Fh)										
12	0x0C	R/W	Reserved	RLAM2	ARAOS2	ATAOS2	TAOS2	TXOE2	TERSEL1	TERSEL0
13	0x0D	R/W	Reserved	SRESET2	AISIE2	DMOIE2	RLOSIE2	Reserved	LB1	LB0
14	0x0E	RUR	Reserved	Reserved	AISI2	DMOI2	RLOSI2	Reserved	Reserved	Reserved
15	0x0F	RO	Reserved	Reserved	AISS2	DMOS2	RLOSS2	Reserved	Reserved	Reserved
Channel 3 Control Register (0x10h - 0x13h)										
16	0x10	R/W	Reserved	RLAM3	ARAOS3	ATAOS3	TAOS3	TXOE3	TERSEL1	TERSEL0
17	0X11	R/W	Reserved	SRESET3	AISIE3	DMOIE3	RLOSIE3	Reserved	LB1	LB0
18	0x12	RUR	Reserved	Reserved	AISI3	DMOI3	RLOSI3	Reserved	Reserved	Reserved
19	0x13	RO	Reserved	Reserved	AISS3	DMOS3	RLOSS3	Reserved	Reserved	Reserved
Channel 4 Control Register (0x14h - 0x17h)										
20	0x14	R/W	Reserved	RLAM4	ARAOS4	ATAOS4	TAOS4	TXOE4	TERSEL1	TERSEL0
21	0x15	R/W	Reserved	SRESET4	AISIE4	DMOIE4	RLOSIE4	Reserved	LB1	LB0
22	0x16	RUR	Reserved	Reserved	AISI4	DMOI4	RLOSI4	Reserved	Reserved	Reserved
23	0x17	RO	Reserved	Reserved	AISS4	DMOS4	RLOSS4	Reserved	Reserved	Reserved
Channel 5 Control Register (0x18h - 0x1Bh)										
24	0x18	R/W	Reserved	RLAM3	ARAOS5	ATAOS5	TAOS5	TXOE5	TERSEL1	TERSEL0
25	0x19	R/W	Reserved	SRESET5	AISIE5	DMOIE5	RLOSIE5	Reserved	LB1	LB0

TABLE 6: MICROPROCESSOR REGISTER DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
26	0x1A	RUR	Reserved	Reserved	AISI5	DMOI5	RLOSI5	Reserved	Reserved	Reserved
27	0X1B	RO	Reserved	Reserved	AISS5	DMOS5	RLOSS5	Reserved	Reserved	Reserved
Channel 6 Control Register (0x1Ch - 0x1Fh)										
28	0x1C	R/W	Reserved	RLAM6	ARAOS6	ATAOS6	TAOS6	TXOE6	TERSEL1	TERSEL0
29	0x1D	R/W	Reserved	SRESET6	AISIE6	DMOIE6	RLOSIE6	Reserved	LB1	LB0
30	0x1E	RUR	Reserved	Reserved	AISI6	DMOI6	RLOSI6	Reserved	Reserved	Reserved
31	0X1F	RO	Reserved	Reserved	AISS6	DMOS6	RLOSS6	Reserved	Reserved	Reserved
Channel 7 Control Register (0x20h - 0x23h)										
32	0x20	R/W	Reserved	RLAM7	ARAOS7	ATAOS7	TAOS7	TXOE7	TERSEL1	TERSEL0
33	0x21	R/W	Reserved	SRESET7	AISIE7	DMOIE7	RLOSIE7	Reserved	LB1	LB0
34	0x22	RUR	Reserved	Reserved	AISI7	DMOI7	RLOSI7	Reserved	Reserved	Reserved
35	0X23	RO	Reserved	Reserved	AISS7	DMOS7	RLOSS7	Reserved	Reserved	Reserved

TABLE 7: MICROPROCESSOR REGISTER 0X00H BIT DESCRIPTION

GLOBAL CONTROL REGISTER FOR ALL 8 CHANNELS (0X00H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	GIE	**Global Interrupt Enable** The global interrupt enable is used to enable/disable all interrupt activity for all 8 channels. This bit must be set "High" for the interrupt pin to operate. "0" = Disable all interrupt generation "1" = Enable interrupt generation to the individual channel registers	R/W	0
D6	SR/DR	**Single Rail / Dual Rail Select** This bit is used to configure the receive outputs and transmit inputs to single rail or dual rail data formats. "0" = Dual Rail "1" = Single Rail	R/W	0
D5	CODE	**Encoding / Decoding Select (Single Rail Mode Only)** This bit is used to select between AMI or HDB3. "0" = HDB3 "1" = AMI	R/W	0
D4	RCLKinv	**Receiver Clock Data** "0" = RPOS/RNEG data is updated on the rising edge of RCLK "1" = RPOS/RNEG data is updated on the falling edge of RCLK	R/W	0
D3	TCLKinv	**Transmitter Clock Data** "0" = TPOS/TNEG data is sampled on the falling edge of TCLK "1" = TPOS/TNEG data is sampled on the rising edge of TCLK	R/W	0
D2	FIFOS	**FIFO Depth Select** The FIFO depth select is used to configure the part for a 32-bit or 64-bit FIFO (Within the Jitter Attenuator Block). The delay of the FIFO is typically equal to ½ the FIFO depth. "0" = 32-bit FIFO "1" = 64-bit FIFO	R/W	0
D1 D0	JASEL1 JASEL0	**Jitter Attenuator Select** These bits are used to configure the Jitter Attenuator into the Receive or Transmit path. "00" = Disabled "01" = Transmit Path "10" = Disabled "11" = Receive Path	R/W	0 0

TABLE 8: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

REVISION "ID" REGISTER (0X01H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Revision "ID"	The revision "ID" of the XRT83SL28 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon (Revision A) will be 0x01h.	RO	0
D6				0
D5				0
D4				0
D3				0
D2				0
D1				0
D0				1

TABLE 9: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

DEVICE "ID" REGISTER (0X02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Device "ID"	The device "ID" of the XRT83SL28 LIU is 0xF7h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1
D6				1
D5				1
D4				1
D3				0
D2				1
D1				1
D0				1

TABLE 10: MICROPROCESSOR REGISTER BIT DESCRIPTION

CHANNEL CONTROL REGISTER (0X04H, 0X08H, 0X0CH, 0X10H, 0X14H, 0X18H, 0X1CH, 0X20H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	RLAM_n	**RLOS/AIS Mode Select** This bit is used to select the industry standard for declaring / clearing RLOS and AIS functionality. See the Receive Path Line Interface section of this datasheet. "0" = ITU G.775 "1" = ETSI300233	R/W	0

TABLE 10: MICROPROCESSOR REGISTER BIT DESCRIPTION

CHANNEL CONTROL REGISTER (0X04H, 0X08H, 0X0CH, 0X10H, 0X14H, 0X18H, 0X1CH, 0X20H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D5	ARAOS_n	**Automatic Receive All Ones** If ARAOS_n is selected, an all ones pattern will be sent to the RPOS/RNEG outputs if the channel experiences an RLOS condition. If RLOS does not occur, ARAOS_n will remain inactive. "0" = Disabled "1" = Enabled	R/W	0
D4	ATAOS_n	**Automatic Transmit All Ones** If ATAOS_n is selected, an all ones pattern will be transmitted from TTIP/TRING if the channel experiences an RLOS condition. If RLOS does not occur, ATAOS_n will remain inactive. "0" = Disabled "1" = Enabled	R/W	0
D3	TAOS_n	**Transmit All Ones** If TAOS_n is selected, an all ones pattern will be transmitted from TTIP/TRING if the transmitter is turned on. Remote Loop Back has priority over TAOS. "0" = Disabled "1" = Enabled	R/W	0
D2	TXOE_n	**Transmit Output Enable** Upon power up, the tranmitters are tri-stated. This bit is used to enable the transmitter for this channel if the TxOE pin is pulled "High". If the TxOE pin is pulled "Low", all 8 transmitters are tri-stated. "0" = Transmitter is disabled "1" = Transmitter is enabled if TxOE pin is pulled "High"	R/W	0
D1 D0	TERSEL1 TERSEL0	**Receive Line Impedance Select** TERSEL[1:0] are used to select the internal line impedance. "00" = 75Ω for Tx and "High-Z" for Rx "01" = 120Ω for Tx and "High-Z" for Rx "10" = 75Ω for Tx and Rx "11" = 120Ω for Tx and Rx	R/W	0 0

TABLE 11: MICROPROCESSOR REGISTER BIT DESCRIPTION

CHANNEL CONTROL REGISTER (0X05H, 0X09H, 0X0DH, 0X11H, 0X15H, 0X19H, 0X1DH, 0X21H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	SRESET_n	**Software Reset** By setting this bit to "1" for more than 10µS, the individual channel is reset to its default register configuration and all state machines are internally reset. "0" = ITU G.775 "1" = ETSI300233	R/W	0
D5	AISIE_n	**Alarm Indication Signal Interrupt Enable** "0" = Masks the AIS interrupt generation "1" = Enables Interrupt generation	R/W	0
D4	DMOIE_n	**Digital Monitor Output Interrupt Enable** "0" = Masks the DMO interrupt generation "1" = Enables Interrupt generation	R/W	0
D3	RLOSIE_n	**Receiver Loss of Signal Interrupt Enable** "0" = Masks the RLOS interrupt generation "1" = Enables Interrupt generation	R/W	0
D2	Reserved	This Register Bit is Not Used	X	X
D1 D0	LB1 LB0	**Loop Back Select** These bits are used to configure the channel in one of three loop-back modes. For additional information on loopback modes, see the Application Section of this datasheet. "00" = No Loopback "01" = Romote Loopback "10" = Analog Loopback "11" = Digital Loopback	R/W	0

TABLE 12: MICROPROCESSOR REGISTER BIT DESCRIPTION

CHANNEL CONTROL REGISTER (0X06H, 0X0AH, 0X0EH, 0X12H, 0X16H, 0X1AH, 0X1EH, 0X22H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	X
D6	Reserved	This Register Bit is Not Used	R/W	X
D5	AISI_n	**Alarm Indication Signal Interrupt Status** "0" = No Change "1" = Change in Status Occured	RUR	0

TABLE 12: MICROPROCESSOR REGISTER BIT DESCRIPTION

CHANNEL CONTROL REGISTER (0X06H, 0X0AH, 0X0EH, 0X12H, 0X16H, 0X1AH, 0X1EH, 0X22H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D4	DMOI_n	**Digital Monitor Output Interrupt Status** "0" = No Change "1" = Change in Status Occured	RUR	0
D3	RLOSI_n	**Receiver Loss of Signal Interrupt Status** "0" = No Change "1" = Change in Status Occured	RUR	0
D2	Reserved	This Register Bit is Not Used	R/W	X
D1	Reserved	This Register Bit is Not Used	R/W	X
D0	Reserved	This Register Bit is Not Used	R/W	X

TABLE 13: MICROPROCESSOR REGISTER BIT DESCRIPTION

CHANNEL CONTROL REGISTER (0X07H, 0X0BH, 0X0FH, 0X13H, 0X17H, 0X1BH, 0X1FH, 0X23H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	X
D6	Reserved	This Register Bit is Not Used	R/W	X
D5	AISS_n	**Alarm Indication Signal Alarm Status** The alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. "0" = No Alarm "1" = An all ones signal is detected	RO	0
D4	DMOS_n	**Digital Monitor Output Alarm Status** The digital monitor output is always active regardless if the interrupt generation is disabled. This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. "0" = No Alarm "1" = Transmit output driver has failures	RO	0

CHANNEL CONTROL REGISTER (0X07H, 0X0BH, 0X0FH, 0X13H, 0X17H, 0X1BH, 0X1FH, 0X23H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D3	RLOSS_n	**Receiver Loss of Signal Alarm Status** The receiver loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. "0" = No Alarm "1" = An RLOS condition is present	RO	0
D2	Reserved	This Register Bit is Not Used	R/W	X
D1	Reserved	This Register Bit is Not Used	R/W	X
D0	Reserved	This Register Bit is Not Used	R/W	X

ELECTRICAL CHARACTERISTICS

TABLE 14: ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5V to +3.8V
Vin	-0.5V to +5.5V

TABLE 15: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Voltage	VDD	3.13	3.3	3.46	V
Input High Voltage	V_{IH}	2.0	-	5.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Output High Voltage IOH=2.0mA	V_{OH}	2.4	-		V
Output Low Voltage IOL=2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_L	-	-	±10	µA
Input Capacitance	C_I	-	5.0		pF
Output Lead Capacitance	C_L	-	-	25	pF

NOTE: *Input leakage current excludes pins that are internally pulled "Low" or "High"*

TABLE 16: AC ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
MCLK Clock Duty Cycle		40	-	60	%
MCLK Clock Tolerance		-	±50	-	ppm

TABLE 17: POWER CONSUMPTION

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED								
MODE	**SUPPLY VOLTAGE**	**IMPEDANCE**	**RECEIVER**	**TRANSMITTER**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
E1	3.3V	75Ω	1:1	1:2	TBD TBD	-	mW	50% ones 100% ones
E1	3.3V	120Ω	1:1	1:2	TBD TBD	-	mW	50% ones 100% ones

TABLE 18: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
Receiver Loss of Signal					
Number of consecutive zeros before RLOS is declared	-	32	-		
Input signal level at RLOS	15	24	-	dB	Cable attenuation @ 1024kHz
RLOS clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (short haul with cable loss)	9	11	-	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω with -18dB interference signal added.
Input Impedance	-	13	-	kΩ	
Input Jitter Tolerance					
1Hz	37	-	-	UI_{p-p}	ITU-G.823
10kHz - 100kHz	0.2	-	-	UI_{p-p}	
Recovered Clock Jitter					
Transfer Corner Frequency	-	36	-	kHz	ITU-G.736
Peaking Amplitude	-	-	-0.5	dB	
Jitter Attenuator Corner Frequency	-	10	-	Hz	ITU-G.736
JABW = "0"	-	1.5	-	Hz	
JABW = "1"					
Return Loss					
51kHz - 102kHz	14	-	-	dB	ITU-G.703
102kHz - 2048kHz	20	-	-	dB	
2048kHz - 3072kHz	16	-	-	dB	

TABLE 19: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
AMI Output Pulse Amplitude					
75Ω	2.13	2.37	2.60	V	1:2 Transformer
120Ω	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05		ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05		ITU-G.703

TABLE 19: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

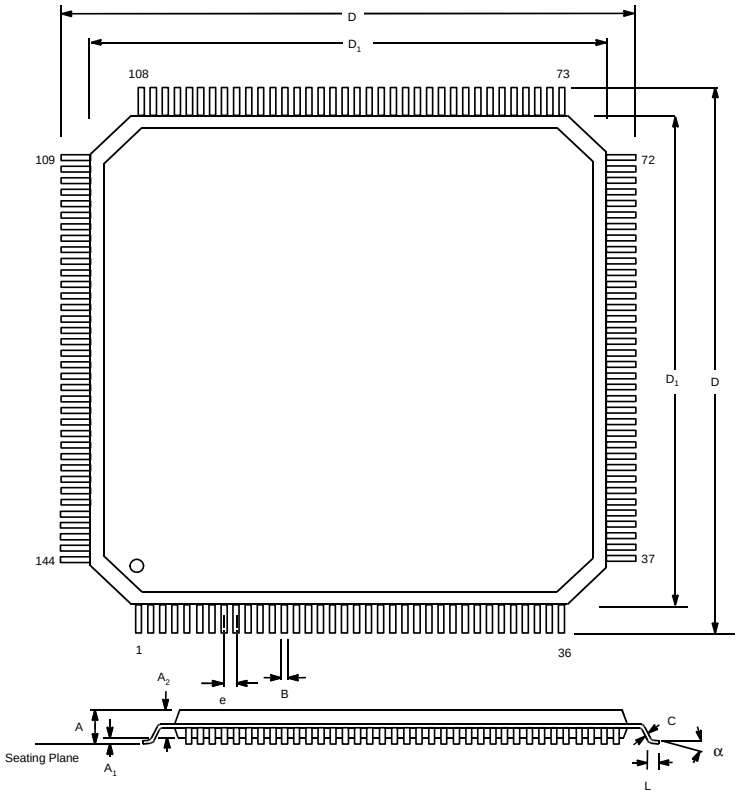
VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
Jitter Added by the Transmitter Output	-	0.025	0.05	UI_{p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	8	-	-	dB	ETSI 300 166, CHPTT
102kHz - 2048kHz	14	-	-	dB	
2048kHz - 3072kHz	10	-	-	dB	

ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83SL28IB	144 LEAD TQFP	-40^{0}C to +85^{0}C

PACKAGE DIMENSIONS

144 LEAD THIN QUAD FLAT PACK
(20 x 20 x 1.4 mm TQFP)
rev. 1.00



Note: *The control dimension is the millimeter column*

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.4	1.6
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.8	22.2
D1	0.783	0.791	19.9	20.1
e	0.020 BSC		0.50 BSC	
L	0.018	0.03	0.45	0.75
α	0º	7º	0º	7º
β	0.490	0.510	12.45	12.96

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	06/02/03	First release of the 8-Channel LIU Preliminary Datasheet
P1.0.1	09/23/03	Updated the Receive Sensitivity in the Electrical Specification. Removed the Copper Slug reference in the package drawing.