

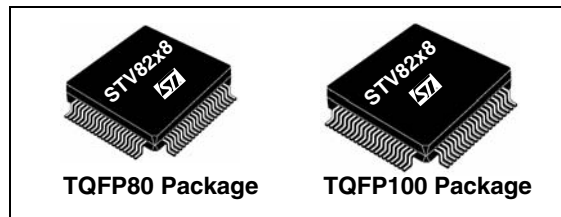


# STV82x8

## Digital audio decoder/processor for BTSC television/video recorders

### Features

- Fully automatic multi-standard demodulation
  - M/N standards
  - FM mono
  - BTSC (US MTS) stereo and SAP standards
- Multi-channel capability
  - 3 x I<sup>2</sup>S digital inputs
  - I<sup>2</sup>S SRC
  - S/PDIF (pass thru/out)
  - 5.1 analog outputs
  - 1 x I<sup>2</sup>S digital output (shared with one I<sup>2</sup>S digital input)
  - 2 x I<sup>2</sup>S additional digital outputs (TQFP100 only)
  - I<sup>2</sup>S digital loop for external delay (TQFP100 only)
- Sound processing: Loudspeaker
  - Dolby<sup>®</sup>, Pro Logic<sup>®</sup>,
  - Dolby<sup>®</sup>, Pro Logic II<sup>®</sup>,
  - ST royalty-free processing: ST WideSurround<sup>™</sup>, ST OmniSurround<sup>™</sup>, (which is Virtual Dolby<sup>®</sup>, Surround and Virtual Dolby<sup>®</sup>, Digital compliant), ST Dynamic Bass<sup>™</sup>
  - SRS<sup>®</sup>, WOW<sup>™</sup>, SRS<sup>®</sup> TruSurround XT<sup>™</sup>, (which is Virtual Dolby<sup>®</sup>, Surround and Virtual Dolby<sup>®</sup>, Digital compliant)
  - SVC (smart volume control), 5-band equalizer and loudness
  - Independent volume/balance
  - Variable beep tone and 3 sampled tones
- Sound processing: Headphone
  - SVC (smart volume control), bass-treble, loudness and SRS<sup>®</sup>, TruBass<sup>™</sup>,
  - Independent volume/balance
- Analog audio matrix
  - 4 stereo inputs or 5 stereo inputs (TQFP100 only)
  - 3 stereo outputs
  - THRU mode
  - 2 V<sub>RMS</sub> capability
- Audio delay for audio video synchronization
  - Embedded stereo delay up to 117 ms for lip-sync function
  - Independent delay on headphone and loudspeaker channels
  - External additional audio delay support (TQFP100 only)



### Description

The STV82x8 family, based on 24-bit 48kHz audio DSPs (digital signal processors), performs high quality and advanced dedicated digital audio processing. The STV82x8 devices provide all of the necessary resources for automatic detection and demodulation of analog audio transmissions for USA, Taiwanese, and Brazilian terrestrial analog TV broadcasts.

Virtual or true multi-channel capabilities and easy digital links make them ideal for digital audio low cost consumer applications. Starting from enhanced stereo up to independent control of 5 loudspeakers and a subwoofer (5.1 channels), the STV82x8 family offers standard and advanced features plus sound enhancements, spatial and virtual effects to enhance television viewer comfort and entertainment.

**Table 1. Device summary**

Order code	Packaging
STV82x8	Tray

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# 1 Block diagrams

Figure 1. STV82x8 block diagram (TQFP80)

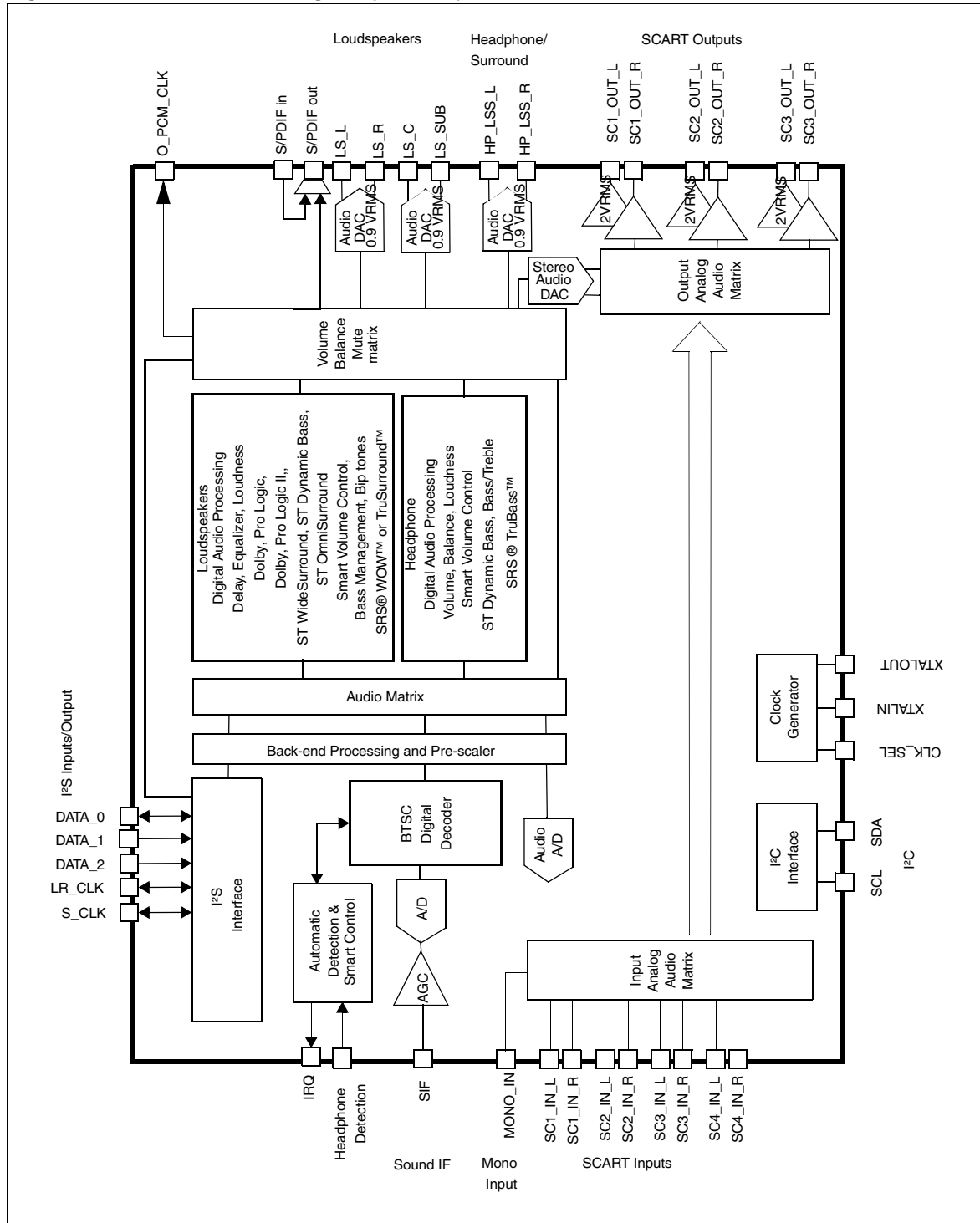
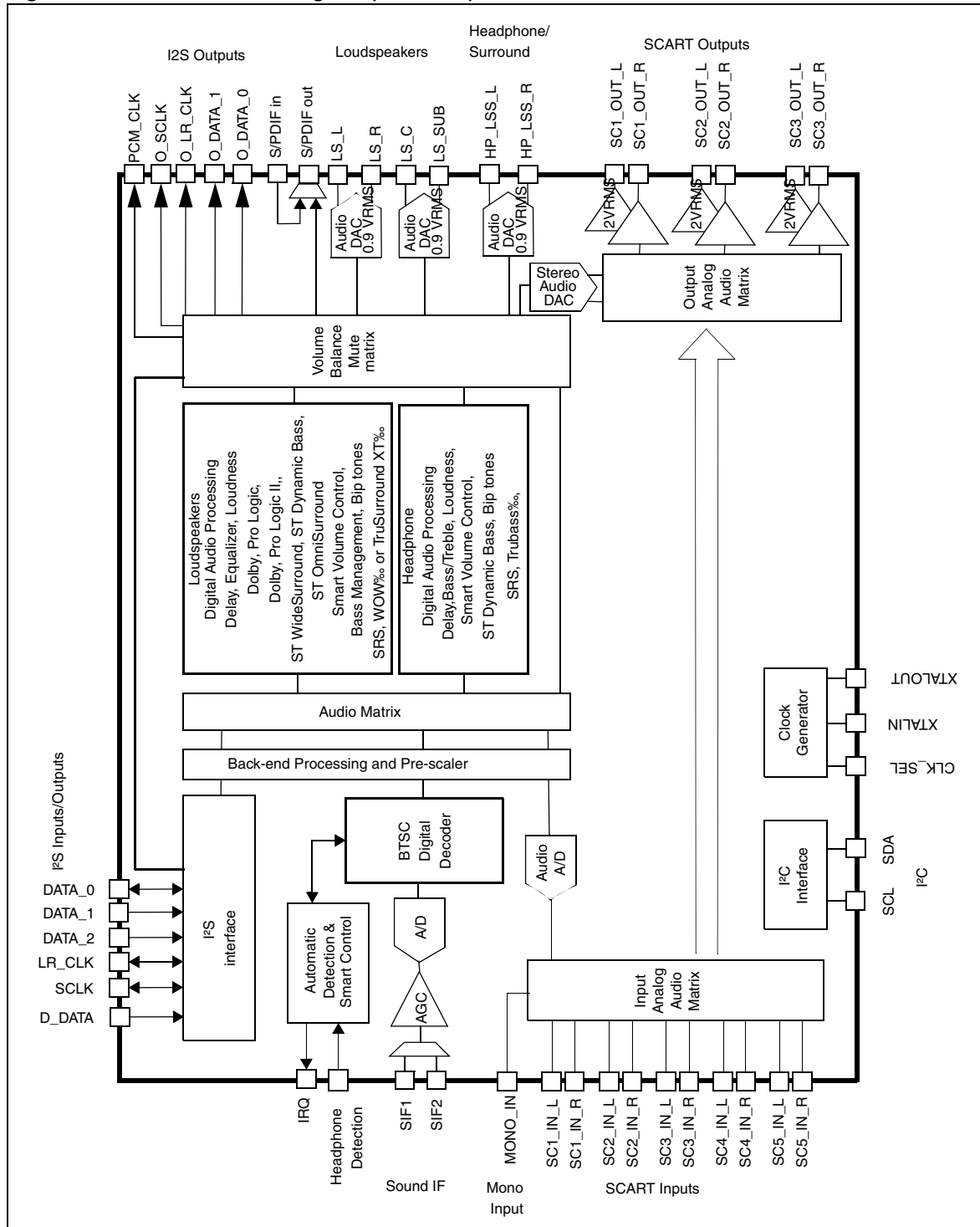


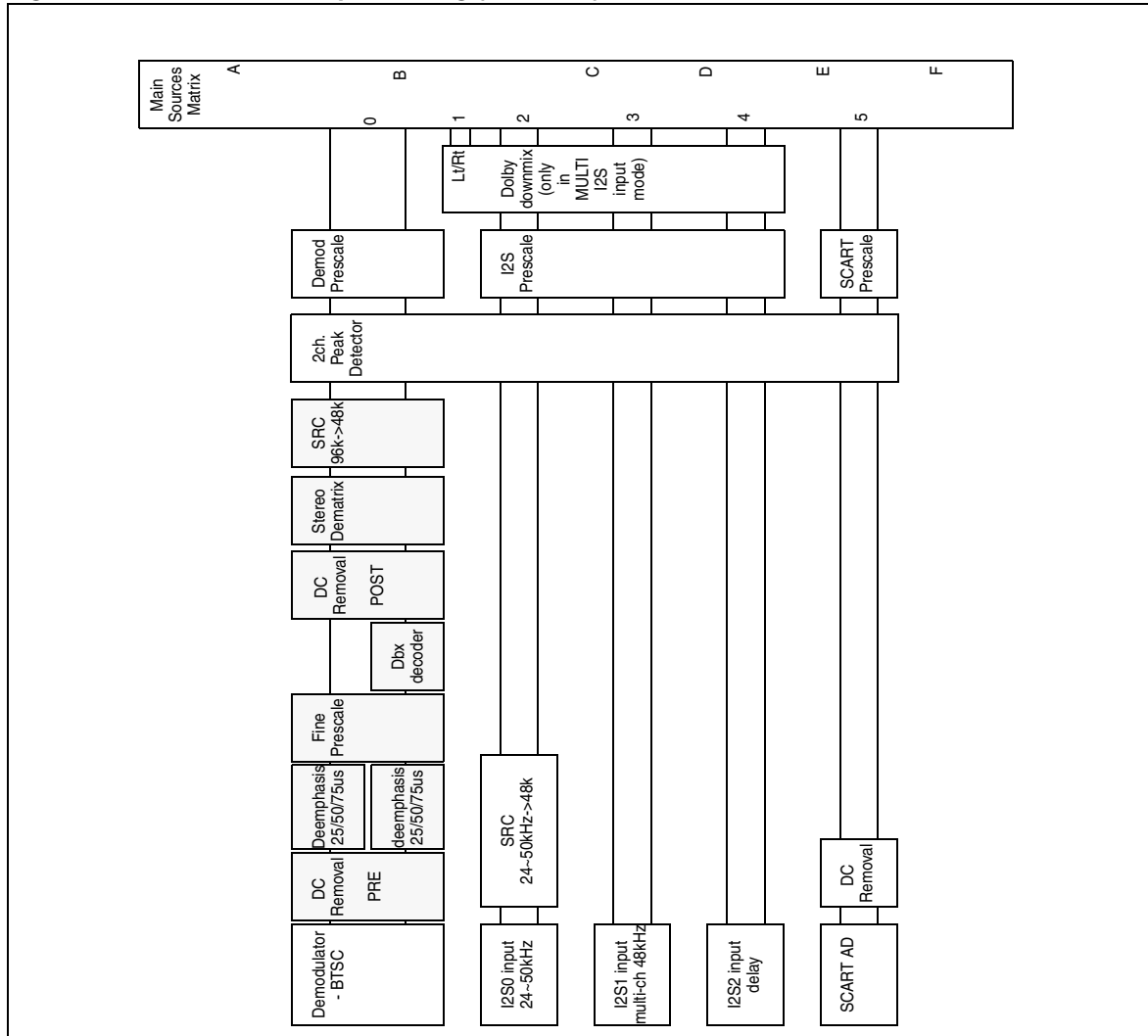
Figure 2. STV82x8 block diagram (TQFP100)



## 2 Digital signal processor

A dedicated DSP (digital signal processor) takes charge of all audio processing features and the low frequency signal processing features of the demodulator. The internal 24-bit architecture will ensure a high quality signal treatment and an excellent dynamic.

Figure 3. STV82x8 audio processing (front-end)



### 2.1 Back-end processing

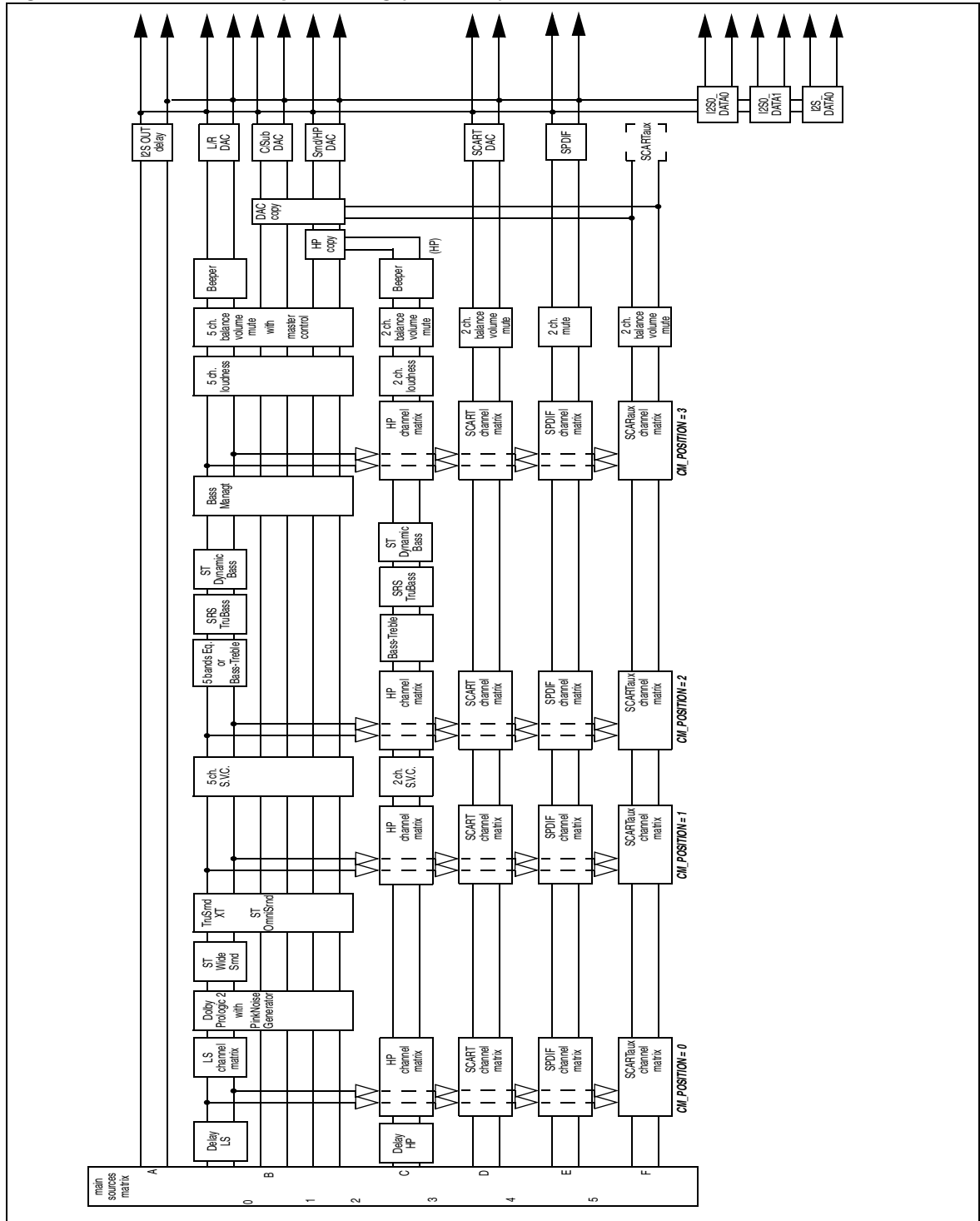
The “back-end” processing corresponds to the low frequency signal processing (32 kHz or higher frequencies) of the demodulator and other inputs (I<sup>2</sup>S, ADC).

Figure 4 shows a flowchart of the back-end processing tasks. However, the figure shows that the processing is only a SINGLE SOURCE PROCESSING flow (no processing is



possible with “Demod + SCART” and I<sup>2</sup>S inputs simultaneously) and that the selection of a headphone output restricts the loudspeakers configuration to 2.1 instead of 5.1.

Figure 4. STV82x8 audio processing (back-end)



The main features depend on the path:

- FM channel
  - DC removal
  - Prescaling
  - De-emphasis (50 or 75 us)
  - Stereo dematrix
- Input SCART Channel
  - DC removal
  - Prescaling
- Input I<sup>2</sup>S channel
  - I<sup>2</sup>S prescaling
- Digital Audio Matrix
  - Audio channel multiplexer between the different sources (IF, I<sup>2</sup>S, SCART) towards all outputs (S/PDIF, LS, HP or SCART).
- Autostandard management
  - device configuration depending on the standard to be detected
  - freeze the device when a standard is detected
  - once a standard detected, check that there is no change in the detection status
  - set the correct action depending on any change in the detection status (mono backup or mute setup and new standard detection)
- SCART
  - Downmixing: L<sub>T</sub> / R<sub>T</sub> or L<sub>0</sub> / R<sub>0</sub> (see AC-3 specification)
  - Soft Mute

## 2.2 Audio processing

The following software is provided for main loudspeakers (L, R, C, L<sub>S</sub>, R<sub>S</sub>, SubW):

- Downmix
- Dolby<sup>®</sup> Pro Logic II<sup>®</sup> decoder (L<sub>T</sub>, R<sub>T</sub> → L, R, C, L<sub>S</sub>, R<sub>S</sub>, SubW) with bass management ST WideSurround<sup>™</sup>, ST OmniSurround<sup>™</sup>, SRS<sup>®</sup> WOW<sup>™</sup> or SRS<sup>®</sup> TruSurround XT<sup>™</sup> (certified Virtual Dolby<sup>®</sup> Surround and Virtual Dolby<sup>®</sup> Digital)
- ST Dynamic Bass<sup>™</sup>
- SVC (smart volume control)
- 5-band equalizer or bass-treble
- Loudness
- Volume with independent channels (smooth volume control)
- Master volume control
- Mute/soft-mute
- Balance
- Beeper
- Pink noise generator (used to position the loudspeakers)
- Programmable delay for each loudspeaker
- Adjustable delay for “lip sync” up to 120 ms (to compensate for audio/video latency)

The following software is provided for the headphone or auxiliary output:

- Downmix
- SRS® TruBass™
- ST Dynamic Bass™
- SVC (smart volume control)
- Bass/Treble
- Loudness
- Independent volume for each channel (smooth volume control)
- Soft mute
- Balance
- Beeper
- Adjustable delay for “lip sync” feature up to 120 ms (to compensate for audio/video latency)

The following software is provided for SCART or S/PDIF outputs:

- Downmix
- Soft Mute

## 2.3 ST WideSurround

STV82x8 offers three preset ST WideSurround™ sound effects on the loudspeakers path:

- Music, a concert hall effects
- Movie, for films on TV
- Simulated stereo, which generates a pseudo-stereo effect from mono source

“ST WideSurround” sound is an extension of the conventional stereo concept which improves the spatial characteristics of the sound. This could be done simply by adding more speakers and coding more channels into the source signal as is done in the cinema, but this approach is too costly for normal home use. The ST WideSurround system exploits a method of phase shifting to achieve a similar result using only two speakers. It restores spatiality by adding artificial phase differences.

The surround/pseudo-stereo mode is automatically selected by the Automatic Standard Recognition System (Autostandard) depending on the detected stereo or mono source. By default, “Movie” is selected for surround mode. This value can be changed to “Music” by the WIDESRND\_MODE bit in the [WIDESRND\\_CONTROL](#) register.

Additional user controls are provided to better adapt the spatial effect to the source. The ST WideSurround Gain ([WIDESRND\\_LEVEL](#)) and ST WideSurround frequency ([WIDESRND\\_FREQ](#)) registers can be used to enhance music predominancy in music mode and theater effect and voice predominancy in movie mode.

## 2.4 ST OmniSurround

STV82x8 offers a spatial virtualizer ST OmniSurround™ to output any multi-channel input in stereo on the loudspeakers path.

“ST OmniSurround” recreates a multi-channel spatial sound environment using only the left and right front speakers. It can be adapted to any input configuration (OMNISRND\_INPUT\_MODE).

ST voice allows you to enhance the voice content of your program to increase the intelligibility and the presence of the sound.

## 2.5 Dolby Pro Logic II decoder

Dolby® Pro Logic II® is a matrix decoder that decodes the five channels of surround sound that have been encoded onto the stereo sound tracks of Dolby® Surround program material such as DVD movies and TV shows.

It is even possible to decode standard stereo signals like music or non encoded movies. Furthermore, it is an active process designed to enhance sound localization through the use of very high-separation decoding techniques.

The Dolby® Pro Logic II® decoder is also able to emulate the former Dolby® Pro Logic® decoder in a specific mode.

## 2.6 Bass management

The base management process generates the subwoofer signal and adjusts all loudspeaker channels gain and bandwidth.

Speakers capable of reproducing the entire frequency range will be referred to as “full range speakers”, then signals sent to full range speaker will be full bandwidth (no filtering).

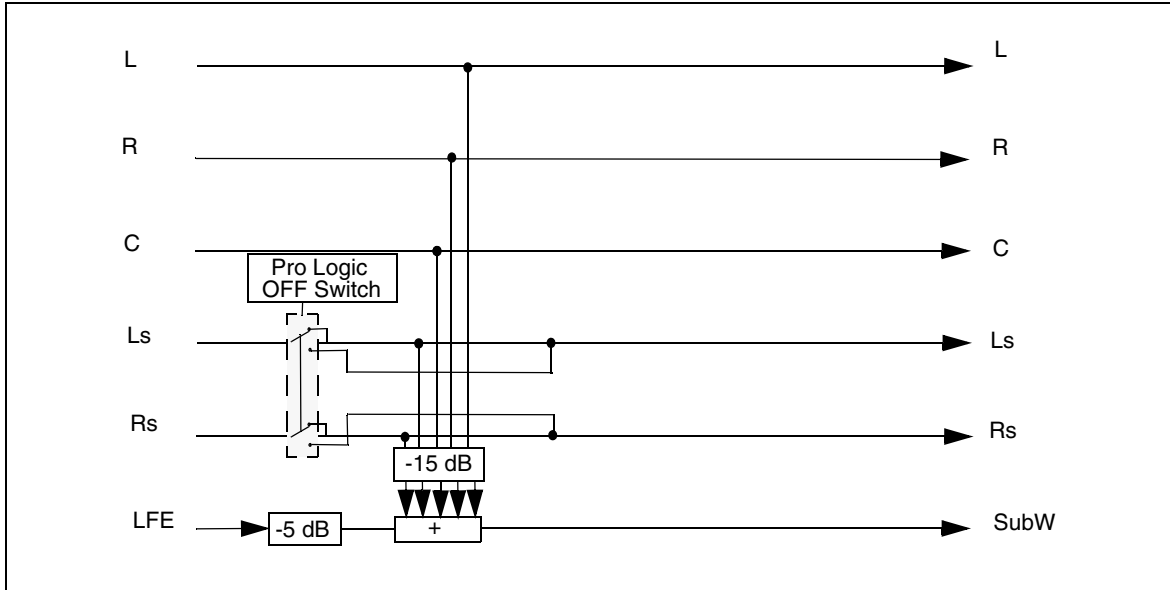
Speakers that have limited bass handling capabilities will be referred to as “satellite speakers”, then signals sent to satellite speaker will be high-pass filtered to remove bass information below 100 Hz.

In the STV82x8, seven output configuration modes have been implemented according to “Dolby Digital Consumer Decoder” specifications. They are described in the following paragraphs:

### 2.6.1 Bass management configuration 0

In some cases, the bass management filters are available in the decoder itself, so there is no need to reproduce these filters. The output configuration shown in [Figure 5](#) offers this possibility.

**Figure 5. Bass management configuration 0 (with Pro Logic switch indicating its reset state)**

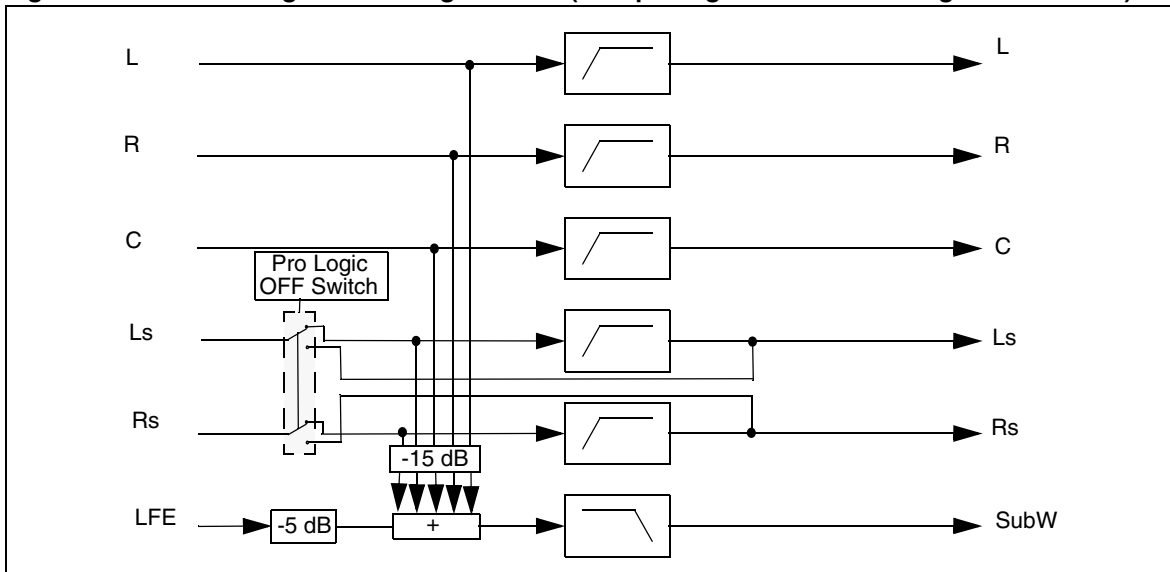


**2.6.2 Bass management configuration 1**

Configuration 1, shown in [Figure 6](#), assumes that all five speakers are not full range and that all of the bass information is redirected to and reproduced by a single subwoofer. This configuration is intended for use with five satellite speakers.

To prevent signal overload, the five main channels are attenuated by 15 dB, while the LFE channel is attenuated by 5dB to maintain the proper mixing ratio.

**Figure 6. Bass management configuration 1 (with pro logic switch indicating its reset state)**

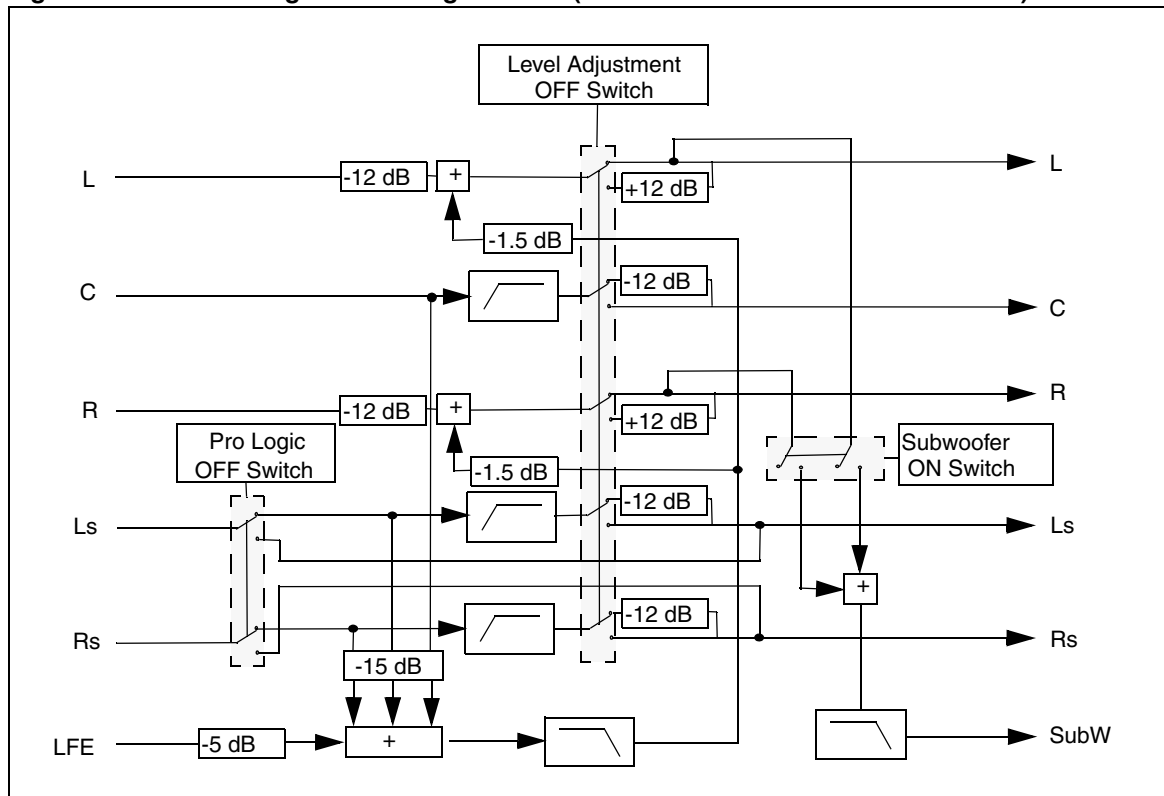


### 2.6.3 Bass management configuration 2

Configuration 2 assumes that the left and right speakers, are full range while the center and surround speakers are smaller speakers. Also, all bass data is redirected to the left and right speakers.

This configuration includes output level adjustment that allows 12 dB attenuation for the three smaller speakers (C, Ls, Rs). When the level adjustment is disabled the decoder boosts the full range speakers (Left, Right) by 12 dB.

Figure 7. Bass management configuration 2 (all switches indicate their reset state)

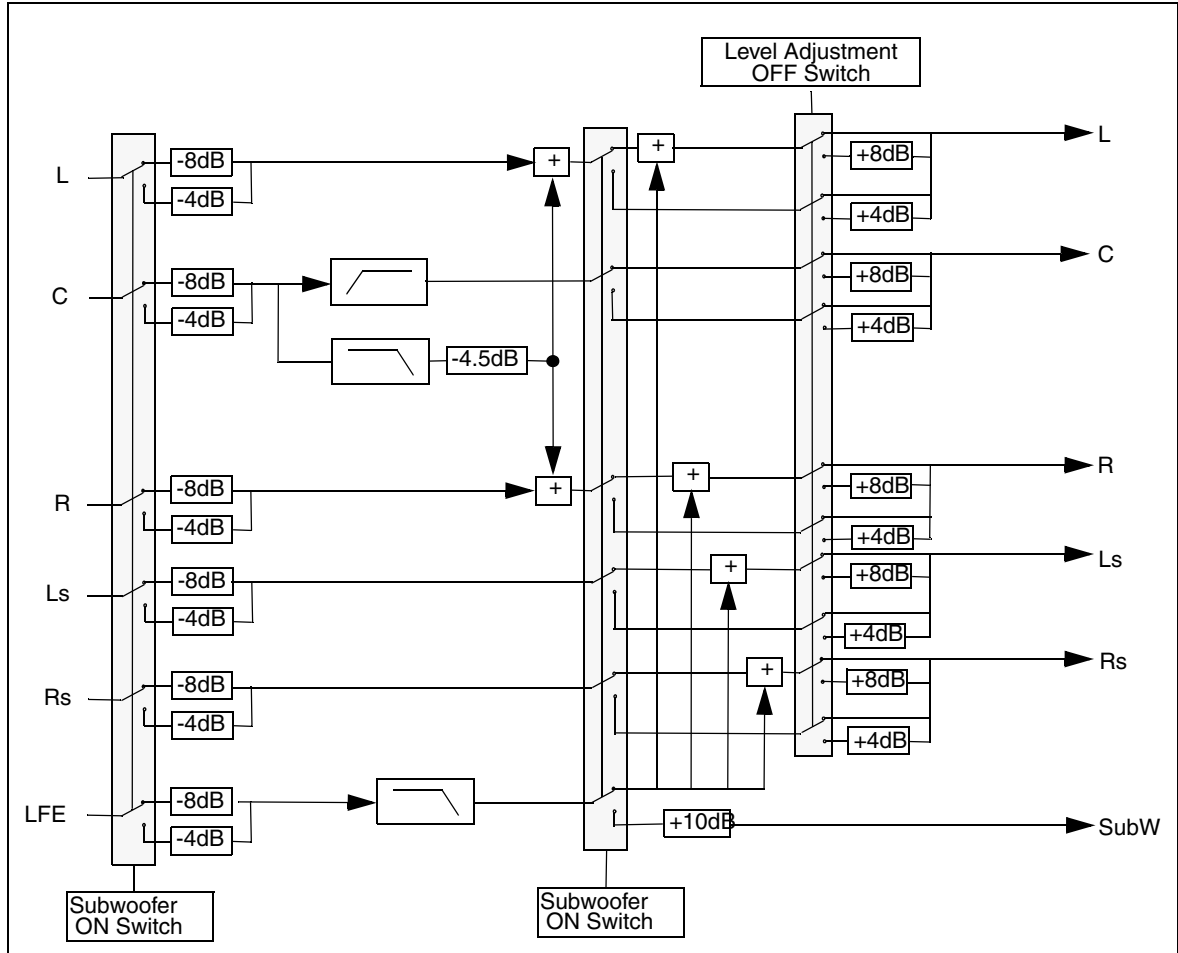


### 2.6.4 Bass management configuration 3

The third configuration, shown in [Figure 8](#), assumes that all speakers except the center are full range, then all bass information is directed to and reproduced by the front left and front right speakers and both surround speakers. To provide more flexibility to this configuration, a subwoofer switch offers an option which produces a subwoofer channel by the LFE channel.

When the subwoofer switch is OFF, the input channels are attenuated by 8 dB. Configuration 3 is required in certain high-end products.

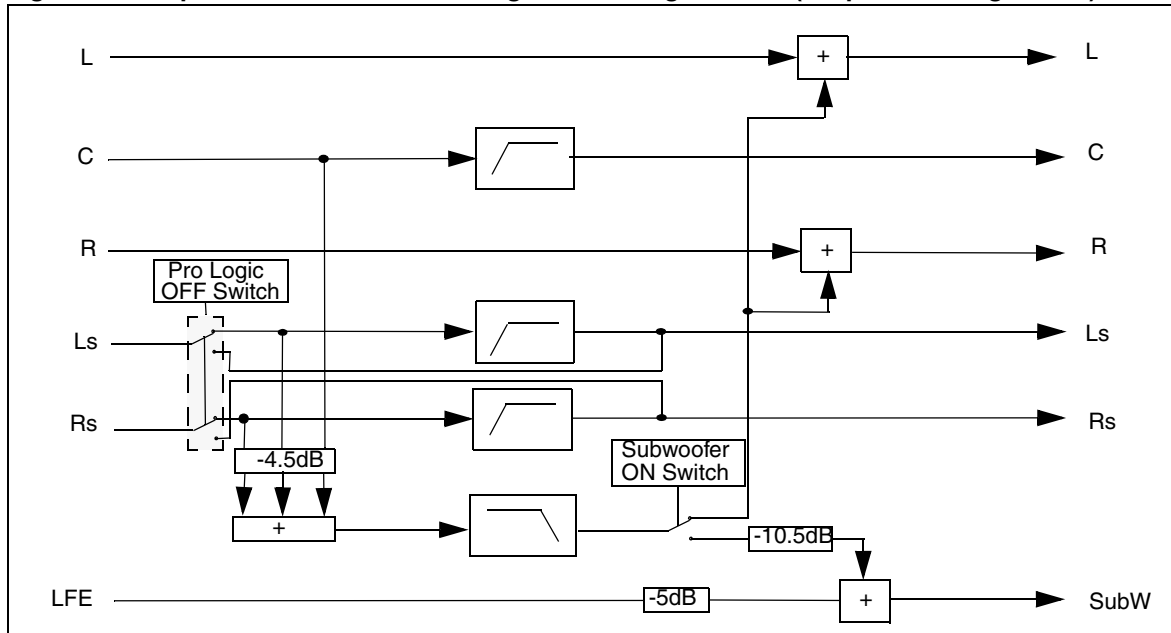
Figure 8. Bass management configuration 3 (all switches indicate their reset state)



### 2.6.5 Bass management configuration 4

This configuration implements the simplified Dolby® configuration. The center, left surround and right surround channels are summed and then filtered by the LPF. The composite bass information is either summed back into the left and right channels or summed with the LFE channel and sent to the subwoofer output, see [Figure 9](#).

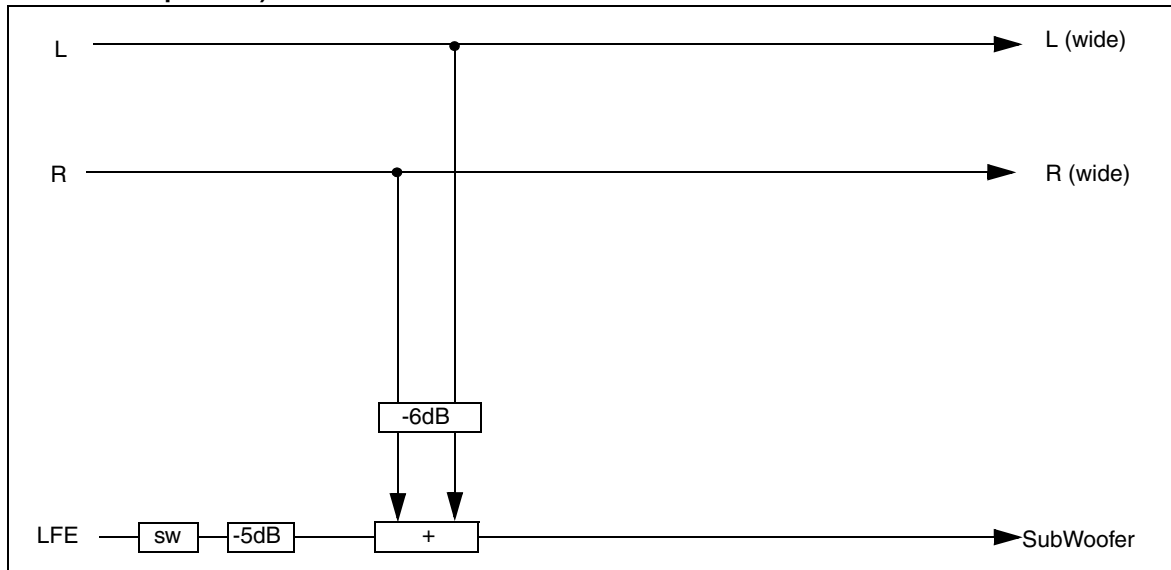
**Figure 9. Implementation of bass management configuration 4 (simplified configuration)**



**2.6.6 Bass management configuration 5 (stereo full bandwidth speakers)**

This configuration is dedicated to stereo applications implementing full bandwidth speakers.

**Figure 10. Implementation of bass management configuration 5 (stereo full bandwidth speakers)**

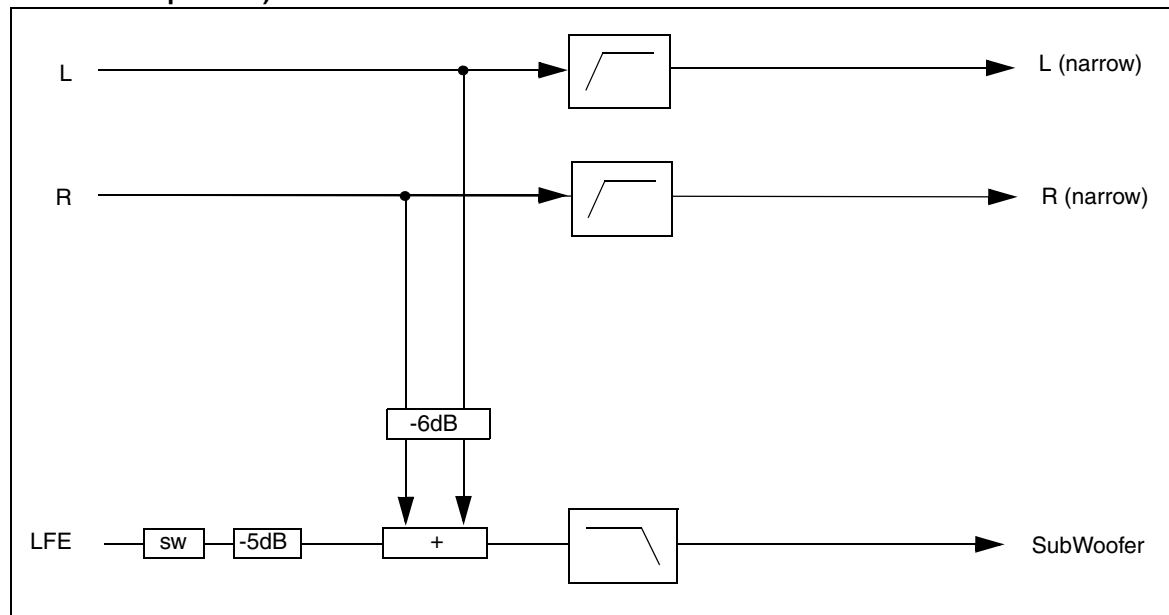


**2.6.7 Bass management configuration 6 (stereo narrow bandwidth speakers)**

This configuration is dedicated to stereo applications implementing narrow bandwidth speakers and subwoofer.



**Figure 11. Implementation of bass management configuration 6 (stereo narrow bandwidth speakers)**



## 2.7 SRS WOW and TruSurround XT

The SRS® TruSurround XT™ is a processing system that can accept from 1 to 6 channels on input and that will generate a 2-channel output signal.

This processing system includes the latest SRS® algorithms:

- SRS® WOW™
- SRS® TruSurround® (multi-channel signal virtualizer)

### 2.7.1 SRS TruSurround

The SRS® TruSurround® is a processing that can accept from 2 to 5 channels on input and that will generate a 2-channel output signal.

SRS® TruSurround® uses HRTF (head-related transfer function) -based frequency tailoring of (L/R) difference signals to extend the sound image out past the physical boundaries of the speaker placements to surround channel information. These rear channel HRTF curves have much greater peak to valley differences at center frequencies. These cause rear channel difference signals that virtualize farther behind the listener directed to a different virtual position as compared to front channel signals. Information that is equal (L+R) in the rear surround channels is processed by an identical HRTF curve but mixed in at a much lower amount. This HRTF processing of equal (L/R) signals is used to virtualize information to the rear of the listener.

The SRS® TruSurround® is certified by Dolby Laboratories to be a Virtual Dolby® Digital and Virtual Dolby® Surround.

## 2.7.2 SRS WOW

The SRS® WOW™ is a sound processing system including:

- SRS® 3D Mono/Stereo™
- SRS® Dialog Clarity™
- SRS® TruBass™

### SRS 3D Mono/Stereo

The 3D Mono/Stereo™ system is used to create a pseudo-stereo signal for mono inputs or a three-dimensional spatial signal for stereo inputs.

### SRS Dialog Clarity

The Dialog Clarity™ system is used to enhance dialog perception.

### SRS TruBass

The SRS® TruBass™ audio enhancement technology provides deep, rich bass to small speaker systems without the need for a subwoofer or additional extra physical components. For systems with a subwoofer, SRS® TruBass™ complements and enhances bass performance. Psycho-acoustically, when the human ear is presented with a low frequency sound signal that is missing the fundamental harmonic, it will fill in the fundamental frequency based on the higher harmonics that are present. By accentuating the second and higher frequency harmonics of the bass portion of a signal, SRS® TruBass™ gives the perception of greatly improved bass response.

SRS® TruBass™ is implemented on the loudspeakers path, the headphone path or on both paths in parallel.

## 2.8 SVC (smart volume control)

SVC (smart volume control) regulates the audio signal level before audio processing. This regulation is necessary in order for the signal level to be independent from the source (terrestrial channels, I<sup>2</sup>S or SCART), its modulation (FM) and annoying volume changes (for example, advertising). SVC works as an audio compressor/expander; that is, when the input signal exceeds the threshold level, a very rapid attenuation (-2 dB/ms) is applied to rescale the signal down to the threshold value. When the input signal is below the threshold level, the previous attenuation is reduced slowly in order to retrieve the original input level (0dB gain). If the input signal is too low, an addition gain of 6 dB can be provided.

To personalize the action of the SVC, five parameters are available:

1. Threshold: maximum quasi-peak level that can be expected on output
2. Peak measurement mode: selects the channel on which the peak measurement must be performed (left, right, center...)
3. Release time: applies gain slope to the amplification phase
4. Expander switch: allows a +6dB amplification of small signals in order to reduce the output dynamic range
5. Make up gain: allows compensation of the signal amplitude limitation by a 0 to 24 dB adjustable gain.

The SVC is implemented on the loudspeakers path, headphone path or on both in parallel (independent settings). Also, the SVC can be applied in six-channel mode (L, R, L<sub>S</sub>, R<sub>S</sub>, C and SubW).

## 2.9 ST Dynamic Bass

STV82x8 offers dynamic bass boost processing on the loudspeakers path.

ST Dynamic Bass™ is a bass boost process that can dramatically increase the bass content of any program without any output level saturation.

Three cutoff frequencies (BASS\_FREQ) can be chosen, 100 Hz, 150 Hz and 200 Hz to adapt the effect to your loudspeakers. The amount of bass (BASS\_LEVEL) can also be fine tuned in order to adapt the effect loudness.

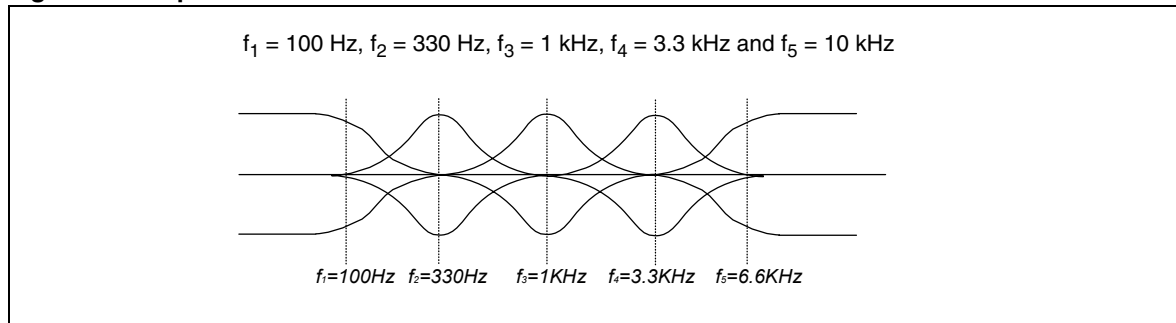
## 2.10 5-band audio equalizer

The loudspeakers audio spectrum is split into five frequency bands and the gain of each of band can be adjusted within a range from -12 dB to +12 dB in steps of 0.25 dB. The audio equalizer can be used to pre-define frequency band enhancement features dedicated to various kinds of music or to attenuate frequency resonances of loudspeakers or the listening environment. The equalizer is enabled by the LS\_EQ\_ON bit in the [EQ\\_BT\\_CTRL](#) register. The gain value for Band X is programmed in register [LS\\_EQ\\_BANDX](#).

The 5-band audio equalizer is exclusive with bass-treble control. Bit LS\_EQ\_BT\_SW in register [EQ\\_BT\\_CTRL](#) is used to select either the 5-band audio equalizer or the bass-treble control for the loudspeakers path.

Depending on the LS equalizer or LS bass-treble value, the volume level can be clamped to the LS output to prevent any possible signal clipping by using the ANTICLIP\_LS\_VOL\_CLAMP bit in the [VOLUME\\_MODES](#) (D7h) register.

Figure 12. Equalizer



### 2.10.1 Bass/Treble control

The gain of bass and treble frequency bands for the headphones can be also tuned within a range from -12 dB to +12 dB in steps of 0.25 dB. It can be used to pre-define frequency band enhancement features dedicated to various kinds of music. The headphone bass/treble feature is enabled by setting the HP\_BT\_ON bit in the [EQ\\_BT\\_CTRL](#) register. The bass and treble gain values are adjusted in registers [HP\\_BASS\\_GAIN](#) and [HP\\_TREBLE\\_GAIN](#), respectively.

Depending on the HP bass-treble value, the volume level can be clamped to the HP output to prevent any possible signal clipping by using the ANTICLIP\_HP\_VOL\_CLAMP bit in the *VOLUME\_MODES* (D7h) register.

### 2.10.2 Automatic loudness control

As the human ear does not hear the audio frequency range the same way depending on the power of the audio source, the loudness control corrects this effect by sensing the volume level and then boosting bass and treble frequencies proportionally to middle frequencies at lower volume.

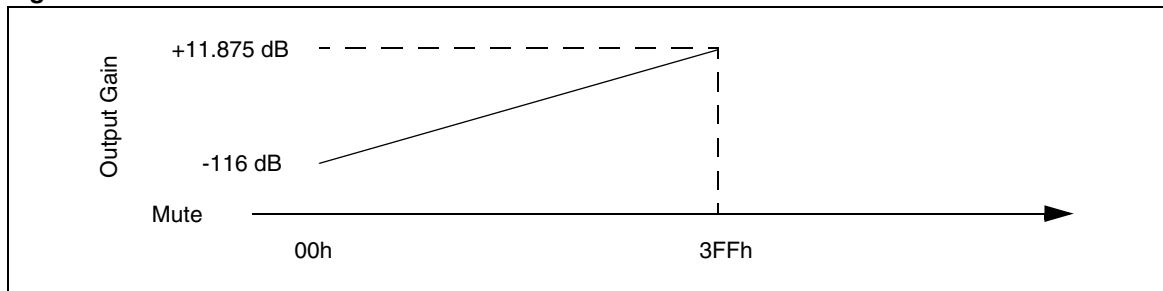
While maintaining the amplitude of the 1 kHz components at an approximately constant value, the gain values of lower and higher frequencies are automatically progressively amplified up to +18 dB when the audio volume level decreases. The maximum treble amplification can be adjusted from 0 dB (first order loudness) to +18 dB (second order loudness) in steps of 0.125 dB. As the volume is proportional to the external audio amplification power, the loudness amplification threshold is programmable in order to tune the absolute level. The loudspeakers loudness function is enabled by setting the LS\_LOUD\_ON bit in register *LS\_LOUDNESS*. The loudspeakers loudness threshold and maximum treble gain values are also programmed in this register. The headphone loudness function is enabled by setting the HP\_LOUD\_ON bit in register *HP\_LOUDNESS*. The headphone loudness threshold and maximum treble gain values are also programmed in this register.

The loudness cut-off frequency is 100 Hz.

## 2.11 Volume/Balance control

The STV82x8 provides a volume/balance control for all output channels configurations (except S/PDIF) with a different volume level per channel (L, R, C, L<sub>S</sub>, R<sub>S</sub>, SubW, SCART). Its wide range (from +11.875 to -116 dB, in a dB linear scale with a 0.125 dB step) largely covers typical home applications (approx. 60 dB) while maintaining a good S/N ratio.

Figure 13. Volume control

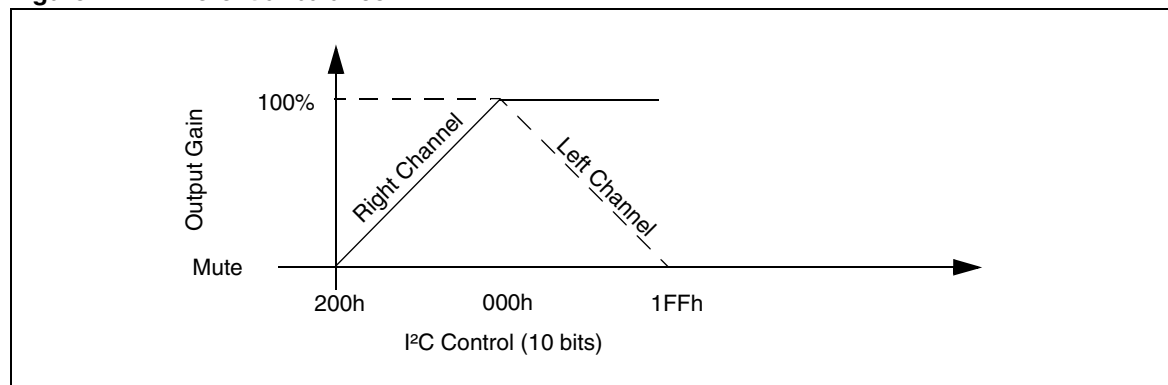


An extra master volume control can apply an extra gain/attenuation on L, R, C, L<sub>S</sub>, R<sub>S</sub> and SubW channels.

The volume/balance control can operate in one of two different modes:

- **Differential mode** (default value): The volume control is a common volume value for both the left and right loudspeakers or headphone channels (see [Figure 13](#)) and complimentary balance control is used (see [Figure 14](#)).
- **Independent mode**: The volume for the left and right channels for loudspeakers or headphones is controlled independently.

**Figure 14. Differential balance**



Note: Each step is 0.25dB

## 2.12 Soft mute control

Digital soft mute is applied smoothly (20 ms for 120 dB range) to avoid any switch noise on the output. It is available on all output channels pairs:

- S/PDIF channel (left/right)
- SCART channels (left/right)
- Loudspeakers channels (left/right)
- Center
- Subwoofer
- Headphone/Surround channels (left/right)

Another soft mute (analog) is also available on each DAC output.

## 2.13 Beeper

The beeper is used to generate a tone on the loudspeakers or/and headphone outputs. The beeper sound (square wave) is added to the audio signal which is attenuated by 20 dB. The beep sound amplitude includes a smooth attack and decay to avoid any parasitic noise when starting and stopping.

It can be used for various applications such as beep sounds for remote control, alarm clock or other features.

The beeper operates in one of two modes:

- **Pulse mode** (beep applications): A tone with a programmable short duration (0.1, 0.25, 0.5 and 1.0 s) is generated. Afterwards, the beeper is automatically disabled and the output is switched back to the audio signal, see [Figure 15](#).
- **Continuous mode** (alarm application): A tone with a programmable long duration is generated. Its start and stop controls must be programmed by I<sup>2</sup>C, see [Figure 16](#).

The beeper function is enabled by setting the BEEPER\_ON bit in register [BEEPER\\_ON](#).

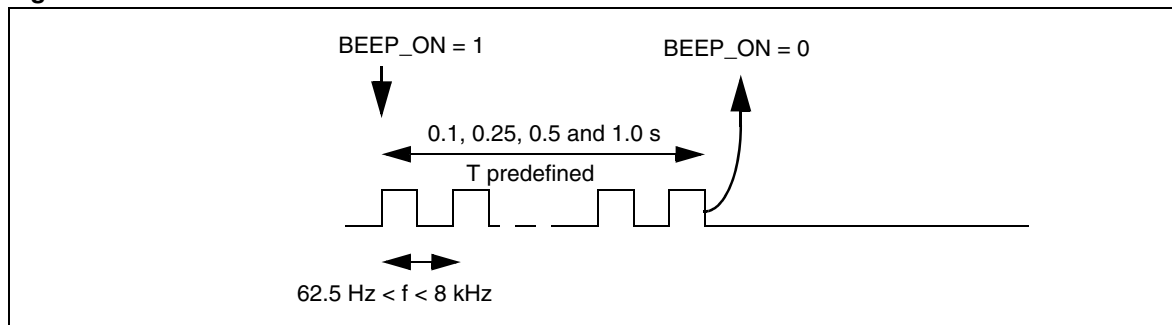
Beeper parameters are controlled in register [BEEPER\\_MODE](#).

The beeper tone level and frequency are programmed in register [BEEPER\\_FREQ\\_VOL](#).

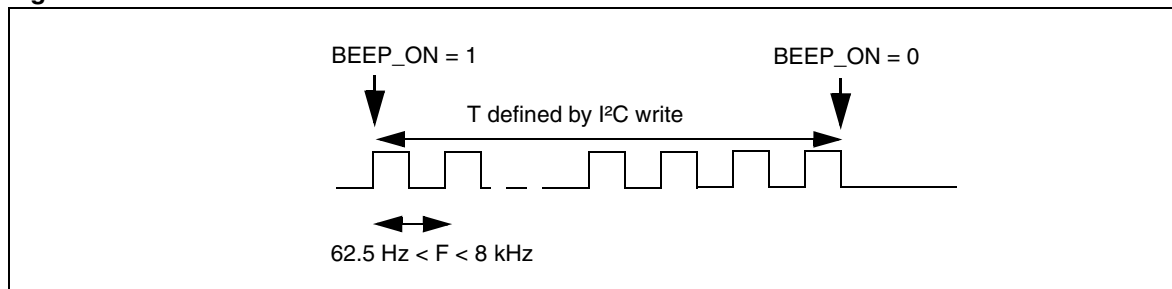
The level (or volume) ranges between 0 dB and -93 dB in steps of 3 dB and the tone frequency ranges between 62.2 Hz and 8 kHz in steps of 1 octave.

A beep generator is shared only by the loudspeakers or headphone outputs. Therefore, in the event of simultaneous beeps when in pulse mode, only the first beep will define the effective duration that will be the same for both outputs.

**Figure 15. Pulse mode**



**Figure 16. Continuous mode**



## 2.14 Internal audio/video delay (lip sync)

Internal audio/video delay is separately adjusted for loudspeakers and headphones by registers AV\_DELAY\_TIME\_LS (address EAh) and AV\_DELAY\_TIME\_HP (address AFh).

Using the delay:

- 117ms is the maximum available value. This delay applies to a stereo signal and can be fully used for loudspeaker or headphone outputs or shared between the two. In the

latter case the total delay must not exceed 117ms and the priority is given to the loudspeakers.

- In the case of a 2.0 or 2.1 platform, even if the DPL or DPLII decoder is used, the full delay is available.
- For a 5.1 platform, when DPL or DPLII is used, one part of the delay is used for center and left and right surround channels and only a 66ms maximum delay can be used or shared for the loudspeaker or headphone outputs, or both.

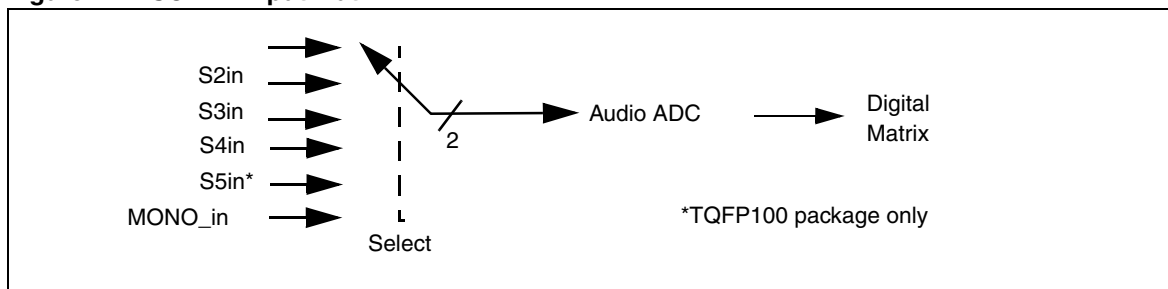
### 2.15 SCARTaux channel

The SCARTaux channel is available in the back end of audio processing, see [Figure 4](#). This gives the possibility of an output in digital format (I<sup>2</sup>S) or analog format (using C/SUB DAC or Srnd/HP DAC selection is done by register [HEADPHONE\\_CONFIG](#)) of a signal with the level of processing chosen by the CM\_POSITION\_SCARTaux[1:0] bits. The analog outputs through C/SUB DAC or Srnd/HP DAC is 1V<sub>RMS</sub> max amplitude signal.

## 3 Analog audio matrix (input/output)

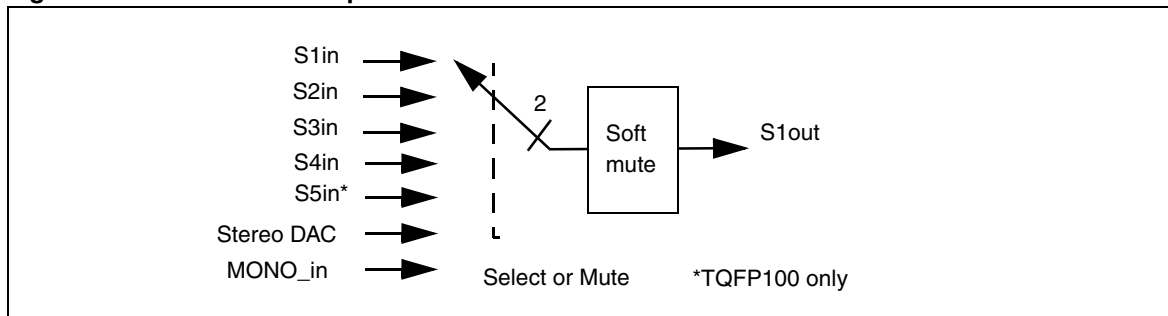
The analog part of the audio matrix can be divided into two parts: the SCART input matrix and the SCART output matrix.

Figure 17. SCART input matrix



The SCART input matrix is an input for the digital matrix (after the ADC) that selects which source is sent to the DSP.

Figure 18. SCART 1/2/3 output matrix



The SCART 1 output matrix selects the sound to output, which can be directly a SCART input or the output of the DSP. A mute function is provided to switch off the outputs.

A soft-mute function is provided to avoid all spurious sounds when switching from one position to another position.

The SCART 2 and 3 output matrixes have the same functions as the SCART 1 output matrix.

The purpose of the matrix is to accept an input signal of  $2 V_{RMS}$  and have the capability to output such a level. In this case, the power supply must be 8 V.

**The mono audio input is able to accept signals with a maximum  $0.5 V_{RMS}$  amplitude.**



## 4 I<sup>2</sup>S interface (input/output)

### 4.1 I<sup>2</sup>S inputs

#### 4.1.1 I<sup>2</sup>S inputs in TQFP 80 package

The STV82x8 can interface with a digital sound decoder. In this case, the digital data can be input at a speed of 0.384 Mbytes/s (3.072 MHz for a 48 kHz sampling frequency with 32 bits of data).

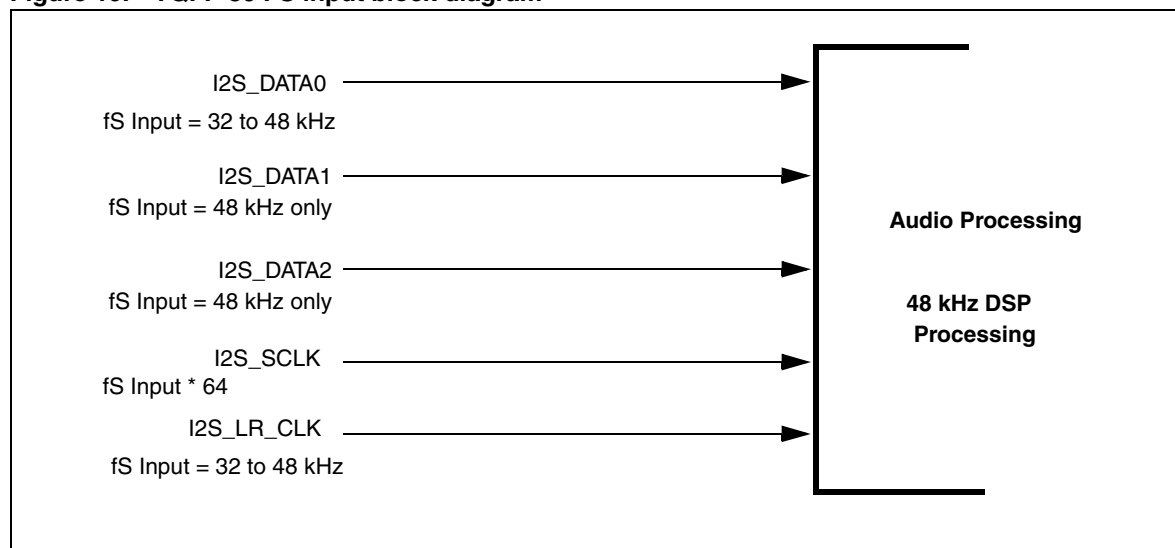
A sample rate conversion (SRC) is necessary if the input frequency is not 48 kHz (STV82x8 slave) in order to obtain a fixed frequency output from this block (48 kHz).

*Note:* The SRC function is available only in single I<sup>2</sup>S input mode.

The interface with one I<sup>2</sup>S connection (I2S\_DATA0) enables the input of stereo or stereo-coded Dolby<sup>®</sup> Pro Logic<sup>®</sup>.

One interface with three I<sup>2</sup>S connections connected to the DSP enables the processing of a multi-channel signal (maximum of 6 channels).

**Figure 19. TQFP 80 I<sup>2</sup>S input block diagram**

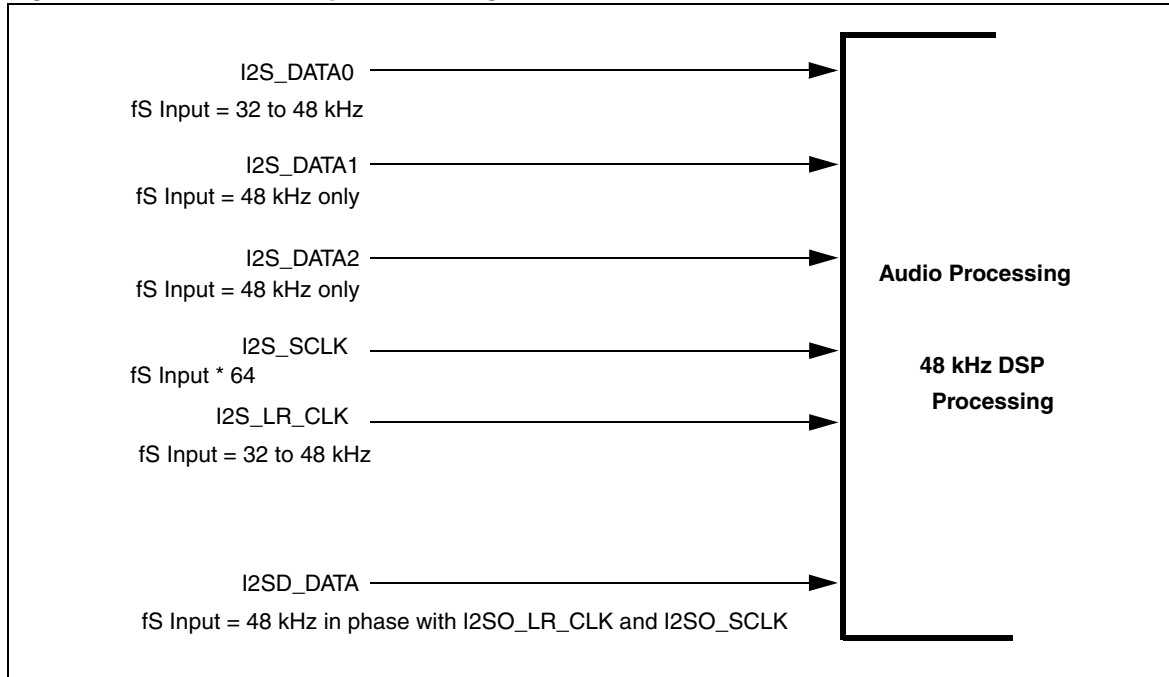


- Note:*
- 1 The I<sup>2</sup>S input and output modes are exclusive (this means that the I2S\_DATA0 can be used as input or as output).
  - 2 Simultaneous processing of I<sup>2</sup>S inputs and SIF inputs and ADC inputs (SCART or MONO inputs) is possible with the device.
  - 3 I2S\_PCM\_CLK is not needed for the device.

### 4.1.2 I<sup>2</sup>S inputs in TQFP 100 package

An I2SD\_DATA input for external delay is available, but it must be in phase with the I<sup>2</sup>S output clocks.

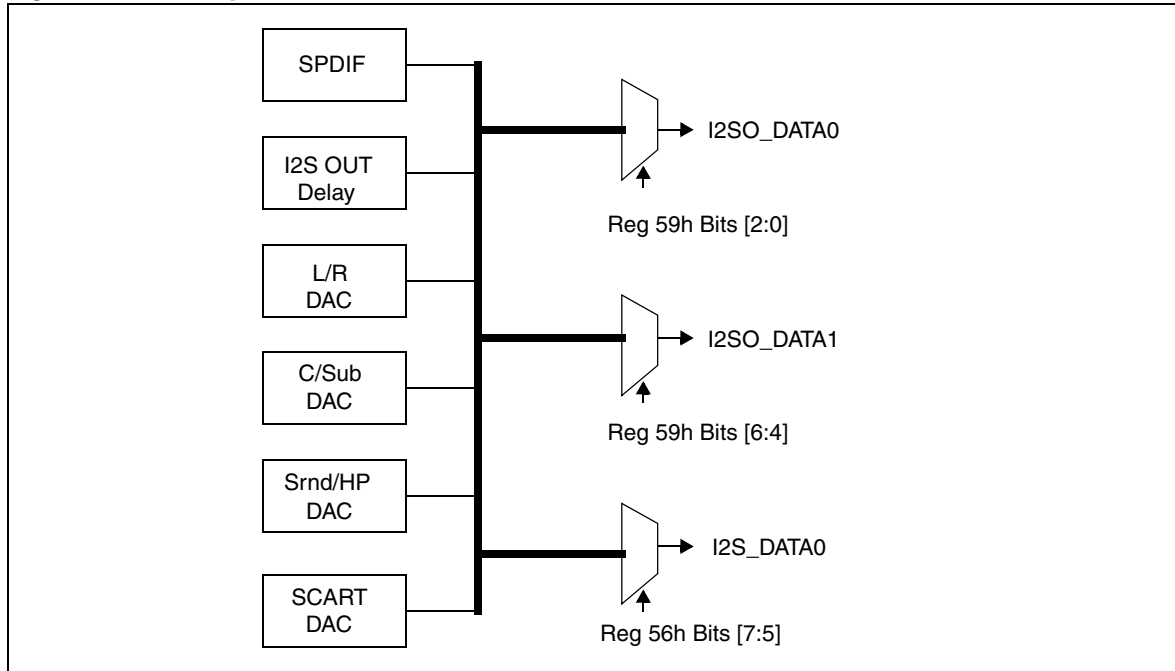
**Figure 20. TQFP100 I<sup>2</sup>S input block diagram**



- Note:*
- 1 The I<sup>2</sup>S inputs can be used together with I<sup>2</sup>S outputs using I2SO\_DATA0 and I2SO\_DATA1.
  - 2 Simultaneous processing of I<sup>2</sup>S inputs and SIF inputs and ADC inputs (SCART or MONO inputs) is possible with the device.
  - 3 I2S\_PCM\_CLK is not needed for the device.

## 4.2 I<sup>2</sup>S outputs

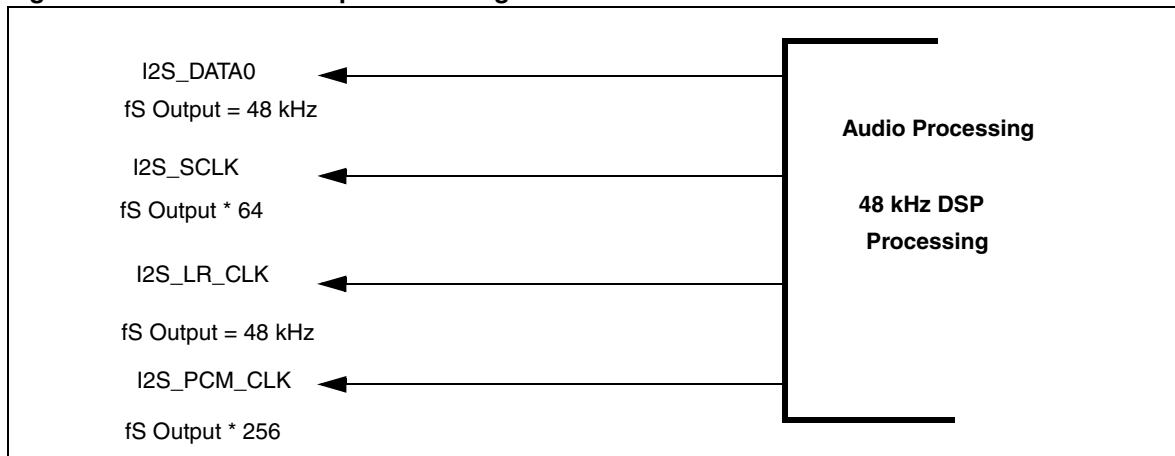
Figure 21. I<sup>2</sup>S output selection



### 4.2.1 I<sup>2</sup>S outputs in TQFP 80 package

A digital stereo output (I<sup>2</sup>S compatible) is also available for routing the demodulated signal or a converted input audio signal to an external device. In this case, the I2S\_DATA0 signal and all clock signals are set as outputs by setting bit D5 in register RESET to 1 (and bit D6 for the clocking). The STV82x8 drives the serial bus (I2S\_SCLK, I2S\_LR\_CLK, and I<sup>2</sup>S\_DATA0) in master mode in 64.fs format with a sampling frequency ( $f_s$ ) of 48 kHz. The I2S\_PCM\_CLK signal can be used as a master clock for the slave interface, if required (frequency of PCM\_CLK is  $256 \times f_s$ ). Both standard and non-standard modes are available.

Figure 22. TQFP 80 I<sup>2</sup>S output block diagram

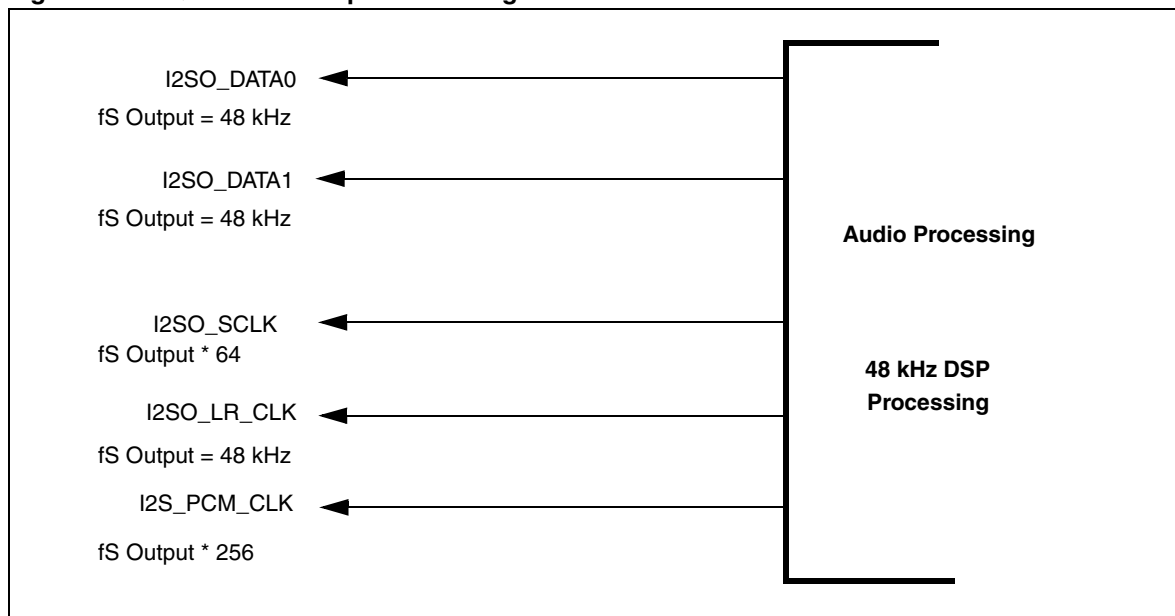


*Note:* The I<sup>2</sup>S input and output modes are exclusive (this means that the I2S\_DATA0 can be used as input or output).

### 4.2.2 I<sup>2</sup>S outputs in TQFP 100 package

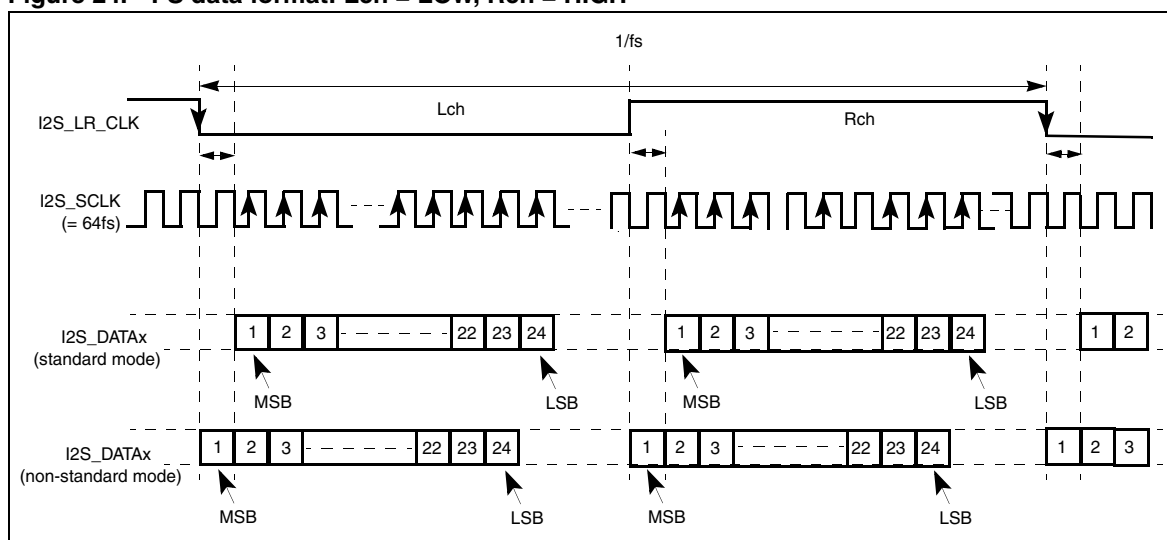
Two digital stereo outputs (I<sup>2</sup>S compatible) are available for routing the demodulated signal or a converted input audio signal to an external device or perform an external delay. In this case, the I2SO\_DATA0 and I2SO\_DATA1 signals are available with all I<sup>2</sup>S inputs active. The control is done by register *I2SO\_DATA\_CTRL*. The STV82x8 drives the serial bus (I2SO\_SCLK, I2SO\_LR\_CLK, I2SO\_DATA0, and I2SO\_DATA1) in master mode in 64.fs format with a sampling frequency (fs) of 48 kHz. The I2S\_PCM\_CLK signal can be used as a master clock if required for the slave interface (frequency of PCM\_CLK is 256 x fs). Both standard and non-standard modes are available.

**Figure 23. TQFP100 I<sup>2</sup>S output block diagram**



*Note:* 1 The I<sup>2</sup>S inputs can be used together with I<sup>2</sup>S outputs using I2SO\_DATA0 and I2SO\_DATA1.

Figure 24. I<sup>2</sup>S data format: Lch = LOW, Rch = HIGH



## 5 S/PDIF input/output

An S/PDIF output is available for connection with an external A/V decoder/amplifier.

The signal on this S/PDIF output is selected by an on chip multiplexer between the internal signal and an external signal present on S/PDIF bypass input (pin 44 for a TQFP80 package or pin 59 for a TQFP100 package) with SPDIF\_MUX bit in the DAC\_CONTROL register.

The outputted internal signal can be selected from:

- L/R
- C/Subwoofer
- HP or surround L/R
- SCART L/R

The external signal is for example the signal provided by an external Dolby® Digital decoder (STD2000).

Mute facility is also provided on the S/PDIF output.

*Note: The S/PDIF\_IN pin (pin 44 for a TQFP80 package or pin 59 for a TQFP100 package) is a CMOS digital pin and input signal on this pin must fulfill the characteristics as mentioned in [Section 17.12: Digital I/Os characteristics](#) ( $\pm 0.5V_{PP}$  standard S/PDIF input level is not directly supported by the device and needs external circuitry).*

## 6 Power supply management

A mixed supply voltage environment requires the following voltages:

- 3.3V capable inputs/outputs for digital pins;
- 1.8V digital core;
- 8V capable inputs/outputs for analog audio interfaces (capability to output 2 V<sub>RMS</sub> for SCART requirements);
- 3.3V for stereo ADC and DAC (analog part);
- 1.8V for stereo ADC and DAC (digital part);
- 1.8V for IF ADC and AGC.

These voltages will be delivered by the application with an accuracy of  $\pm 5\%$ . For more information, refer to [Section 17.3: Power supply data](#).

Other specific DC voltages or features are provided:

- Voltage reference and biasing generation (AGC, ADCs, DACs),
- Bandgap reference.

### 6.1 Standby mode (loop-through mode)

The STV82x8 provides a loop-through mode configuration that bypasses IC functions via a SCART I/O pin (full analog path only). In this case, only a minimum power of 200 mW is required.

In standby mode, the digital and analog power supplies are switched off, except for pins VCC\_H, VCC33\_LS, VCC33\_SC, and VCC\_NISO which are used to maintain the SCART path with the last configuration programmed by analog matrixing (register [SCART1\\_2\\_OUTPUT\\_CTRL](#) and [SCART3\\_OUTPUT\\_CTRL](#)). When switching back to normal full power mode, all I<sup>2</sup>C registers are reset except for those used in standby mode to maintain the original configuration.

In standby mode, the I<sup>2</sup>C bus does not operate. However, the bus can still be used by other ICs since the I<sup>2</sup>C I/O pins (SDA and SCL) of the STV82x8 are forced into a high-impedance configuration.

### 6.2 Power on reset

The following supply voltages are involved for power on reset for the STV82x8:

#### TQFP80

- 1.8V: VDD18 on pins 38, 42, 50 and 66, VCC18\_CLK1 on pin 54 and VCC18\_CLK2 on pin 57.
- 3.3V: VDD33\_IO1 on pin 46 and VDD33\_IO2 on pin 59.

#### TQFP100

- 1.8V: VDD18 on pins 50, 65 and 85, VCC18\_CLK1 on pin 69 and VCC18\_CLK2 on pin 72.
- 3.3V: VDD33\_IO1 on pin 61 and VDD33\_IO2 on pin 74.

The first condition for a valid reset is that all 1.8V supply voltages involved have reached a minimum valid voltage of 1.7V and that all 3.3V supply voltages involved have reached a minimum valid voltage of 3.1V. When this is the case and starting from this point, the reset must be maintained at a low level for at least 100 $\mu$ s then put to a high level.



## 7 Additional controls and flags

This logic contains:

- Headphone detection
- IRQ generation, the signal to be output to the MCU
- I<sup>2</sup>C bus expander output pin.

### 7.1 Headphone detection

For headphone, the  $\overline{\text{HP\_DET}}$  input can be used to automatically mute the loudspeakers and subwoofer outputs when the HP\_LS\_MUTE bit is set in register [HEADPHONE\\_CONFIG](#) (active low). When a headphone is detected (the  $\overline{\text{HP\_DET}}$  pin is set to 0) and the mute function is enabled. Each change on the  $\overline{\text{HP\_DET}}$  pin generates an IRQ request to the microprocessor on the IRQ pin.

### 7.2 IRQ generation

Four IRQs are generated by the STV82x8. On each IRQ generation, the IRQ pin is set to 1. The pending IRQ status must be read at the I<sup>2</sup>S address 81h and the acknowledge is done by writing 0 to this register.

The four available IRQs are:

**IRQ0:** The identified TV sound standard is displayed in register [AUTOSTD\\_STATUS](#). Each change in the detected standard is flagged to the host system via hardware pin IRQ. The flag must be reset by re-programming the IRQ bit in register [AUTOSTD\\_CTRL](#) and then checking the detected standard status by reading registers [AUTOSTD\\_DEM\\_STATUS](#) and [AUTOSTD\\_TIME](#).

**IRQ1:** This IRQ is enabled only in digital input mode. In case of I<sup>2</sup>S synchronization loss, this IRQ is set to 1.

**IRQ2:** This IRQ is set to 1 when the device detects any change on the HP detection pin (headphone connection or de-connection).

**IRQ3:** On the STV82x8, same pins are used for both headphone and surround loudspeaker signal output. A change in the headphone configuration (HP active or not active) leads to a signal switch on those hardware pins. In order to ensure a smooth audio transition, the output is soft muted before the signal is switched. The IRQ3 is then set to 1 to advise the master processor that the signal has been switched and to request an HP/Srnd Output Un-Mute.

### 7.3 I<sup>2</sup>C bus expander

Pin BUS\_EXP can be used to control external switchable IF SAW filters or audio switches. This pin can be directly programmed by register [RESET](#).

## 8 STV82x8 reset

All STV82x8 features are controlled via the I<sup>2</sup>C bus.

The STV82x8 can be reset in 2 ways:

- By software via the I<sup>2</sup>C bus: This clears all synchronous logic, except for the I<sup>2</sup>C bus registers.
- By hardware via the RESET pin: In addition to clearing all synchronous logic, the RESET input (active on the low level) resets all the I<sup>2</sup>C bus registers to the *default values* listed below.

**Table 2. RESET default values**

Function	Default mode
<b>Demodulation</b>	
Auto-standard	OFF
Scanned Standards	M/N BTSC
<b>Audio outputs</b>	
Automatic mute mode	ON
Loudspeaker source	Demodulated sound
Loudspeaker volume	-40 dB, differential mode, muted
Loudspeaker L/R balance	L/R = 100%
Subwoofer	-40 dB / OFF
Headphone source	Demodulated sound
Headphone automatic detection	ON
Headphone volume	-40 dB, differential mode, muted
Headphone L/R balance	L/R = 100%
SCART1 output	Demodulated sound
SCART2 output	SCART1 source
SCART3 output	SCART2 source
I <sup>2</sup> S output (TQFP 100)	Mute

## 9 I<sup>2</sup>C interface

### 9.1 I<sup>2</sup>C address and protocol

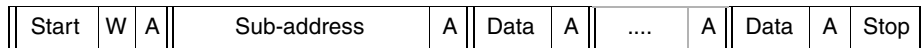
The STV82x8 I<sup>2</sup>C interface works in slave mode and is fully compliant with I<sup>2</sup>C standards in fast mode (maximum frequency of 400 kHz). Two pairs of I<sup>2</sup>C chip addresses are used to connect two STV82x8 chips to the same I<sup>2</sup>C serial bus. The device address pairs are defined by the polarity of the ADR\_SEL pin and are listed in the following table:

**Table 3. I<sup>2</sup>C read/write addresses**

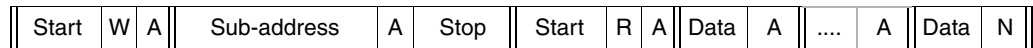
ADR	Write Address (W)	Read Address (R)
LOW (connected to GND1)	80h	81h
HIGH (connected to VDD1)	84h	85h

#### Protocol description

- Write Protocol



- Read Protocol



- W = Write address
- R = Read address
- A = Acknowledge
- N = No acknowledgement
- Sub-address is the register address pointer; this value auto-increments for both write and read.

*Note:* A minimum of 1ms is necessary for a I<sup>2</sup>C write command to be taken into account.

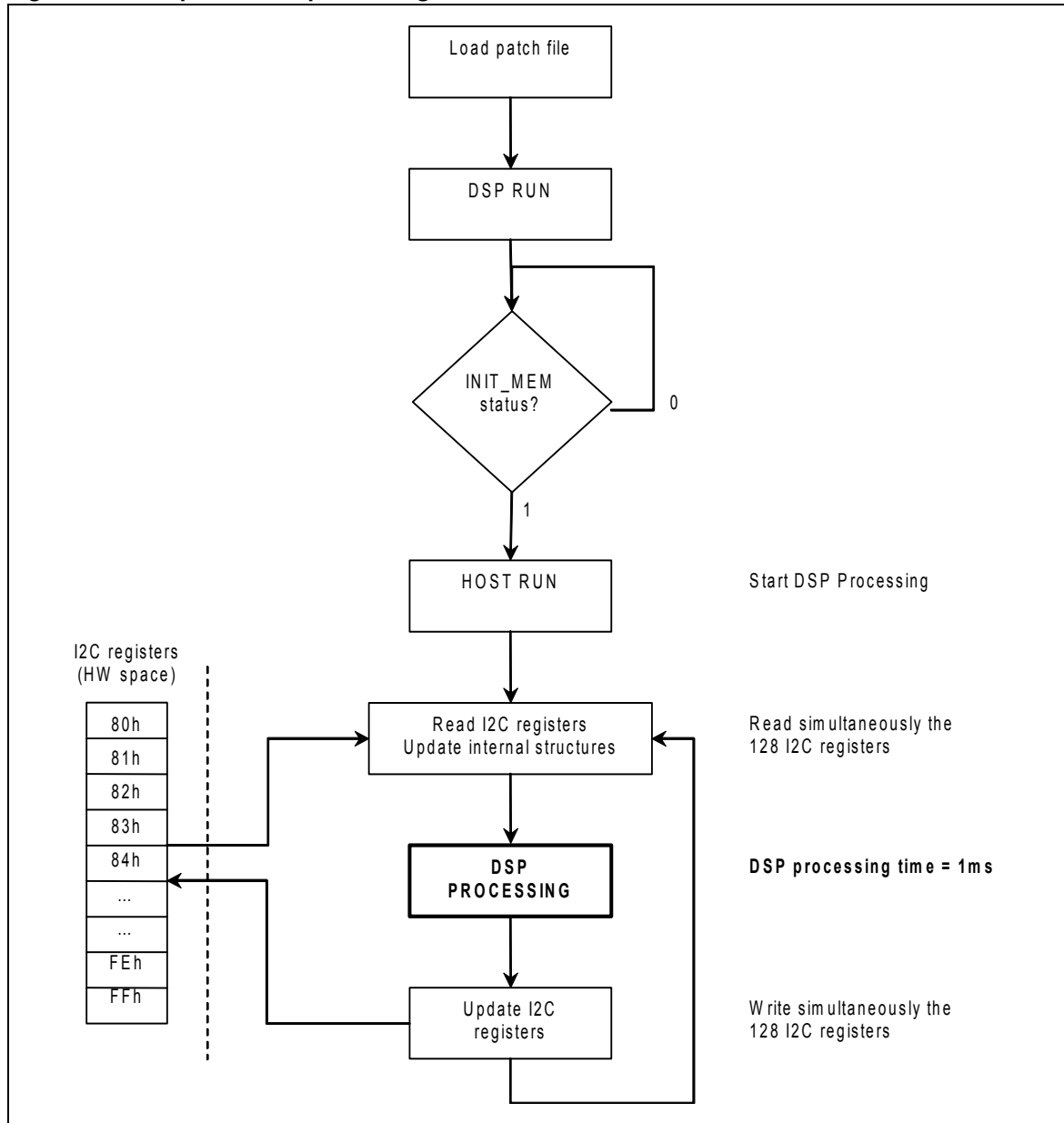
### 9.2 Start-up and configuration change procedure

The DSP running loop is:

- Read IC registers and update internal structures (memory variable)
- Process sound samples
- Write I<sup>2</sup>C registers with new updated values

The step “process sound sample” duration is **1ms**. This is shown in [Figure 25](#).

Figure 25. Simplified DSP processing flow

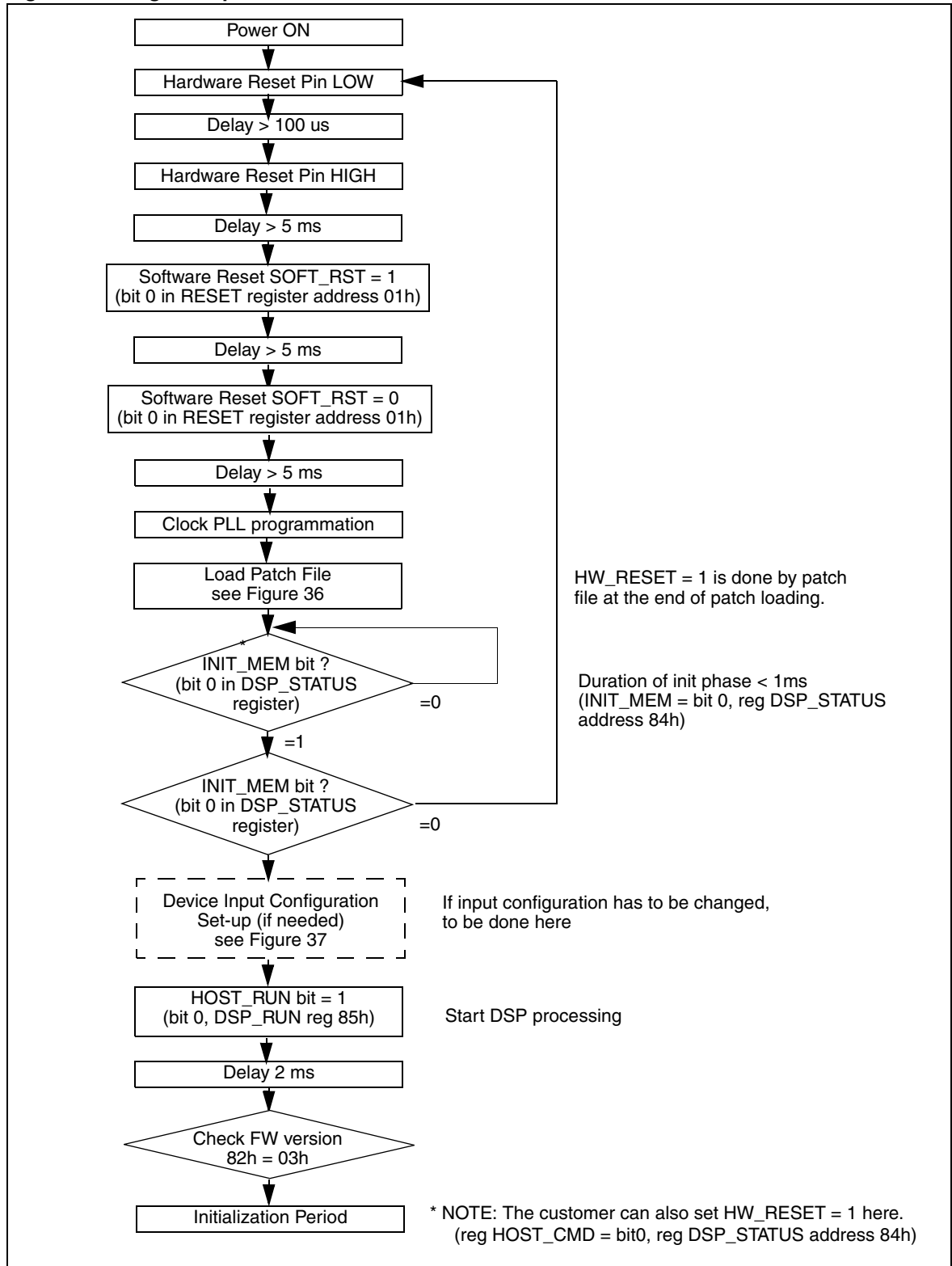


When programming the I<sup>2</sup>C read/write register with addresses between 80h and FFh this flow has to be taken into account.

For example, if two different values are written in the **same** register in less than 2 ms, it is possible that the DSP does not see the first value. This is because the second value overwrites the first one during the “DSP processing” phase, before DSP can read the registers again.

In the same way, when waiting for a register value change, the software program must wait for a least 2 ms in order to allow sufficient time for the DSP to update the register values.

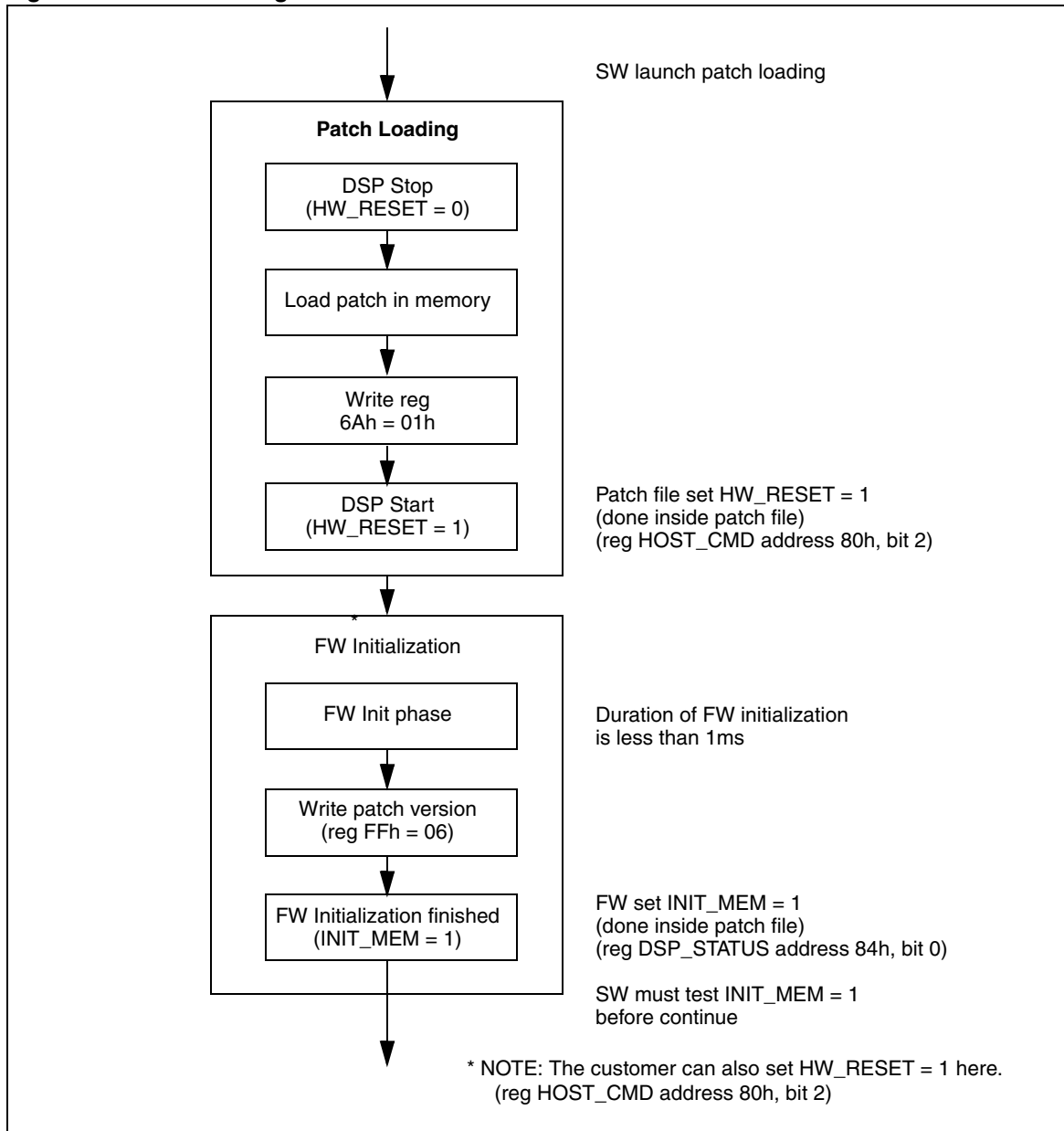
Figure 26. Register update time



### 9.3 Process flow during patch loading and DSP initialization

Patch loading and DSP firmware initialization are shown in [Figure 27](#)

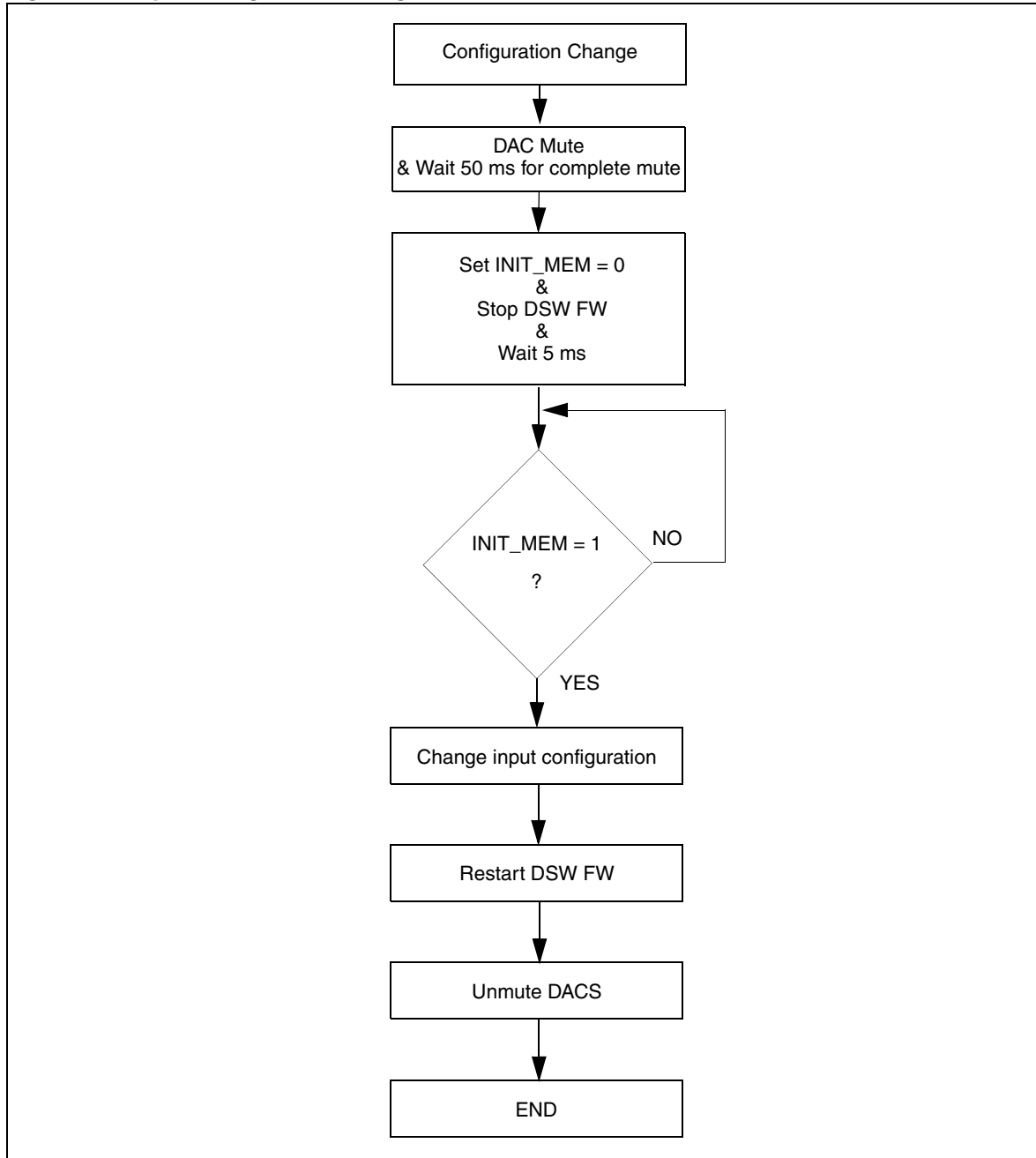
**Figure 27. Patch loading and DSP initialization**



## 9.4 Input configuration change

The input configuration change must be programmed as shown in [Figure 27](#):

**Figure 28. Input configuration change**



# 10 Register list

*Note:* The unused bits (defined as ‘Reserved’) in the I<sup>2</sup>C registers must be kept to zero.

The system clock registers (from address 08h to 0Bh and from address 5Ah to 5Dh) do not need to be modified if a standard 27 MHz crystal oscillator is used.

The default values of the demodulator registers (from address 0Ch to 55h) are for optimum performances and any change is not recommended, except for:

- **CAROFFSET1** (22h) to compensate IF carrier frequency with an out-of-standard offset.
- Soundlevel Prescaling **PRESCALE\_DEMOD\_MONO** (94h), **PRESCALE\_DEMOD\_STEREO** (95h), **PRESCALE\_DEMOD\_SAP** (96h), **PRESCALE\_SCART** (97h), **PRESCALE\_I2S0** (98h), **PRESCALE\_I2S1** (99h), **PRESCALE\_I2S2** (9Ah) to equalize demodulated or external audio signal before audio processing.
- Peak detector registers **PEAK\_DETECTOR** (9Bh), **PEAK\_L** (9Ch), **PEAK\_R** (9Dh), **PEAK\_L\_R** (9Eh) can be used to measure internal sound level.

Sound source selection for each audio output channel to be done using **AUDIO\_MATRIX1** (A2h), **AUDIO\_MATRIX2** (A3h) and **AUDIO\_MATRIX3** (A4h).

Register **AUTOSTD\_CTRL** (8Ah) is used to select the list of mono, stereo and SAP signals to be recognized automatically.

*Note:* ( ) used in reset value column means that the bit or the byte is read-only.  
 (S) symbol indicates that the field value is represented in signed binary format.

## 10.1 I<sup>2</sup>C register map

By default, all I<sup>2</sup>C registers controlled by Automatic Standard Recognition System (Autostandard) are forced to read-only mode for the user. These registers and bits are shaded in [Table 4](#).

**Table 4. List of I<sup>2</sup>C registers**

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IC General control										
<b>CUT_ID</b>	00h	(0000 0001)	0	0	CUT_NUMBER[5:0]					
<b>RESET</b>	01h	0000 0000	BUS_EXP	I2S_CO_EN	I2S_DO_EN	EN_STBY	CLOCK_DOWN	0	SOFT_LRST1	SOFT_RST
<b>I2S_CTRL</b>	04h	0000 0001	I2S_PLL	SYNC_SIGN	I2S_SRC	LOCK_TH[1:0]		LOCK_MODE	SYNC_CST[1:0]	
<b>I2S_STAT</b>	05h	(0000 0000)	0	0	0	0	0	0	LR_OFF	LOCK_FLAG
<b>I2S_SYNC_OFFSET</b>	06h	(0000 0000)	I2S_SFO[7:0]							
Clocking 1										
<b>SYS_CONFIG</b>	07h	0000 1010	SYNC_PL_L	OPEN_PL_L	INPUT_FREQ[3:0]				BIT[1:0]	
<b>FS1_DIV</b>	08h	0001 0011	EN_PROG	0	NDIV1[1:0]		0	SDIV1[2:0]		



Table 4. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>FS1_MD</i>	09h	0001 0001	0	0	0	MD1[4:0]				
<i>FS1_PE_H</i>	0Ah	0011 0110	PE_H1[7:0]							
<i>FS1_PE_L</i>	0Bh	0000 0000	PE_L1[7:0]							

**Demodulator**

<i>DEMOD_CTRL</i>	0Ch	0000 0001	0	0	0	0	0	DEMOD_MODE[2:0]		
<i>DEMOD_STAT</i>	0Dh	(0000 0000)	0	0	0	0	0	0	FM1_CA R	FM1_SQ
<i>AGC_CTRL</i>	0Eh	0001 0001	0	0	IF_SELE CT	AGC_REF[2:0]			AGC_CST[1:0]	
<i>AGC_GAIN</i>	0Fh	(0000 0000)	0	AGC_ERR[4:0]					SIG_OVE R	SIG_ UNDER
<i>DC_ERR_IF</i>	10h	(0000 0000)	DC_ERR[7:0]							

## Demodulator channel 1

<i>CARFQ1H</i>	12h	0010 1110	CARFQ1H[23:16]							
<i>CARFQ1M</i>	13h	1110 0000	CARFQ1M[15:8]							
<i>CARFQ1L</i>	14h	0000 0000	CARFQ1L[7:0]							
<i>FIR1C0</i>	15h	0000 0001	FIR1C0[7:0] (S)							
<i>FIR1C1</i>	16h	0000 0000	FIR1C1[7:0] (S)							
<i>FIR1C2</i>	17h	1111 1110	FIR1C2[7:0] (S)							
<i>FIR1C3</i>	18h	1111 1100	FIR1C3[7:0] (S)							
<i>FIR1C4</i>	19h	0000 0000	FIR1C4[7:0] (S)							
<i>FIR1C5</i>	1Ah	0000 1011	FIR1C5[7:0] (S)							
<i>FIR1C6</i>	1Bh	0001 1001	FIR1C6[7:0]6 (S)							
<i>FIR1C7</i>	1Ch	0010 0100	FIR1C7[7:0] (S)							
<i>ACOEFF1</i>	1Dh	0010 0010	ACOEFF1[7:0]							
<i>BCOEFF1</i>	1Eh	0000 1001	BCOEFF1[7:0]							
<i>CRF1</i>	1Fh	(0000 0000)	CRF1[7:0] (S)							
<i>CETH1</i>	20h	0010 0000	CETH1[7:0]							
<i>SQTH1</i>	21h	0011 1100	SQTH1[7:0]							
<i>CAROFFSET1</i>	22h	0000 0000	CAROFFSET1[7:0] (S)							

## BTSC stereo and SAP

<i>STEREO_CONF</i>	43h	00111000	LOCK_TH_STE[3:0]				LOOP_GAIN[1:0]		FREQ_PI L	RESET
<i>STEREO_FSM_CONF</i>	44h	00001110	0	0	BYPASS	FSM_OF F	GAIN_INI[2:0]		STE_DE M	
<i>STEREO_LEVEL_H</i>	45h	00100000	STE_LEV_H[7:0]							
<i>STEREO_LEVEL_L</i>	46h	00010000	STE_LEV_L[7:0]							
<i>SAP_CONF</i>	47h	00000000	0	0	0	0	0	0	0	SAP_SEL
<i>SAP_LEVEL_H</i>	48h	00100000	SAP_LEV_H[7:0]							
<i>SAP_LEVEL_L</i>	49h	00010000	SAP_LEV_L[7:0]							

Table 4. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>STE_CAR_LEV</i>	4Ah	(00000000)	STE_CAR_LEV[7:0]							
<i>STE_PLL_STAT</i>	4Bh	(00000000)	0	0	LOOP_GAIN[2:0]			OVER	LOCK_DET	STE_DET
<i>STE_SAP_STAT</i>	4Ch	(00000000)	0	OVER	LOCK_DET	STE_DET	0	0	SQ_DET	SAP_DET
<i>PLL_P_GAIN</i>	4Dh	01101100	PLL_P_GAIN[7:0]							
<i>PLL_I_GAIN</i>	4Eh	0000011	0	0	0	0	PLL_I_GAIN[3:0]			
<i>SAP_SQ_TH</i>	4Fh	00110000	SAP_SQ_TH[7:0]							

Analog and I<sup>2</sup>S out control

<i>I2S_ADC_CTRL</i>	56h	0000 1000	I2S_DATA0_CTRL			0	ADC_POWER_UP	ADC_INPUT_SEL[2:0]		
<i>SCART1_2_OUTPUT_CTRL</i>	57h	1010 1000	SC2_MUTE	SC2_OUTPUT_SEL[2:0]			SC1_MUTE	SC1_OUTPUT_SEL[2:0]		
<i>SCART3_OUTPUT_CTRL</i>	58h	0000 1011	0	0	0	0	SC3_MUTE	SC3_OUTPUT_SEL[2:0]		
<i>I2SO_DATA_CTRL</i>	59h	0000 0000	0	I2SO_DATA1_CTRL			0	I2SO_DATA0_CTRL		

Clocking 2

<i>FS2_DIV</i>	5Ah	0001 0001	0	NDIV2[2:0]			0	SDIV2[2:0]		
<i>FS2_MD</i>	5Bh	0001 0001	0	0	0	MD2[4:0]				
<i>FS2_PE_H</i>	5Ch	0101 1100	PE_H2[7:0]							
<i>FS2_PE_L</i>	5Dh	0010 1001	PE_L2[7:0]							

## 10.2 Software registers

Table 5. List of I<sup>2</sup>C registers

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DSP control										
<i>HOST_CMD</i>	80h	0000 0000	0	0	0	0	0	HW_RESET	0	0
<i>IRQ_STATUS</i>	81h	0000 0000	IRQ7	IRQ6	IRQ5 (HP/Srmd unmute ready)	IRQ4 (HP detected)	IRQ3 (I2S SRC input freq change)	IRQ2 (I2S sync found)	IRQ1 (I2S sync lost)	IRQ0 (Autostand)
<i>FW_VERSION</i>	82h	(0000 0001)	SOFT_VERSION[7:0]							
<i>ONCHIP_ALGOS</i>	83h	(0000 0000)	0	0	PROLOGIC_TYPE	MULTI_I2S_IN	TRUBASS	TRUSURROUND	PROLOGIC	MULTICHANNEL_OUT
<i>DSP_STATUS</i>	84h	0000 0000	0	0	0	0	0	0	0	INIT_MEM
<i>DSP_RUN</i>	85h	0000 0000	0	0	0	0	INPUT_CONFIG		REGISTER_RESET	HOST_RUN
<i>I2S_IN_CONFIG</i>	86h	1000 1110	LOCK_MODE_EN	RESET_I2S	0	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE

Table 5. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>I2S_IN_SHIFT_RIGHT</i>	87h	0000 1000	0	0	0	SHIFT_RIGHT_RANGE				
<i>I2S_IN_MASK</i>	88h	0001 1111	0	0	0	WORD_MASK				
<i>I2S_IN_STATUS</i>	89h	1000 0(000)	AUTO_SRC_SYNC	ENABLE_IRQ_SRC_FREQ_CHANGE	ENABLE_IRQ_SYNC_FOUNDED	ENABLE_IRQ_SYNC_LOST	0	I2S_INPUT_FREQ[2:0]		

## Automatic standard detection

<i>AUTOSTD_CTRL</i>	8Ah	0000 0000	SINGLE_SHOT	MONO_SAP_MATRIX_CTRL	FORCE_SQ_SAP	FORCE_SQ_MONO	AUTO_MUTE	SAP_CHECK	STEREO_CHECK	MONO_CHECK
<i>AUTOSTD_TIME</i>	8Bh	0000 1010	0	0	0	STEREO_TIME			FM_TIME	
<i>AUTOSTD_STATUS</i>	8Ch	(0000 0000)	0	0	0	0	SAP_OK	STEREO_OK	MONO_OK	AUTOSTD_ON
<i>AUTOSTD_DEM_STATUS</i>	8Dh	(0000 0000)	0	OVERFLOW	LCK_DET	ST_DET	SAP_SQ	SAP_DET	FM1_CAR	FM1_SQ
<i>I2S_IN_DELAY_CONFIG</i>	8Fh	0000 0111	0	0	SYNC	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE

## Demodulator

<i>BTSC_FINE_PRESCALE_ST</i>	90h	0000 0000	BTSC_FINE_PRESCALE_ST[7:0] (S)								
<i>BTSC_FINE_PRESCALE_SAP</i>	91h	0000 0000	BTSC_FINE_PRESCALE_SAP[7:0] (S)								
<i>BTSC_CONTROL</i>	92h	0010 0000	FINE_PRESCALE_SELECT_SAP	DBX_DEMATRIX		DBX_ON	DEEMPHASIS_CH1		DEEMPHASIS_CH0		
<i>DC_REMOVAL</i>	93h	0011 0111	0	0	DBX_FILTER_SELECT	DEEMPHASIS_FILTER_SELECT	0	DC_DEMOD_POSITION	DC_DEMOD_PRE_ON	DC_SCART_ON	

## Audio preprocessing and selection

<i>PRESCALE_DEMOD_MONO</i>	94h	0000 0000	PRESCALE_DEMOD_SELECT_SAP	PRESCALE_DEMOD_MONO[6:0] (S)							
<i>PRESCALE_DEMOD_STEREO</i>	95h	0000 0000	0	PRESCALE_DEMOD_STEREO[6:0] (S)							
<i>PRESCALE_DEMOD_SAP</i>	96h	0000 0000	0	PRESCALE_DEMOD_SAP[6:0] (S)							
<i>PRESCALE_SCART</i>	97h	0000 0000	0	PRESCALE_SCART[6:0] (S)							
<i>PRESCALE_I2S0</i>	98h	0000 0000	0	PRESCALE_I2S0[6:0] (S)							
<i>PRESCALE_I2S1</i>	99h	0000 0000	0	PRESCALE_I2S1[6:0] (S)							
<i>PRESCALE_I2S2</i>	9Ah	0000 0000	0	PRESCALE_I2S2[6:0] (S)							
<i>PEAK_DETECTOR</i>	9Bh	0000 0000	0	PEAK_LR_RANGE[2:0]			PEAK_DET_INPUT[2:0]			PEAK_DETECT_ON	
<i>PEAK_L</i>	9Ch	0(000 0000)	OVERLOAD_L	PEAK_L[6:0]							

Table 5. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>PEAK_R</i>	9Dh	0(000 0000)	OVERLO AD_R	PEAK_R[6:0]						
<i>PEAK_L_R</i>	9Eh	0(000 0000)	OVERLO AD_L_R	PEAK_L_R[6:0]						

## Matrixing

<i>DOWNMIX_MODE</i>	9Fh	0111 1111	LTRT_OU T_MODE	MIX_OUT_MODE[2:0]			LFE_IN	MIX_IN_MODE[2:0]			
<i>DOWNMIX_DUAL_MO DE</i>	A0h	0000 0000	0	0	0	DUAL_ON	LS_DUAL_SELECT[1: 0]	LTRT_DUAL_SELEC T [1:0]			
<i>DOWNMIX_CONFIG</i>	A1h	0000 0001	0	0	SRND_FACTOR[1:0]		CENTER_FACTOR[1: 0]	LR_UPMI X	NORMAL IZE		
<i>AUDIO_MATRIX1</i>	A2h	0001 0010	0	0	HP_OUT[2:0]			LS_OUT[2:0]			
<i>AUDIO_MATRIX2</i>	A3h	0000 0010	0	0	SCART2_OUT[2:0]			SCART1_OUT[2:0]			
<i>AUDIO_MATRIX3</i>	A4h	0001 0000	0	0	SPDIF_OUT[2:0]			DELAY_OUT[2:0]			
<i>CHANNEL_MATRIX_L S</i>	A5h	0000 0010	AUTOST D_CONT ROL_LS	AUTOST D_CONT ROL_SPD IF	0	0	0	CM_MATRIX_LS[2:0]			
<i>CHANNEL_MATRIX_H P</i>	A6h	0000 0000	AUTOST D_CONT ROL_HP	CM_SOURCE_HP[1:0 ]		CM_POSTION_HP[1:0 ]		CM_MATRIX_HP[2:0]			
<i>CHANNEL_MATRIX_S CART</i>	A7h	0000 0000	AUTOST D_CONT ROL_SCA RT	CM_SOURCE_SCAR T[1:0]		CM_POSTION_SCAR T[1:0]		CM_MATRIX_SCART[2:0]			
<i>CHANNEL_MATRIX_S CARTaux</i>	A8h	0000 0000	AUTOST D_CONT ROL_SCA RTaux	CM_SOURCE_SCAR Taux[1:0]		CM_POSTION_SCAR Taux[1:0]		CM_MATRIX_SCARTaux[2:0]			
<i>CHANNEL_MATRIX_S PDIF</i>	A9h	0000 0000	CM_SOURCE_SPDIF[2:0]			CM_POSTION_SPDIF [1:0]		CM_MATRIX_SPDIF[2:0]			
<i>DEMOD_DC_LEVEL</i>	AAh	(0000 0000)	DEMOD_DC_LEVEL[7:0] (S)								

## Audio processing

<i>AV_DELAY_CONFIG</i>	ADh	0000 0000	0	0	0	0	0	0	DOLBY_ DELAY_ ON	AV_DELA Y_ON	
<i>AV_DELAY_TIME_LS</i>	AEh	0000 0000	AV_DELAY_TIME_LS[7:0]								
<i>AV_DELAY_TIME_HP</i>	AFh	0000 0000	AV_DELAY_TIME_HP[7:0]								
<i>PRO_LOGIC2_CONTR OL</i>	B0h	0111 0110	PL2_LFE	PL2_OUTPUT_DOWNMIX[2:0]			PL2_MODES[2:0]			PL2_ACT IVE	
<i>PRO_LOGIC2_CONFI G</i>	B1h	0000 0000	0	0	0	PL2_SRND_FILTER[1: 0]		PL2_RS_ POLARIT Y	PL2_PAN ORAMA	PL2_AUT OBALAN CE	
<i>PRO_LOGIC2_DIMEN SION</i>	B2h	0000 0000	0	PL2_C_WIDTH[2:0]			0	PL2_DIMENSION[2:0]			
<i>PRO_LOGIC2_LEVEL</i>	B3h	0000 0011	PL2_LEVEL[7:0]								
<i>NOISE_GENERATOR</i>	B4h	0000 0000	10_DB_A TTENUAT E	SRIGHT_ NOISE	SLEFT_ NOISE	SUB_ NOISE	CENTER_ NOISE	RIGHT_ NOISE	LEFT_ NOISE	NOISE_O N	
<i>PCM_SRND_DELAY</i>	B5h	0000 0000	0	0	0	DOLBY_DELAY_SRND[4:0]					

Table 5. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>PCM_CENTER_DELAY</i>	B6h	0000 0000	0	0	0	0	DOLBY_DELAY_CENTER[3:0]			
<i>TRUSRND_CONTROL</i>	B7h	0000 1000	DIALOG_CLARITY_ON	HEADPHONE_ON	TRUSRND_INPUT_MODE[3:0]			TRUSRND_BYPASS	TRUSRND_ON	
<i>TRUSRND_DC_ELEVATION</i>	B8h	0000 1100	TRUSRND_DC_ELEVATION[7:0]							
<i>TRUSRND_INPUT_GAIN</i>	B9h	0000 0000	TRUSRND_INPUT_GAIN[7:0]							
<i>TRUBASS_LS_CONTROL</i>	BAh	0000 0110	0	0	0	0	TRUBASS_LS_SIZE[2:0]		TRUBASS_LS_ON	
<i>TRUBASS_LS_LEVEL</i>	BBh	00001 1001	TRUBASS_LS_LEVEL[7:0]							
<i>TRUBASS_HP_CONTROL</i>	BCh	0000 0110	SRS_TSX_GAIN_ON	0	0	0	TRUBASS_HP_SIZE[2:0]		TRUBASS_HP_ON	
<i>TRUBASS_HP_LEVEL</i>	BDh	0000 1001	TRUBASS_HP_LEVEL[7:0]							
<i>SVC_LS_CONTROL</i>	BEh	0000 0010	0	0	0	0	SVC_LS_INPUT[1:0]	SVC_LS_AMP	SVC_LS_ON	
<i>SVC_LS_TIME_TH</i>	BFh	0000 0000	SVC_LS_TIME[2:0]			SVC_LS_THRESHOLD[4:0] (S)				
<i>SVC_LS_GAIN</i>	C0h	0000 1111	0	0	SVC_LS_MAKE_UP_GAIN[5:0]					
<i>SVC_HP_CONTROL</i>	C1h	0000 0010	0	0	0	0	0	0	SVC_LHP_AMP	SVC_HP_ON
<i>SVC_HP_TIME_TH</i>	C2h	0000 0000	SVC_HP_TIME[2:0]			SVC_HP_THRESHOLD[4:0] (S)				
<i>SVC_HP_GAIN</i>	C3h	0000 1111	0	0	SVC_HP_MAKE_UP_GAIN[5:0]					
<i>WIDESRND_CONTROL</i>	C4h	0000 0100	0	0	0	0	0	WIDESRND_STEREO	WIDESRND_MODE	WIDESRND_ON
<i>WIDESRND_FREQ</i>	C5h	0001 0101	0	0	WIDESRND_BASS[1:0]	WIDESRND_MEDIUM[1:0]	WIDESRND_TREBLE[1:0]			
<i>WIDESRND_LEVEL</i>	C6h	1000 0000	WIDESRND_GAIN[7:0]							
<i>OMNISURROUND_CONTROL</i>	C7h	0000 1100	ST_VOICE[1:0]	SRND_PHASE_INV	OMNISURROUND_INPUT_MODE[3:0]			OMNISURROUND_ON		
<i>DYNAMIC_BASS_LS</i>	C8h	0110 0010	LS_BASS_LEVEL[4:0]				LS_BASS_FREQ[1:0]		LS_DYN_BASS_ON	
<i>DYNAMIC_BASS_HP</i>	C9h	0110 0010	HP_BASS_LEVEL[4:0]				HP_BASS_FREQ[1:0]		HP_DYN_BASS_ON	
<i>EQ_BT_CTRL</i>	CCh	0000 0000	0	0	0	0	0	HP_BT_ON	LS_EQ_BT_SW	LS_EQ_ON
<i>LS_EQ_BANDX</i>	CDh	0000 0000	EQ_BAND1[7:0] (S)							
	CEh	0000 0000	EQ_BAND2[7:0] (S)							
	CFh	0000 0000	EQ_BAND3[7:0] (S)							
	D0h	0000 0000	EQ_BAND4[7:0] (S)							
	D1h	0000 0000	EQ_BAND5[7:0] (S)							
<i>LS_BASS_GAIN</i>	D2h	0000 0000	LS_BASS[7:0] (S)							
<i>LS_TREBLE_GAIN</i>	D3h	0000 0000	LS_TREBLE[7:0] (S)							

Table 5. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>HP_BASS_GAIN</i>	D4h	0000 0000	HP_BASS[7:0] (S)							
<i>HP_TREBLE_GAIN</i>	D5h	0000 0000	HP_TREBLE[7:0] (S)							
<i>OUTPUT_BASS_MNGT</i>	D6h	1000 0000	BASS_M ANAGE_ ON	ST_LFE_ ADD	DOLBY_P ROLOGIC	SUB_ ACTIVE	GAIN_ SWITCH	OCFG_NUM[2:0]		
<i>LS_LOUDNESS</i>	D7h	0000 0100	0	LS_LOUD_THRESHOLD[2:0]			LS_LOUD_GAIN_HR[2:0]			LS_ LOUD_O N
<i>HP_LOUDNESS</i>	D8h	0000 0100	0	HP_LOUD_THRESHOLD[2:0]			HP_LOUD_GAIN_HR[2:0]			HP_ LOUD_O N

## Volume

<i>VOLUME_MODES</i>	D9h	1101 1111	ANTCLIP HP_VOL _CLAMP	ANTICLIP _LS_VOL _CLAMP	0	SCART2_ VOLUME MODE	SCART1_ VOLUME MODE	HP_ VOLUME MODE	SRND_ VOLUME MODE	LS_ VOLUME MODE
<i>LS_L_VOLUME_MSB</i>	DAh	1001 1000	LS_L_VOLUME_MSB[7:0]							
<i>LS_L_VOLUME_LSB</i>	DBh	0000 0000	0	0	0	0	0	0	LS_L_VOLUME_LSB[1:0]	
<i>LS_R_VOLUME_MSB</i>	DCh	0000 0000	LS_R_VOLUME_MSB[7:0]							
<i>LS_R_VOLUME_LSB</i>	DDh	0000 0000	0	0	0	0	0	0	LS_R_VOLUME_LSB[1:0]	
<i>LS_C_VOLUME_MSB</i>	DEh	1001 1000	LS_C_VOLUME_MSB[7:0]							
<i>LS_C_VOLUME_LSB</i>	DFh	0000 0000	0	0	0	0	0	0	LS_C_VOLUME_LSB[1:0]	
<i>LS_SUB_VOLUME_MSB</i>	E0h	1001 1000	LS_SUB_VOLUME_MSB[7:0]							
<i>LS_SUB_VOLUME_LSB</i>	E1h	0000 0000	0	0	0	0	0	0	LS_SUB_VOLUME_LSB[1:0]	
<i>LS_SL_VOLUME_MSB</i>	E2h	1001 1000	LS_SL_VOLUME_MSB[7:0]							
<i>LS_SL_VOLUME_LSB</i>	E3h	0000 0000	0	0	0	0	0	0	LS_SL_VOLUME_LSB[1:0]	
<i>LS_SR_VOLUME_MSB</i>	E4h	0000 0000	LS_SR_VOLUME_MSB[7:0]							
<i>LS_SR_VOLUME_LSB</i>	E5h	0000 0000	0	0	0	0	0	0	LS_SR_VOLUME_LSB[1:0]	
<i>LS_MASTER_VOLUME_MSB</i>	E6h	1110 1000	LS_MASTER_VOLUME_MSB[7:0]							
<i>LS_MASTER_VOLUME_LSB</i>	E7h	0000 0000	0	0	0	0	0	0	LS_MASTER_VOLUME_LSB[1:0]	
<i>HP_L_VOLUME_MSB</i>	E8h	1001 1000	HP_L_VOLUME_MSB[7:0]							
<i>HP_L_VOLUME_LSB</i>	E9h	0000 0000	0	0	0	0	0	0	HP_L_VOLUME_LSB[1:0]	
<i>HP_R_VOLUME_MSB</i>	EAh	0000 0000	HP_R_VOLUME_MSB[7:0]							
<i>HP_R_VOLUME_LSB</i>	EBh	0000 0000	0	0	0	0	0	0	HP_R_VOLUME_LSB[1:0]	
<i>AUX_VOLUME_IN DEX</i>	ECh	0000 0001	0	0	0	0	0	0	AUX_VOLUME_SELECT[1:0]	
<i>AUX_L_VOLUME_MSB</i>	EDh	1101 1101	AUX_L_VOLUME_MSB[7:0]							

Table 5. List of I<sup>2</sup>C registers (continued)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<i>AUX_L_VOLUME_LSB</i>	EEh	0000 0000	0	0	0	0	0	0	AUX_L_VOLUME_LSB[1:0]	
<i>AUX_R_VOLUME_MSB</i>	EFh	0000 0000	AUX_R_VOLUME_MSB[7:0]							
<i>AUX_R_VOLUME_LSB</i>	F0h	0000 0000	0	0	0	0	0	0	AUX_R_VOLUME_LSB[1:0]	

## Mute

<i>MUTE_SOFTWARE</i>	F1h	1111 1111	HP_D_MUTE	SPDIF_D_MUTE	SCART2_D_MUTE	SCART1_D_MUTE	SRND_D_MUTE	SUB_D_MUTE	C_D_MUTE	LS_D_MUTE
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## Beeper

<i>BEEPER_ON</i>	F2h	0000 0000	0	0	0	0	0	BEEPER_SOUND_SELECT[1:0]		BEEPER_ON
<i>BEEPER_MODE</i>	F3h	0100 0011	BEEPER_DECAY[2:0]			BEEPER_DURATION[1:0]		BEEPER_CONTINUOUS	BEEPER_PATH[1:0]	
<i>BEEPER_FREQ_VOL</i>	F4h	0111 0110	BEEPER_FREQ[2:0]			BEEPER_VOLUME[4:0]				

## S/PDIF out configuration

<i>SPDIF_OUT_CHANNEL_STATUS</i>	F5h	0000 0010	0	0	0	0	0	SPDIF_COPYRIGHT	SPDIF_NO_PCM	SPDIF_CONSUMER_PRO
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## Headphone configuration

<i>HEADPHONE_CONFIG</i>	F6h	0000 0010	0	0	SCARTaux_OUT_SELECT		HP_FORCE	HP_LSMUTE	HP_DETECTACTIVE	HP_DETECTED
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## DAC control

<i>DAC_CONTROL</i>	F7h	0001 1111	0	0	SPDIF_MUX	DAC_SCART_MUTE	DAC_SHP_MUTE	DAC_SUBMUTE	DAC_LSLR_MUTE	POWER_UP
<i>SW1_CHANNELS</i>	F8h	0000 0000	C_SUB_SW[1:0]		SUR_HP_SW[1:0]		SCART_SW[1:0]		SPDIF_SW[1:0]	
<i>SW2_CHANNELS</i>	F9h	0000 0000	0	0	0	0	DELAY_SW[1:0]		L_R_SW[1:0]	

## Autostandard coefficients settings

<i>AUTOSTD_COEFF_CTRL</i>	FBh	0000 0001	0	0	0	0	0	0	AUTOSTD_COEFF_CTRL[1:0]	
<i>AUTOSTD_COEFF_INDEX_MSB</i>	FCh	0000 0000	0	0	0	0	0	0	0	AUTOSTD_COEFF_INDEX_MSB
<i>AUTOSTD_COEFF_INDEX_LSB</i>	FDh	0000 0000	AUTOSTD_COEFF_INDEX_LSB[7:0]							
<i>AUTOSTD_COEFF_VALUE</i>	FEh	0000 0000	AUTOSTD_COEFF_VALUE[7:0]							
<i>PATCH_VERSION</i>	FFh	0000 0000	PATCH_VERSION[7:0]							

## 10.3 STV82x8 general control registers

### CUT\_ID Version identification

7	6	5	4	3	2	1	0
0	0	CUT_NUMBER[5:0]					
RO							

**Address:** 00h  
**Type:** RO  
**Reset:** 0000 0001

- [7:6] Reserved
- [5:0] Dice version identification

### RESET Software reset

7	6	5	4	3	2	1	0
BUS_EXP	I2S_CO_EN	I2S_DO_EN	EN_STBY	CLOCK_DOWN	0	SOFT_LRST1	SOFT_RST
R/W							

**Address:** 01h  
**Type:** R/W  
**Reset:** 0000 0000

**Description:** The built-in Automatic Standard Recognition System (Autostandard) can be disabled. In this case, the software reset function (bits SOFT\_LRST1 and SOFT\_LRST2) can be used to implement the Autostandard by I<sup>2</sup>C Software. This is not required if the built-in Autostandard function is used (default)

- [7] Static control by I<sup>2</sup>C of hardware pin BUS\_EXP
- [6] 0 = I<sup>2</sup>S Input (I2S\_SCK, I2S\_LR\_CLK, I2S\_PCM\_CLK in input mode)  
1 = I<sup>2</sup>S Output (I2S\_SCK, I2S\_LR\_CLK, I2S\_PCM\_CLK in output mode)
- [5] 0 = I<sup>2</sup>S Input (I2S\_DATA0 in input mode)  
1 = I<sup>2</sup>S Output (I2S\_DATA0 in output mode)
- [4] Standby mode enabling:  
0: Normal mode  
1: Lock the digital signals before putting the device in standby mode
- [3] Clock down of the DSP decoder.
- [2] Reserved

*Note:* The following register bit is controlled by Autostandard and is forced by default to read-only mode.

- [1] Softreset (active high) of decoder.
- [0] General softreset (active high) to reset all hardware registers except for I<sup>2</sup>C data.



**I2S\_CTRL****I<sup>2</sup>S synchronization control**

7	6	5	4	3	2	1	0
I2S_PLL	SYNC_SIGN	I2S_SRC	LOCK_TH[1:0]		LOCK_MODE	SYNC_CST[1:0]	
R/W							

**Address:** 04h  
**Type:** R/W  
**Reset:** 0000 0001

- [7] I<sup>2</sup>S source synchronization with synthesizer (at 48KHz only) activation:
  - 0: Selected
  - 1: Not selected
- [6] Sign of the loop reversion (to be used in case of gain inversion of the frequency synthesizer)
- [5] SRC I<sup>2</sup>S source activation:
  - 0: ON
  - 1: OFF
- [4:3] Lock detector threshold programming:
  - 00: ±1 CLK period error of accumulation
  - 01: ±2 CLK period error of accumulation
  - 10: ±4 CLK period error of accumulation
  - 11: ±8 CLK period error of accumulation
- [2] Lock detector mode:
  - 0: Lock when accumulation error within lock threshold and LR detected (period counter not saturated)
  - 1: Lock only when accumulation error within lock threshold. Not interested in LR detection
- [1:0] Synchronization time constant. Defines the measurement period of LR:
  - 00: Half period measured (lowest accuracy)
  - 01: One full period measured
  - 10: Two full periods measured
  - 11: Four full periods measured (highest accuracy)

**I2S\_STAT****I<sup>2</sup>S synchronization status**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LR_OFF	LOCK_FLAG
R/W							

**Address:** 05h  
**Type:** R/W  
**Reset:** 0000 0000

- [7:2] Reserved
- [1] LR signal detection:
  - 0: LR signal detected and correct
  - 1: Missing LR pulses detected

[0] Lock flag allowing unmute of audio output

## I2S\_SYNC\_OFFSET                      I<sup>2</sup>S synchronization offset frequency

7	6	5	4	3	2	1	0
I2S_SFO[7:0]							
R/W							

**Address:**        06h  
**Type:**            R/W  
**Reset:**           0000 0000

[7:0] I<sup>2</sup>S synchronization frequency offset ( $\pm 450$  ppm full scale)

## 10.4            Clocking 1

A low-jitter PLL Clock is integrated and can be fully reprogrammed using the registers described below. By default, the programming is defined for a 27-MHz crystal oscillator, which is the frequency recommended for reducing potential RF interference in the application. However, if necessary, the PLL Clock can be re-programmed for other crystal oscillator frequencies within a range from 23 to 30 MHz. Other crystal frequencies can be programmed on your demand.

*Note:*            A crystal frequency change is compatible with other default I<sup>2</sup>C programming including the built-in Automatic Standard Recognition System.

## SYS\_CONFIG                              System configuration control

7	6	5	4	3	2	1	0
SYNC_PLL	OPEN_PLL	INPUT_FREQ[3:0]				BIT[1:0]	
R/W							

**Address:**        07h  
**Type:**            R/W  
**Reset:**           0000 1010

- [7] Status of the loop with the synthesizer:
  - 0: Open
  - 1: Closed
- [6] Force the loop with the synthesizer to be open:
  - 0: No action
  - 1: Loop open
- [5:2] I<sup>2</sup>S Input frequency:
  - 0010: 48 kHz
- [1:0] Reserved

### FS1\_DIV FS1 I/O divider programming

	7	6	5	4	3	2	1	0
EN_PROG	0	NDIV1[1:0]			0	SDIV1[2:0]		
R/W								

**Address:** 08h  
**Type:** R/W  
**Reset:** 0001 0011

- [7] FS1 programming enable:  
 0: FS1 I<sup>2</sup>C register programming ignored by system - FS1 pre-programmed automatically by SYS-CONFIG register (normal use with standard oscillator of 27 MHz)  
 1: FS1 I<sup>2</sup>C register programming used by system - FS1 pre-programming by SYS-CONFIG deactivated (to be used in case of no standard oscillator, other than 27 MHz)
- [6] Reserved
- [5:4] FS1 input clock divider selection
- [3] Reserved
- [2:0] FS1 output clock divider selection

### FS1\_MD FS1 coarse selection

	7	6	5	4	3	2	1	0
0	0	0	MD1[4:0]					
R/W								

**Address:** 09h  
**Type:** R/W  
**Reset:** 0001 0001

- [7:5] Reserved
- [4:0] FS1 Coarse Selection

### FS1\_PE\_H FS1 fine selection (MSBs)

	7	6	5	4	3	2	1	0
PE_H1[7:0]								
R/W								

**Address:** 0Ah  
**Type:** R/W  
**Reset:** 0011 0110

- [7:0] FS1 fine selection (MSBs)

**FS1\_PE\_L** **FS1 fine selection (LSBs)**

7	6	5	4	3	2	1	0
PE_L1[7:0]							
R/W							

**Address:** 0Bh  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] FS1 fine selection (LSBs)

**10.5 Demodulator****DEMOD\_CTRL** **Demodulator control**

7	6	5	4	3	2	1	0
0	0	0	0	0	DEMOD_MODE[2:0]		
R/W							

**Address:** 0Ch  
**Type:** R/W  
**Reset:** 0000 0001

[7:3] Reserved

*Note: This register is controlled by Autostandard and is forced by default to read-only mode.*

[2:0] Demodulator mode selection:

Demod FM

000: Normal

001: Wide

Other configuration: Reserved

**DEMOD\_STAT** **Demodulator detection status**

7	6	5	4	3	2	1	0
0	0	0				FM1_CAR	FM1_SQ
RO							

**Address:** 0Dh  
**Type:** RO  
**Reset:** 0000 0000

[7:2] Reserved

[1] Channel 1 FM carrier detector flag:

0: Not detected  
1: Detected

[0] Channel 1 FM squelch selector flag:

0: Not detected  
1: Detected

*Note:* These registers allow direct access to the demodulator signal detectors.

## AGC\_CTRL

## IF AGC control

7	6	5	4	3	2	1	0
0	0	IF_SELECT	AGC_REF[2:0]			AGC_CST[1:0]	
R/W							

**Address:** 0Eh

**Type:** R/W

**Reset:** 0001 0001

[7:6] Reserved

[5] Selection of the IF input:

0: IF input SIF 1  
1: IF input SIF 2

[4:2] Defines the clipping level which adjusts the allowable proportion of samples at the input of the ADC which will be clipped. The AGC tries to maximize the use of the full scale range of the ADC. The default setting gives a ratio of 1/256.

### Clipping ratio

000: 1/16 (single carrier)  
001: 1/32  
010: 1/64  
011: 1/128  
100: 1/256 (default)  
101: 1/512  
110: 1/1024  
111: 1/2048 (multiple carriers)

[1:0] AGC time constant

This is the time constant between each step of 1.5 dB by the AGC.

### Step duration (ms)

00: 1.33  
01: 1.33  
10: 2.66  
11: 5.33  
11: 10.66

**AGC\_GAIN****IF AGC control and status**

7	6	5	4	3	2	1	0
0	AGC_ERR[4:0]				SIG_OVER	SIG_UNDER	
R/W							

**Address:** 0Fh  
**Type:** R/W  
**Reset:** 0000 0000

[7] Reserved

[6:2] Amplifier gain control. This is the AGC gain control value. There are 20 steps of +1.5 dB (see Note below):

00000: Gain-min  
 10100: Gain-min + 30 dB  
 11111: Gain-min + 30 dB

[1] AGC input signal upper threshold:  
 0: Normal signal  
 1: Signal too large and AGC overloaded

[0] AGC input signal lower threshold:  
 0: Normal signal  
 1: Signal too small and AGC is underloaded

When the AGC is in automatic mode (AGC\_CMD = 0), bits SIG\_OVER and SIG\_UNDER indicate if the input signal is too small/large and the AGC is under/overloaded. This is useful when setting the STV82x8 SIF input level.

**DC\_ERR\_IF****DC offset status for IF ADC**

7	6	5	4	3	2	1	0
DC_ERR[7:0]							
RO							

**Address:** 10h  
**Type:** RO  
**Reset:** 0000 0000

[7:0] DC offset error of IF ADC output

**10.6 Demodulator channel 1****CARFQ1H****Channel 1 carrier DCO frequency**

7	6	5	4	3	2	1	0
CARFQ1H[23:16]							
R/W							

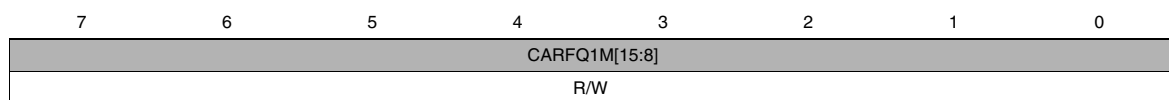
**Address:** 12h  
**Type:** R/W  
**Reset:** 0010 1110

[7:0] Channel 1 DCO carrier frequency (8 MSBs).

*Note:* This register is controlled by Autostandard and is forced by default to read-only mode

### CARFQ1M Channel carrier DCO frequency

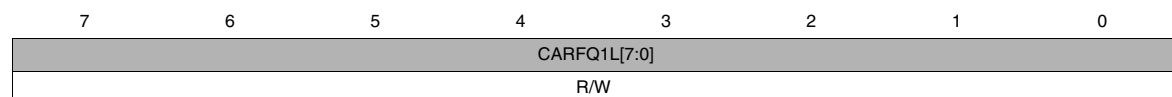
**Address:** 13h  
**Type:** R/W  
**Reset:** 1110 0000



[7:0] Channel 1 DCO carrier frequency.

*Note:* This register is controlled by Autostandard and is forced by default to read-only mode

### CARFQ1L Channel 1 carrier DCO frequency



**Address:** 14h  
**Type:** R/W  
**Reset:** 0000 0000

[7]:0 Channel 1 DCO carrier frequency (8 LSBs), see [Table 6](#).

*Note:* This register is controlled by Autostandard and is forced by default to read-only mode.

**Table 6. Mono carrier frequencies by system**

System	Mono carrier frequency. (MHz)	CARFQ1[23:0] (dec)	CARFQ1[23:0]
M/N	4.5	3072000	2EE000h

*Note:* Carrier frequency:  $CARFQ1(dec) \cdot f_S / 2^{24}$  with  $f_S = 24.576$  MHz (crystal oscillator frequency independent)

## FIR1C[0:7]

## Channel 1 FIR coefficients

7	6	5	4	3	2	1	0
FIR1C0[7:0] to FIR1C7[7:0]							
R/W							

**Address:** 15h

**Type:** R/W

**Reset:** 0000 0001

Bitfield	Description					
	(reset state)					
	FM 27 kHz	FM 50 kHz	FM 200 kHz	FM 350 kHz	FM 500 kHz	BTSC
FIR1C0[7:0]	FFh	00h	00h	02h	01h	01h
FIR1C1[7:0]	FEh	FEh	01h	01h	00h	00h
FIR1C2[7:0]	FEh	FCh	01h	FCh	04h	FEh
FIR1C3[7:0]	00h	FDh	FCh	03h	FAh	FCh
FIR1C4[7:0]	06h	02h	08h	04h	05h	00h
FIR1C5[7:0]	0Eh	0Dh	F6h	F2h	00h	0Bh
FIR1C6[7:0]	16h	18h	F8h	06h	F2h	19h
FIR1C7[7:0]	1Bh	1Fh	4Ah	43h	4Dh	24h

*Note:* The above registers are controlled by Autostandard and are forced by default to read-only mode.

## ACOEFF1

## Channel 1 baseband PLL loop filter proportional coefficient

7	6	5	4	3	2	1	0
ACOEFF1[7:0]							
R/W							

**Address:** 1Dh

**Type:** R/W

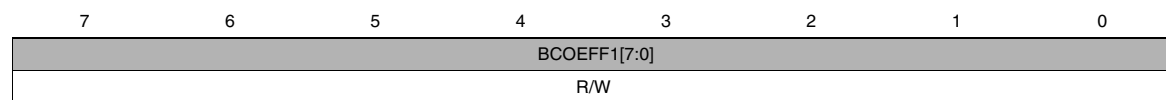
**Reset:** 0010 0010

[7]:0 Used to program the proportional coefficient of the baseband PLL loop filter (channel 1)  
 Defines the damping factor of the loop. For values, refer to [Table 7](#).

*Note:* This register is controlled by Autostandard and is forced by default to read-only mode.



**BCOEFF1** **Channel 1 baseband PLL loop filter integral coefficient & DCO gain**



**Address:** 1Eh  
**Type:** R/W  
**Reset:** 0000 1001

[7]:0 Used to program the integral coefficient of the baseband PLL loop filter and DCO gain. Defines the bandwidth of the loop. For values, refer to [Table 7](#).

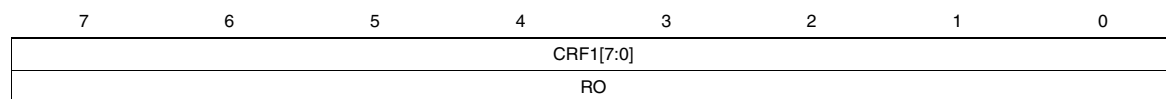
*Note: This register is controlled by Autostandard and is forced by default to read-only mode*

**Table 7. Baseband PLL loop filter adjustment (FM mode)**

FM Mode	Small	Standard	Medium	Wide*	BTSC
ACOEFF	10h	22h	2Ch	2Ch	22h
BCOEFF	1Ah	12h	0Ah	0Ah	09h
FM_DEV max (kHz)	62.5	125	250	500	500
DCO Range (kHz)	96	192	384	768	768

(\*) Refer to [DEMOD\\_CTRL](#) (DEMOD\_MODE[2:0])

**CRF1** **Channel 1 baseband PLL demodulator offset**



**Address:** 1Fh  
**Type:** RO  
**Reset:** 0000 0000

[7:0] Channel 1 carrier recovery frequency. Displays the instantaneous frequency offset of the channel 1 baseband PLL demodulator.

**CETH1****Channel 1 FM carrier level threshold**

7	6	5	4	3	2	1	0
CETH1[7:0]							
R/W							

**Address:** 20H  
**Type:** R/W  
**Reset:** 0010 0000

[7:0] This register is used to compare the carrier level in the channel and the threshold value. This level is measured after the channel filter and is relative to the full scale reference level (0 dB). This is used as part of the validation of an FM signal, if the carrier level is below the threshold, the signal is considered to be non-valid. Recommended value is 10h.

<u>CETH</u>	<u>Threshold (dB)</u>
FFh	-6
80h	-12
40h	-18
20h	-24 (default)
10h	-32 (recommended value)
08h	-38
OFF	(all carrier levels are accepted)

**SQTH1****Channel 1 FM squelch threshold**

7	6	5	4	3	2	1	0
SQTH1[7:0]							
R/W							

**Address:** 21h  
**Type:** R/W  
**Reset:** 0011 1100

[7:0] The squelch detector measures the level of high frequency noise and compares it to the threshold level (SQTH). If the level is below this value, the S/N of the FM signal is considered to be acceptable. Values are given for FM with standard deviation.

<u>SQTH</u>	<u>S/N (dB)</u>
FA	h0
77	h10
3C	h15 (default)
23	h20
19	h25

## CAROFFSET1 Channel 1 DCO carrier offset compensation

7	6	5	4	3	2	1	0
CAROFFSET1[7:0] (S)							
R/W							

**Address:** 22h  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] This value is used to correct the carrier frequency offset of the incoming IF signal. Automatic frequency control in FM mode can be implemented by registers [DC\\_REMOVAL](#).

A DCO frequency offset (in two's complement format) is added to the pre-programming value by AUTOTSD in the CARFQ1 registers (corresponding to the standard IF carrier frequency). The programmable carrier offset ranges from -192 kHz to +190.5 kHz with a resolution of 1.5 kHz.

For standard FM deviation, the value displays by [DC\\_REMOVAL](#) can be directly loaded in CAROFFSET1 to exactly compensate the carrier offset on Channel 1

## STEREO\_CONF BTSC stereo configuration

7	6	5	4	3	2	1	0
LOCK_TH_STE[7:4]				LOOP_GAIN[1:0]		FREQ_PIL	RESET
R/W							

**Address:** 43h  
**Type:** R/W  
**Reset:** 0011 1000

[7:4] BTSC lock stereo threshold

[3:2] Gain of stereo PLL:

- 00: Gain \* 4
- 01: Gain \* 2
- 10: Gain (default)
- 11: Gain / 2

[1] Pilot frequency selection:

- 0: 15.625-15.734 kHz
- 1: Reserved

*Note:* The following register bit is controlled by Autostandard and is forced by default to read-only mode

[0] Stereo reset:

- 1: Reset active.

**STEREO\_FSM\_CONF**      **BTSC finite state machine configuration**

7	6	5	4	3	2	1	0
0	0	BYPASS	FSM_OFF	GAIN_INI[2:0]			STE_DEM
R/W							

**Address:** 44h  
**Type:** R/W  
**Reset:** 0000 1110

- [7:6] Reserved
- [5] Bypass of the stereo block:
  - 0: Stereo block is on
  - 1: Stereo block is bypassed
- [4] FSM switch off:
  - 0: FSM is on
  - 1: FSM is off. Gain set by I<sup>2</sup>C
- [3:1] Initial loop gain for FSM
  - [0] Stereo dematrix inside the stereo block (before DBX):
    - 1: Reset active

**STEREO\_LEVEL\_H**      **BTSC threshold high for stereo detection**

7	6	5	4	3	2	1	0
STE_LEV_H[7:0]							
R/W							

**Address:** 45h  
**Type:** R/W  
**Reset:** 0010 0011

[7:0] Threshold high for stereo detection. If carrier level is > STE\_LEV\_H, stereo is detected.

*Note:* This parameter can only be modified when AUTO STANDARD is off.

**STEREO\_LEVEL\_L**      **BTSC threshold low for stereo detection**

7	6	5	4	3	2	1	0
STE_LEV_L[7:0]							
R/W							

**Address:** 46h  
**Type:** R/W  
**Reset:** 0000 1100

[7:0] Threshold low for stereo detection. If carrier level is <STE\_LEV\_L, stereo is no longer detected.

Note: This parameter can only be modified when AUTO STANDARD is off.

**SAP\_CONF BTSC SAP selection**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SAP_SEL
R/W							

**Address:** 47h  
**Type:** R/W  
**Reset:** 0000 0000

[7:1] Reserved

Note: The following register bit is controlled by Autostandard and is forced by default to read-only mode.

- [0] Selection of the SAP:
  - 0: Stereo selected
  - 1: SAP is selected on second channel

**SAP\_LEVEL\_H BTSC threshold high for SAP detection**

7	6	5	4	3	2	1	0
SAP_LEV_H[7:0]							
R/W							

**Address:** 48h  
**Type:** R/W  
**Reset:** 0101 0000

[7:0] Threshold high for SAP detection. If SAP signal level is > SAP\_LEV\_H, SAP is detected.

Note: This parameter can only be modified when AUTO STANDARD is off.

**SAP\_LEVEL\_L BTSC threshold low for SAP detection**

7	6	5	4	3	2	1	0
SAP_LEV_L[7:0]							
R/W							

**Address:** 49h  
**Type:** R/W  
**Reset:** 0011 0000

[7:0] Threshold low for SAP detection. If sap signal level is <SAP\_LEV\_L, SAP is no longer detected.

*Note:* This parameter can only be modified when AUTO STANDARD is off.

### STE\_CAR\_LEV BTSC stereo carrier level

7	6	5	4	3	2	1	0
STE_CAR_LEV[7:0]							
RO							

**Address:** 4Ah  
**Type:** RO  
**Reset:** 0000 0000

[7:0] Stereo carrier level

### STE\_PLL\_STAT BTSC stereo PLL status

7	6	5	4	3	2	1	0
0	0	LOOP_GAIN[3:0]			OVER	LOCK_DET	STE_DET
RO							

**Address:** 4Bh  
**Type:** RO  
**Reset:** 0000 0000

- [7:6] Reserved
- [5:3] Final FSM gain at the end of the stereo search process
  - [2] Overflow append in stereo search process:
    - 1: Overflow
  - [1] Stereo PLL lock status:
    - 0: No lock on pilot
    - 1: Lock on pilot or no pilot detected (no stereo)
  - [0] Stereo detection:
    - 0: No stereo detected
    - 1: Stereo detected

**STE\_SAP\_STAT****BTSC stereo SAP status**

7	6	5	4	3	2	1	0
0	OVER	LOCK_DET	STE_DET	0	0	SQ_DET	SAP_DET
RO							

**Address:** 4Ch**Type:** RO**Reset:** 0000 0000

- [7] Reserved
- [6] Overflow append in stereo search process:  
1: Overflow
- [5] Stereo PLL lock status:  
0: No lock on pilot  
1: Lock on pilot or no pilot detected (no stereo)
- [4] Stereo detection:  
0: No stereo detected  
1: Stereo detected
- [3:2] Reserved
- [1] Squelch detection of SAP;  
0: Problem with noise  
1: Level of noise is good
- [0] Signal detection of SAP:  
0: SAP not detected  
1: SAP detected

**PLL\_P\_GAIN****BTSC PLL proportional gain**

7	6	5	4	3	2	1	0
PLL_P_G[7:0]							
R/W							

**Address:** 4Dh**Type:** R/W**Reset:** 0110 1100

- [7:0] PLL proportional gain

**PLL\_I\_GAIN****BTSC PLL integral gain**

7	6	5	4	3	2	1	0
0	0	0	0	PLL_I_G[3:0]			
R/W							

**Address:** 4Eh**Type:** R/W**Reset:** 0000 0011

[7:4] Reserved

[3:0] PLL integral gain

**SAP\_SQ\_TH****SAP squelch threshold**

7	6	5	4	3	2	1	0
SAP_SQ_TH[7:0]							
R/W							

**Address:** 4Fh**Type:** R/W**Reset:** 0011 0000

[7:0] SAP squelch threshold

**10.7 I<sup>2</sup>S and analog control****I2S\_ADC\_CTRL****I2S\_DATA0 and ADC input selection and power-up****Address:** 56h**Type:** R/W**Reset:** 0000 1000

7	6	5	4	3	2	1	0
I2S_DATA0_CTRL[2:0]			0	ADC_ POWER_UP	ADC_INPUT_SEL[2:0]		
R/W							



**SCART1\_2\_OUTPUT\_CTRL      SCART 1\_2 output selection and mute**

7	6	5	4	3	2	1	0
SC2_MUTE	SC2_OUTPUT_SEL[2:0]			SC1_MUTE	SC1_OUTPUT_SEL[2:0]		
R/W							

**Address:** 57h  
**Type:** R/W  
**Reset:** 1010 1000

[7] Mute command for the output SCART 2:

- 0: Output not muted
- 1: Output muted

[6:4] Selection of the output SCART 2 configuration:

- 000: DSP
- 001: Input mono
- 010: Input SCART 1 (def) (B SDIP 64)
- 011: Input SCART 2 (res. SDIP 64)
- 100: Input SCART 3 (res. SDIP 64)
- 101: Input SCART 4 (res. SDIP 64)
- 110: Input SCART (res. TQFP) (A SDIP 64) (1\_BIS)
- 111: Input SCART (5 TQFP 100) (C SDIP 64) (3\_BIS)

[3] Mute command for the output SCART 1:

- 0: Output not muted
- 1: Output muted

[2:0] Selection of the output SCART 1 configuration:

- 000: DSP (default)
- 001: Input mono
- 010: Input SCART 1 (B SDIP 64)
- 011: Input SCART 2 (res SDIP 64)
- 100: Input SCART 3 (res. SDIP 64)
- 101: Input SCART 4 (res. SDIP 64)
- 110: Input SCART (res. TQFP) (A SDIP 64) (1\_BIS)
- 111: Input SCART (5 TQFP100) (C SDIP64) (3\_BIS)

**SCART3\_OUTPUT\_CTRL      SCART 3 output selection and mute**

7	6	5	4	3	2	1	0
0	0	0	0	SC3_MUTE	SC3_OUTPUT_SEL[2:0]		
R/W							

**Address:** 58h  
**Type:** R/W  
**Reset:** 0000 10111

[7:4] Reserved

- [3] Mute command for the output SCART 3:
  - 0: Output not muted
  - 1: Output muted
- [2:0] Selection of the output SCART 3 configuration:
  - 000: DSP
  - 001: Input mono
  - 010: Input SCART 1 (B SDIP)
  - 011: Input SCART 2 (default)
  - 100: Input SCART 3 (res. SDIP 64)
  - 101: Input SCART 4 (res. SDIP 64)
  - 110: Input SCART (res. TQFP) (A SDIP64) (1\_BIS)
  - 111: Input SCART (5 TQFP 100) (C SDIP 64) (res. SDIP 64) (3\_BIS)

**I2SO\_DATA\_CTRL                      I<sup>2</sup>S data source control**

	7	6	5	4	3	2	1	0
	0	I2SO_DATA1_CTRL[2:0]			0	I2SO_DATA0_CTRL[2:0]		
R/W								

**Address:**            59h  
**Type:**                R/W  
**Reset:**                0000 0000

- [7] Reserved
- [6:4] Source selection for I2SO\_DATA1 output:
  - 000: Mute
  - 001: LR
  - 010: HP\_LSS
  - 011: LS\_C and LS\_SUB
  - 100: SCART DAC
  - 101: S/PDIF\_OUT
  - 110: Delay
  - 111: Mute
- [3] Reserved
- [2:0] Source selection for I2SO\_DATA0 output:
  - 000: Mute
  - 001: LR
  - 010: HP\_LSS
  - 011: LS\_C and LS\_SUB
  - 100: SCART DAC
  - 101: S/PDIF\_OUT
  - 110: Delay
  - 111: Mute

## 10.8 Clocking 2

### FS2\_DIV FS2 I/O divider programming

7	6	5	4	3	2	1	0
0	0	NDIV2[1:0]		0	SDIV2[2:0]		

**Address:** 5Ah  
**Type:** R/W  
**Reset:** 0010 0001

- [7:6] Reserved
- [5:4] FS2 Input clock divider selection
- [3] Reserved
- [2:0] FS2 Output clock divider selection

### FS2\_MD FS2 coarse selection

7	6	5	4	3	2	1	0
0	0	0	MD2[4:0]				
R/W							

**Address:** 5Bh  
**Type:** R/W  
**Reset:** 0001 0001

- [7:5] Reserved
- [4:0] FS2 coarse selection

### FS2\_PE\_H FS2 fine selection (MSBs)

7	6	5	4	3	2	1	0
PE_H2[7:0]							
R/W							

**Address:** 5Ch  
**Type:** R/W  
**Reset:** 0101 1100

- [7:0] FS2 fine selection (MSBs)

**FS2\_PE\_L** **FS2 fine selection (LSBs)**

7	6	5	4	3	2	1	0
PE_L2[7:0]							
R/W							

**Address:** 5Dh  
**Type:** R/W  
**Reset:** 0010 1001

[7:0] FS2 fine selection (LSBs)

**10.9 DSP control****HOST\_CMD** **DSP hardware control**

7	6	5	4	3	2	1	0
0	0	0	0	0	HW_RESET	0	0
R/W							

**Address:** 80h  
**Type:** R/W  
**Reset:** 0000 0000

[7:3] Reserved

[2] DSP hardware run when set, see [Figure 26](#).

[1:0] Reserved

**IRQ\_STATUS** **IRQ status**

7	6	5	4	3	2	1	0
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
R/W							

**Address:** 81h  
**Type:** R/W  
**Reset:** 0000 0000

[7:6] Reserved

[5] Hp/Srnd DAC unmute ready IRQ

[4] HP detected IRQ

[3] I<sup>2</sup>S SRC frequency change detected IRQ

[2] I<sup>2</sup>S sync found IRQ

- [1] I<sup>2</sup>S sync lost IRQ
- [0] Autostandard IRQ

**FW\_VERSION****Embedded firmware version**

7	6	5	4	3	2	1	0
FW_VERSION[7:0]							
RO							

**Address:** 82h  
**Type:** RO  
**Reset:** 0000 0001

[7:0] Version of the embedded software.

**ONCHIP\_ALGOS****Display algorithms available on the chip**

7	6	5	4	3	2	1	0
0	0	PROLOGIC_TY PE	MULTI_I2S_IN	TRUBASS	TRU SURROUND	PROLOGIC	MULTICHANNEL _OUT
RO							

**Address:** 83h  
**Type:** RO  
**Reset:** 0000 0000

- [7:6] Reserved
- [5] 0: Pro Logic 1  
1: Pro Logic 2
- [4] 0: 1 I<sup>2</sup>S input  
1: 3 I<sup>2</sup>S inputs
- [3] SRS TruBass algorithm is present when set.
- [2] SRS TruSurround algorithm is present when set.
- [1] Dolby Pro Logic algorithm is present when set.
- [0] Multi-channel output is present when set.

**DSP\_STATUS**                      **DSP status**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	INIT_MEM
RO							

**Address:**        84h  
**Type:**            RO  
**Reset:**            0000 0000

- [7:1] Reserved  
 [0] DSP initialization:  
      0: DSP is not initialized  
      1: DSP is initialized

**DSP\_RUN**                              **DSP configuration and run**

7	6	5	4	3	2	1	0
0	0	0	0	INPUT_CONFIG	REGISTERS_R ESET	HOST_RUN	
R/W							

**Address:**        85h  
**Type:**            R/W  
**Reset:**            0000 0000

- [7:4] Reserved  
 [3:2] 00: BTSC + I2S SRC + I2S DELAY + ADC  
      01: BTSC + I2S 48K + I2S DELAY + ADC  
      10: Not used  
      11: BTSC + MULTI I2S 48K + ADC  
 [1] 0: 2C register table is not initialized when soft reset  
      1: 2C register table is initialized when soft reset  
 [0] 0: Soft reset DSP  
      1: Start DSP processing

**I2S\_IN\_CONFIG**                      **I<sup>2</sup>S configuration**

7	6	5	4	3	2	1	0
LOCK_MODE_E N	RESET_I2S	SYNC	LRCLK_START	LRCLK_POLA RITY	SCLK_POLA RITY	DATA_CFG	I2S_MODE
R/W							

**Address:**        86h  
**Type:**            R/W  
**Reset:**            1000 0111

- [7] Enable lock mode for external I<sup>2</sup>S input:  
0: Disable lock mode for external I<sup>2</sup>S input  
1: Enable lock mode for external I<sup>2</sup>S input
- [6] Reset I<sup>2</sup>S input sync when set
- [5] I<sup>2</sup>S Synchronization:  
0: Direct capture  
1: Wait for sync signal
- [4] According to LRCLK POLARITY, first data take:  
0: Left  
1: Right
- [3] Polarity of the left data
- [2] 0: Falling edge  
1: Rising edge
- [1] 0: LSB first  
1: MSB first
- [0] 0: Not standard mode  
1: Standard mode

*Note:* This register must be set before the Start of the Software (85h: HOST\_RUN = 1).

### I2S\_IN\_SHIFT\_RIGHT      I<sup>2</sup>S shift right

7	6	5	4	3	2	1
0	0	0	SHIFT_RIGHT_RANGE[4:0]			
R/W						

**Address:**      87h  
**Type:**        R/W  
**Reset:**        0000 1000

- [7:5] Reserved
- [4:0] Defines the shift right to apply to 32-bit input samples. Range: 0 to 31

*Note:* This register has to be set before starting the software (0x85 : HOST\_RUN = 1).

### I2S\_IN\_MASK            I<sup>2</sup>S mask

7	6	5	4	3	2	1	0
0	0	0	WORD_MASK[4:0]				
R/W							

**Address:**      88h  
**Type:**        R/W  
**Reset:**        0001 1111

[7:5] Reserved

[4:0] Defines the mask to apply to 32-bit input samples. Range: 0 to 31

*Note:* This register has to be set before starting the software (0x85 : HOST\_RUN = 1).

**I2S\_IN\_STATUS SRC I<sup>2</sup>S input behavior**

7	6	5	4	3	2	1	0
AUTO_SRC_SYNC	ENABLE_IRQ_SRC_FREQ_CHANGE	ENABLE_IRQ_SYNC_FOUND	ENABLE_IRQ_SYNC_LOST	0	I2S_INPUT_FREQ		
R/W							

**Address:** 89h  
**Type:** R/W  
**Reset:** 1000 0000

- [7] Allow the DSP to reset the SRC input DMA when an input freq change is detected. (Working in SRC mode only):  
 0: No reset on input frequency change  
 1: Reset on input frequency change
- [6] Generate an IRQ3 when a frequency change is detected on SRC input. (Working in SRC mode only):  
 0: RQ3 generation not active  
 1: RQ3 generation active
- [5] Generate an IRQ2 when a signal is synchronized on SRC input. (Working in SRC mode only):  
 0: RQ2 generation not active  
 1: RQ2 generation active
- [4] Generate an IRQ1 when a signal is lost on SRC input. (Working in SRC mode only):  
 0: RQ1 generation not active  
 1: RQ1 generation active
- [3] Reserved
- [2:0] Display the frequency detected on SRC input:  
 000: No signal locked on SRC input  
 001: 32 kHz  
 010: 44.1 kHz  
 011: 48 kHz  
 100: Signal locked but frequency unknown  
 101: Not used  
 110: Not used  
 111: Not used



## 10.10 Automatic standard recognition

### AUTOSTD\_CTRL

### Automatic standard recognition control

7	6	5	4	3	2	1	0
SINGLE_SHOT	MONO_SAP_CT RL_MATRIX	FORCE_SQ_SA P	FORCE_SQ_M ONO	AUTO_MUTE	SAP_CHECK	STEREO_CHEC K	MONO_CHECK
R/W							

**Address:** 8Ah

**Type:** R/W

**Reset:** 0000 0000

- [7] Single-shot mode (to be selected with any of the Mono/Stereo or Sap check bits):
  - 0: Single Shot mode is not selected
  - 1: Single Shot mode is selected<sup>(1)</sup>
- [6] Changes the behavior of the automatic matrix control for SAP language:
  - 0: When SAP signal is detected, the SAP signal is outputted on both left and right channels
  - 1: When SAP signal is detected, mono signal is outputted on the left channel and the SAP signal is outputted on the right channel
- [5] Force the squelch status during SAP detection by autostandard.
  - 0: SAP squelch from demod status
  - 1: SAP squelch forced to 1
- [4] Force the squelch status during MONO detection by AutoStandard.
  - 0: MONO squelch from demod status
  - 1: MONO squelch forced to 1
- [3] 0: Output channels are never muted  
1: Output channels are automatically muted when no signal is detected
- [2] 0: No SAP standard research  
1: SAP standard research
- [1] 0: No STEREO standard research  
1: STEREO standard research (priority is given to SAP if selected)
- [0] 0: No MONO standard research (Autostandard OFF)  
1: MONO standard research (mandatory to activate Autostandard)

1. **Single\_Shot** mode pre-programs demodulator registers in a chosen standard (bits b2, b1, b0).  
Autostandard is switched OFF (Mono\_check = 0) after the programming of the registers.

**AUTOSTD\_TIME**                      **Detection time-out**

7	6	5	4	3	2	1	0
0	0	0	STEREO_TIME[2:0]			FM_TIME[1:0]	
R/W							

**Address:**        8Bh  
**Type:**            R/W  
**Reset:**           0000 1010

- [7:5] Reserved
- [4:2] Stereo detection time-out:  
 000: 20 ms (default)  
 001: 40 ms  
 010: 100 ms  
 011: 200 ms  
 100: 400 ms  
 101: 800 ms  
 110: 1200 ms  
 111: 1600 ms
- [1:0] FM detection time-out:  
 00: 16 ms  
 01: 32 ms  
 10: 48 ms (default)  
 11: 64 ms

*Note:*            The time-out default value is optimum and does not normally need to be changed.

**AUTOSTD\_STATUS**                      **Detection standard status**

7	6	5	4	3	2	1	0
0	0	0	0	SAP_OK	STEREO_OK	MONO_OK	AUTOSTD_ON
RO							

**Address:**        8Ch  
**Type:**            RO  
**Reset:**           0000 0000

- [7:4] Reserved
- Note:*            The following register bits are controlled by Autostandard and are forced by default to read-only mode
- [3] SAP standard recognition status:  
 0: SAP standard not detected  
 1: SAP standard detected
- [2] Stereo standard recognition status:  
 0: Stereo standard not detected  
 1: Stereo standard detected

- [1] Mono standard recognition status:  
 0: Mono Standard not detected  
 1: Mono Standard detected
- [0] Automatic Standard Recognition System status:  
 0: Automatic Standard Recognition System is OFF  
 1: Automatic Standard Recognition System is ON

## AUTOSTD\_DEM\_STATUS Demodulator status

7	6	5	4	3	2	1	0
0	OVERFLOW	LCK_DET	ST_DET	SAP_SQ	SAP_DET	FM1_CAR	FM1_SQ
RO							

**Address:** 8Dh  
**Type:** RO  
**Reset:** 0000 0000

- [7] Reserved

*Note: The following register bits are controlled by Autostandard and are forced by default to read-only mode*

- [6] Overflow
- [5] Lock detection:  
 0: Stereo lock not detected  
 1: Stereo lock detected
- [4] Stereo lock detection:  
 0: Stereo not detected  
 1: Stereo detected
- [3] SAP squelch detection:  
 0: SAP squelch not detected  
 1: SAP squelch detected
- [2] SAP detection:  
 0: SAP not detected  
 1: SAP detected
- [1] FM1 carrier detection:  
 0: FM1 carrier not detected  
 1: FM1 carrier detected
- [0] FM1 squelch detection:  
 0: FM1 squelch not detected  
 1: FM1 squelch detected

**I2S\_IN\_DELAY\_CONFIG**      **I<sup>2</sup>S configuration for delay input**

7	6	5	4	3	2	1	0
0	0	SYNC	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE
R/W							

**Address:**        8Fh  
**Type:**            R/W  
**Reset:**            1000 1110

- [7:6] Reserved
- [5] I<sup>2</sup>S Synchronization:
  - 0: Direct capture
  - 1: Wait for synchronization signal
- [4] According to LRCLK POLARITY, first data take:
  - 0: Left
  - 1: Right
- [3] Polarity of the left data
  - 0: Falling edge
  - 1: Rising edge
- [2] 0: LSB first
  - 1: MSB first
- [1] 0: Not standard mode
  - 1: Standard mode

*Note:*        For this input, the *SHIFT\_RIGHT* and *MASK* of the I<sup>2</sup>S input are set.  
*SHIFT\_RIGHT* = 0x08  
*MASK* = 0x1F

**10.11 Demodulator****BTSC\_FINE\_PRESCALE\_ST**      **BTSC input prescale for stereo mode**

7	6	5	4	3	2	1	0
BTSC_FINE_PRESCALE_ST[7:0] (S)							
R/W							

**Address:**        90h  
**Type:**            R/W  
**Reset:**            0000 0000

[7:0] Set the prescale of the signal coming from the demodulator when STEREO is demodulated in order to optimize the signal level at DBX block input (steps of 0.02 dB):

1000 0000: -2.56 dB

...

0000 0000: 0 dB

0000 0001: 0.02 dB

...

0111 1111: 2.54 dB

**BTSC\_FINE\_PRESCALE\_SAP****BTSC input prescale for SAP mode**

7	6	5	4	3	2	1	0
BTSC_FINE_PRESCALE_SAP[7:0] (S)							
R/W							

**Address:** 91h

**Type:** R/W

**Reset:** 0000 0000

[7:0] Set the preschool of the signal coming from the demodulator when SAP is demodulated in order to optimize the signal level at DBX block input (steps of 0.02 dB):

1000 0000: -2.56 dB

...

0000 0000: 0 dB

0000 0001: 0.02 dB

...

0111 1111: 2.54 dB

**BTSC\_CONTROL****BTSC back-end decoder control**

7	6	5	4	3	2	1	0
FINE_PRESCALE_SELECT_SAP	DBX_DEMATRIX[1:0]	DBX_ON	DEEMPHASIS_CH1[1:0]	DEEMPHASIS_CH0[1:0]			
RO							

**Address:** 92h

**Type:** RO

**Reset:** 0000 0000

*Note: This register is controlled by Autostandard and is forced by default to read-only mode.*

[7] Select the prescale value to apply on second channel before DBX:

0: STEREO prescale (register 90h)

1: SAP prescale (register 91h)

- [6:5] Select L/R dematrix for STEREO standard
  - 00: No dematrixing (mono or SAP)
  - 01: L/R dematrix (STEREO):  $L=Ch0+(Ch1)/2$ ,  $R=Ch0-(Ch1)/2$
  - 10: Reserved
  - 11: Reserved
- [4] 0: DBX noise reduction not active
  - 1: DBX noise reduction active on second channel (STEREO or SAP)
- [3:2] Select the de-emphasis for demodulator second channel:
  - 00: No de-emphasis
  - 01: 25  $\mu$ s de-emphasis
  - 10: 50  $\mu$ s de-emphasis
  - 11: 75  $\mu$ s de-emphasis
- [1:0] Select the de-emphasis for demodulator first channel:
  - 00: No de-emphasis
  - 01: 25  $\mu$ s de-emphasis
  - 10: 50  $\mu$ s de-emphasis
  - 11: 75  $\mu$ s de-emphasis

**DC\_REMOVAL**

**DC removal**

	7	6	5	4	3	2	1	0
0	0	DBX_FILTER_S ELECT	DEEMPHASIS_ FILTER_SELEC T	0	DC_DEMOD_P OST_ON	DC_DEMOD_PR E_ON	DC_SCART_ON	
RO								

**Address:** 93h  
**Type:** RO  
**Reset:** 0011 0000

- [7:6] Reserved
- [5] Select the type of filter used in the DBX block:
  - 0: 1st order filter de-emphasis
  - 1: 2nd order filter de-emphasis
- [4] Select the type of filter used in the de-emphasis block
  - 0: 1st order filter de-emphasis
  - 1: 2nd order filter de-emphasis
- [3] Reserved
- [2] Control the DC removal placed on the demod path, AFTER the DBX block:
  - 0: DC removal OFF
  - 1: DC Removal ON
- [1] Control the DC removal placed on the demod path, BEFORE the DBX block:
  - 0: DC removal OFF
  - 1: DC Removal ON
- [0] Control the DC removal placed on the SCART path:
  - 0: DC removal OFF
  - 1: DC Removal ON

## 10.12 Audio preprocessing and selection

### PRESCALE\_DEMOD\_MONO Prescale for demod MONO

7	6	5	4	3	2	1	0
PRESCALE_DEMOD_SELECT_SAP		PRESCALE_DEMOD_MONO[6:0] (S)					
R/W							

**Address:** 94h  
**Type:** R/W  
**Reset:** 0000 0000

*Note:* The following register bit is controlled by Autostandard and is forced by default to read-only mode.

- [7] Select the prescale value to apply on channel 0 (mono/stereo):  
 0: Apply STEREO prescale (95h) to the demodulated signal. To be used in case of STEREO demodulation.  
 1: Apply MONO prescale (94h) on left channel and SAP prescale (96h) on right channel to the demodulated signal. To be used in case of MONO or SAP demodulation.
- [6:0] Set the prescale of the signal coming from the demodulator when MONO (channel 0):  
 110 1000: 12 dB  
 ...  
 000 0000: 0 dB  
 000 0001: 0.5 dB  
 ...  
 011 0000: 24 dB

### PRESCALE\_DEMOD\_STEREO Prescale for stereo demodulation

7	6	5	4	3	2	1	0
0	PRESCALE_DEMOD_STEREO[6:0] (S)						
R/W							

**Address:** 95h  
**Type:** R/W  
**Reset:** 0000 0000

- [7] Reserved
- [6:0] Sets the prescale value of the stereo signal coming from the demodulator (channels 0 and 1):  
 110 1000: -12 dB  
 ...  
 000 0000: 0 dB  
 000 0001: 0.5 dB  
 ...  
 011 0000: 24 dB

**PRESCALE\_DEMOD\_SAP      Prescale for SAP demodulation**

7	6	5	4	3	2	1	0
0	PRESCALE_DEMOD_SAP[6:0] (S)						
R/W							

**Address:**      96h  
**Type:**        R/W  
**Reset:**        0000 0000

[7] Reserved

[6:0] Set the prescale of the signal coming from the demodulator when SAP (channel 0):  
 110 1000: -12dB  
 ...  
 000 0000: 0dB  
 000 0001: 0.5dB  
 ...  
 011 0000: 24dB

**PRESCALE\_SCART      Prescale for SCART**

7	6	5	4	3	2	1	0
0	PRESCALE_SCART[6:0] (S)						
R/W							

**Address:**      97h  
**Type:**        R/W  
**Reset:**        0000 0000

[7] Reserved

[6:0] Set the prescale of the signal coming from the SCART ADC:  
 110 1000: -12dB  
 ...  
 000 0000: 0dB  
 000 0001: 0.5dB  
 ...  
 011 0000: 24dB

**PRESCALE\_I2S0      Prescale for I2S0**

7	6	5	4	3	2	1	0
0	PRESCALE_I2S0[6:0] (S)						
R/W							

**Address:**      98h  
**Type:**        R/W  
**Reset:**        0000 0000



[7] Reserved

[6:0] Set the prescale of the signal coming from the I<sup>2</sup>S0 (SRC input or I2S0 in multi-channel input mode):

110 1000: -12dB

...

000 0000: 0dB

000 0001: 0.5dB

...

011 0000: 24dB

## PRESCALE\_I2S1

### Prescale for I2S1

7	6	5	4	3	2	1	0
0	PRESCALE_I2S1[6:0] (S)						
R/W							

**Address:** 99h

**Type:** R/W

**Reset:** 0000 0000

[7] Reserved

[6:0] Set the prescale of the signal coming from the I2S1 (I2S1 in multi-channel input mode):

110 1000: -12dB

...

000 0000: 0dB

000 0001: 0.5dB

...

011 0000: 24dB

## PRESCALE\_I2S2

### Prescale for I2S2

7	6	5	4	3	2	1	0
0	PRESCALE_I2S2[6:0] (S)						
R/W							

**Address:** 9Ah

**Type:** R/W

**Reset:** 0000 0000

[7] Reserved

[6:0] Set the prescale of the signal coming from the I<sup>2</sup>S2 (delay input or I<sup>2</sup>S2 in multi-channel input mode):

110 1000: -12dB

...

000 0000: 0dB

000 0001: 0.5dB

...

011 0000: 24dB

**PEAK\_DETECTOR****Peak detector**

7	6	5	4	3	2	1	0
0	PEAK_L_R_RANGE[2:0]			PEAK_DET_INPUT[2:0]			PEAK_DETECT OR_ON
RO							

**Address:** 9Bh

**Type:** RO

**Reset:** 0000 0000

[7] Reserved

[6:4] Control the sensitivity of the “Left - Right” peak measurement (register 0x9E). The difference between Left and Right signal is sometimes very small (for example, in the case of mono input), so you can multiply the “Left - Right” peak measurement in order to add precision:

000: Left - Right

001: Left - Right) x 2

010: Left - Right) x 4

011: Left - Right) x 8

100: Left - Right) x 16

101: Left - Right) x 32

110: Left - Right) x 64

111: Left - Right) x 128

[3:1] Select the input on which the peak detector makes the measurement:

000: Demod signal

001: I2S0 signal

010: I2S1 signal

011: I2S2 signal

100: SCART signal

101: Reserved

110: Reserved

111: Reserved

[0] Control the peak detector:

0: Peak detector OFF

1: Peak detector ON

**PEAK\_L** **Peak detector left channel**

7	6	5	4	3	2	1	0
OVERLOAD_L		PEAK_L[6:0] (S)					
R/W							

**Address:** 9Ch  
**Type:** R/W  
**Reset:** 0(000 0000)

[7] This bit is set to 1 by the DSP when the left peak detector reaches its maximum value (0x7F). It can be reset to 0.

[6:0] Displays the absolute peak level of the left channel of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB).

- 000 0000: <-36dBFS
- ...
- 000 0001: -36dBFS
- ...
- 000 0011: -30dBFS
- ...
- 000 0111: -24dBFS
- ...
- 000 1111: -18dBFS
- ...
- 001 1111: -12dBFS
- ...
- 111 1111: 0dBFS

**PEAK\_R** **Peak detector right channel**

7	6	5	4	3	2	1	0
OVERLOAD_R		PEAK_R[6:0] (S)					
R/W							

**Address:** 9Dh  
**Type:** R/W  
**Reset:** 0(000 0000)

[7] This bit is set to 1 by the DSP when the right peak detector reaches its maximum value (0x7F). It can be reset to 0.

[6:0] Displays the absolute peak level of the right channel of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB).

000 0000: <-36dBFS  
 ...  
 000 0001: 36dBFS  
 ...  
 000 0011: -30dBFS  
 ...  
 000 0111: -24dBFS  
 ...  
 000 1111: -18dBFS  
 ...  
 001 1111: -12dBFS  
 ...  
 011 1111: -6dBFS  
 ...  
 111 1111: 0dBFS

**PEAK\_L\_R****Peak detector left minus right channel**

7	6	5	4	3	2	1	0
OVERLOAD_L_ R	PEAK_L_R[6:0] (S)						
R/W							

**Address:** 9Eh  
**Type:** R/W  
**Reset:** 0(000 0000)

[7] This bit is set to 1 by the DSP when the “Left-Right” peak detector reaches its maximum value (0x7F). It can be reset to 0.

[6:0] Displays the difference between L and R (L - R) channels for the audio source selected:

000 0000: -36dBFS  
 ...  
 000 0001: -36dBFS  
 ...  
 000 0011: -30dBFS  
 ...  
 000 0111: -24dBFS  
 ...  
 000 1111: -18dBFS  
 ...  
 001 1111: -12dBFS  
 ...  
 011 1111: -6dBFS  
 ...  
 111 1111: 0dBFS

## 10.13 Matrixing

### DOWNMIX\_MODE DownMix mode configuration

7	6	5	4	3	2	1	0
LT_RT_OUT_M ODE	MIX_OUT_MODE[2:0]			LFE_IN	MIX_IN_MODE[2:0]		
R/W							

**Address:** 9Fh

**Type:** R/W

**Reset:** 0111 1111

[7] Defines to format for downmix Lt/Rt output:

- 0: Lt/Rt Pro Logic compatible mode
- 1: L/R stereo mode

[6:4] Selects output channels configuration for downmix:  
see [Table 9](#).

[3] To select if LFE is inputted on I2S1 in multi-channel input mode:

- 0: No LFE on I2S1 input
- 1: LFE on I2S1 input

[2:0] Selects input channels configuration for downmix:  
see [Table 8](#).

**Table 8. DownMix IN modes**

Parameter coding (bin)	Parameter field label	Function
000	MODE11	Not used
001	MODE10	1/0 (C)
010	MODE20	2/0 (L,R)
011	MODE30	3/0 (L,R,C)
100	MODE21	2/1 (L,R,S)
101	MODE31	3/1 (L,R,C,S)
110	MODE22	2/2 (L,R,Ls,Rs)
111	MODE32	3/2 (L,R,C,Ls,Rs)

**Table 9. DownMix OUT modes**

Parameter coding (bin)	Parameter field label	Function
000	MODE20t	2/0 Dolby Surround (L,R)
001	MODE10	1/0 (C)
010	MODE20	2/0 (L,R)
011	MODE30	3/0 (L,R,C)
100	MODE21	2/1 (L,R,S)

Table 9. DownMix OUT modes (continued)

Parameter coding (bin)	Parameter field label	Function
101	MODE31	3/1 (L,R,C,S)
110	MODE22	2/2 (L,R,Ls,Rs)
111	MODE32	3/2 (L,R,C,Ls,Rs)

**DOWNMIX\_DUAL\_MODE** Downmix dual mode configuration

7	6	5	4	3	2	1	0
0	0	0	DUAL_ON	LS_DUAL_SELECT[1:0]	LTRT_DUAL_SELECT[1:0]		
R/W							

**Address:** A0h**Type:** R/W**Reset:** 0000 0000

[7:5] Reserved

[4] Selects dual mode for DownMix bloc in case of dual language (in dual mode, Input and output mode are forced to 2\_0):

0: Standard DownMix  
1: DownMix in dual mode

[3:2] Selects the language for LS output in case of dual mode:

00: Stereo  
01: Left mono  
10: Right mono  
11: Left + Right mix

[1:0] Selects the language for LtRt output in case of dual mode:

00: Stereo  
01: Left mono  
10: Right mono  
11: Left + Right mix

**DOWNMIX\_CONFIG** Downmix configuration

7	6	5	4	3	2	1	0
0	0	SRND_FACTOR[1:0]	CENTER_FACTOR[1:0]	LR_UPMIX	NORMALIZE		
R/W							

**Address:** A1h**Type:** R/W**Reset:** 0000 0001

[7:6] Reserved

- [5:4] 00: -3 dB  
 01: -4.5 dB  
 10: -6 dB  
 10: -6 dB
- [3:2] 00: -3 dB  
 01: -4.5 dB  
 10: -6 dB  
 11: -4.5 dB
- [1] 0: Up mixing disabled  
 1: Up mixing enabled (DTS specified)
- [0] 0: Normalization disabled  
 1: Normalization enabled

**AUDIO\_MATRIX1****Audio matrix 1 configuration**

7	6	5	4	3	2	1	0
0	0	HP_OUT			LS_OUT		
R/W							

**Address:** A2h  
**Type:** R/W  
**Reset:** 0010 0010

- [7:6] Reserved
- [5:3] Select the source to output on HP. See [Table 10](#).
- [2:0] Select the source to output on LS. See [Table 10](#).

**AUDIO\_MATRIX2****Audio matrix 2 configuration**

7	6	5	4	3	2	1	0
0	0	SCART2_OUT			SCART1_OUT		
R/W							

**Address:** A3h  
**Type:** R/W  
**Reset:** 0001 0010

- [7:6] Reserved
- [5:3] Select the source to output on SCART2:  
 see [Table 10](#).
- [2:0] Select the source to output on SCART1:  
 see [Table 10](#).

**AUDIO\_MATRIX3****Audio matrix 3 configuration**

7	6	5	4	3	2	1	0
0	0	SPDIF_OUT			DELAY_OUT		
R/W							

**Address:** A4h**Type:** R/W**Reset:** 0001 0010

[7:6] Reserved

[5:3] Select the source to output on SPDIF. See [Table 10](#).[2:0] Select the source to output on DELAY. See [Table 10](#).**Table 10. AudioMatrix input sources**

Parameter coding (bin)	Parameter field label	Function
000	MUTE	Mute output
001	DELAY	Delay input
010	DEMODO	BTSC demod input
011	LtRt	Downmix LtRt Input
100	I <sup>2</sup> S	I2S input
101	SCART	SCART input
110	-	Reserved
111	-	Reserved

**CHANNEL\_MATRIX\_LS****Channel matrix configuration for LS**

7	6	5	4	3	2	1	0
AUTOSTD_CTR L_LS	AUTOSTD_CTR L_SPDIF	0	0	0	CM_MATRIX_LS[2:0]		
R/W							

**Address:** A5h**Type:** R/W**Reset:** 0000 0000

[7] If this bit is activated, Autostandard algorithm automatically selects the appropriate matrixing (Bits[2:0]) for LS output channels depending on the detected standard (see [Table 12](#)).

0: Manual matrix selection

1: Automatic matrix selection if Autostandard is ON

Note: Automatic matrix selection must be used only when the DEMOD signal is directed to the matrix.



[6] If this bit is activated, Autostandard algorithm will select automatically the appropriate matrixing (bits[2:0]) for SPDIF output channels depending on the detected standard (see [Table 12](#)).

0: Manual matrix selection

1: Automatic matrix selection if Autostandard is ON

Note: Automatic matrix selection must be used only when the DEMOD signal is directed to the matrix.

[5:3] Reserved

[2:0] Select the matrixing for the LS channels. See [Table 11](#).

## CHANNEL\_MATRIX\_HP Channel matrix configuration for HP

7	6	5	4	3	2	1	0
AUTOSTD_CTRL_HP	CM_SOURCE_HP[1:0]		CM_POSITION_HP[1:0]			CM_MATRIX_HP[2:0]	
R/W							

**Address:** A6h

**Type:** R/W

**Reset:** 0000 0000

[7] If this bit is activated, Autostandard algorithm will select automatically the appropriate matrixing (bits[2:0]) for HP output channels depending on the detected standard (see [Table 12](#)).

0: Manual matrix selection

1: Automatic matrix selection if Autostandard is ON Note: Automatic matrix selection must be used only when the DEMOD signal is directed to the Matrix.

[6:5] Select the source to copy on HP channel. See [Table 13](#).

[4:3] Select the position for the HP matrix. See [Figure 4](#)

00 = POSITION 0

01 = POSITION 1

10 = POSITION 2

11 = POSITION 3

[2:0] Select the matrixing for the HP channels. See [Table 11](#).

## CHANNEL\_MATRIX\_SCART Channel matrix configuration for SCART

7	6	5	4	3	2	1	0
AUTOSTD_CTRL_SCART	CM_SOURCE_SCART[1:0]		CM_POSITION_SCART[1:0]			CM_MATRIX_SCART[2:0]	
R/W							

**Address:** A7h

**Type:** R/W

**Reset:** 0000 0000

- [7] If this bit is activated, the Autostandard algorithm automatically selects the appropriate matrixing (Bits[2:0]) for SCART output channels depending on the detected standard (see [Table 12](#)).  
 0: Manual matrix selection  
 1: Automatic matrix selection must be used only when DEMOD signal is directed to the matrix.
- [6:5] Select the source to copy on SCART channel. See [Table 13](#).
- [4:3] Select the position for the SCART matrix. See [Figure 4](#)  
 00 = POSITION 0  
 01 = POSITION 1  
 10 = POSITION 2  
 11 = POSITION 3
- [2:0] Select the matrixing for the SCART channels. See [Table 11](#).

**CHANNEL\_MATRIX\_SCARTaux      Channel matrix configuration for SCARTaux**

7	6	5	4	3	2	1	0
AUTOSTD_CTR L_SCARTaux	CM_SOURCE_SCARTaux[1:0]		CM_POSITION_SCARTaux[1:0]		CM_MATRIX_SCARTaux[2:0]		
R/W							

**Address:**        A8h  
**Type:**            R/W  
**Reset:**            0000 0000

- [7] If this bit is activated, the Autostandard algorithm automatically selects the appropriate matrixing (Bits[2:0]) for SCARTaux output channels depending on the detected standard (see [Table 12](#)).  
 0: Manual matrix selection  
 1: Automatic matrix selection if Autostandard is ON  
  
 Note: Automatic matrix selection must be used only when the DEMOD signal is directed to the matrix.
- [6:5] Select the source to copy on SCARTaux channel. See [Table 13](#).
- [4:3] Select the position for the SCARTaux matrix. See [Figure 4](#).  
 00 = POSITION 0  
 01 = POSITION 1  
 10 = POSITION 2  
 11 = POSITION 3
- [2:0] Select the matrixing for the SCARTaux channels. See [Table 11](#).

## CHANNEL\_MATRIX\_SPDIF Channel matrix configuration for SPDIF

7	6	5	4	3	2	1	0
CM_SOURCE_SPDIF[2:0]			CM_POSITION_SPDIF[1:0]		CM_MATRIX_SPDIF[2:0]		
R/W							

**Address:** A9h

**Type:** R/W

**Reset:** 0000 0000

[7:5] Select the source to copy on SPDIF channel. See [Table 13](#).

[4:3] Select the position for the SPDIF matrix. See [Figure 4](#).

00 = POSITION 0

01 = POSITION 1

10 = POSITION 2

11 = POSITION 3

[2:0] Select the matrixing for the SPDIF channels. See [Table 11](#).

**Table 11. Channel matrix modes**

Parameter coding (Bin)	Parameter field label	Function
000	BYPASS	Bypass stereo signal
001	LEFT ONLY	Copy left signal on both channels
010	RIGHT ONLY	Copy right signal on both channels
011	LEFT + RIGHT MIX	Copy (left + right)/2 on both channels
100	SWAP	Swap channel (left = right, right = left)
101	-	Reserved
110	-	Reserved
111	-	Reserved

**Table 12. Automatic channel matrix modes**

Standard detected by Autostandard	MONO_SAP_CTRL_MATRIX reg 0x8A, bit[6] value = 0		MONO_SAP_CTRL_MATRIX reg 0x8A, bit[6] value = 1	
	Left output	Right output	Left output	Right output
Mono	Mono signal	Mono signal	Mono signal	Mono signal
Stereo	Left signal	Right signal	Left signal	Right signal
SAP	SAP signal	SAP signal	Mono signal	SAP signal

**Table 13. Channel matrix source selection**

Parameter coding (Bin)	Parameter field label	Function
000	BYPASS	Bypass stereo signal coming from audio matrix
001	LS channels	Copy signal from LS channels

**Table 13. Channel matrix source selection (continued)**

Parameter coding (Bin)	Parameter field label	Function
010	HP channels	Copy signal from HP channels
011	C/Sub channels	Copy signal from C/Sub channels (ONLY AVAILABLE ON SPDIF CHANNEL MATRIX)
100	Ls/Rs channels	Copy signal from Ls/Rs channels (ONLY AVAILABLE ON SPDIF CHANNEL MATRIX)
101	-	Reserved
110	-	Reserved
111	-	Reserved

**DEMODOC\_LEVEL DC level on demod FM mono input**

7	6	5	4	3	2	1	0
DEMODOC_LEVEL[7:0] (S)							
RO							

**Address:** AAh  
**Type:** RO  
**Reset:** 0000 0000

[7:0] Displays the amount of the DC component in the signal coming from the FM mono channel. This DC level can be used to implement carrier offset compensation.

**10.14 Audio processing**

**AV\_DELAY\_CONFIG AV delay configuration**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DOLBY_DELAY_ON	AV_DELAY_ON
R/W							

**Address:** ADh  
**Type:** R/W  
**Reset:** 0000 0000

[7:2] Reserved  
 [1] Must be set to 1 to use the center, left Srnd and right Srnd delays for Pro Logic decoder multi-channel output.  
 Note: This value must be updated when AV\_DELAY\_ON = 0.  
 [0] 0: No AV delay  
 1: AV delay is active

Note: See [Table 14](#) for Audio/Video delay configuration.

### AV\_DELAY\_TIME\_LS AV delay LS configuration

7	6	5	4	3	2	1	0
AV_DELAY_TIME_LS[7:0]							
R/W							

**Address:** AEh  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] Set the delay time for LS channel.  
 0000 0000: 0 ms  
 0000 0001: 0.66 ms  
 ...  
 1011 0001: 116.82 ms (max)  
 Note: This value must be updated when AV\_DELAY\_ON = 0.

Note: See [Table 14](#) for Audio/Video delay configuration.

### AV\_DELAY\_TIME\_HP AV delay HP configuration

7	6	5	4	3	2	1	0
AV_DELAY_TIME_HP[7:0]							
R/W							

**Address:** AFh  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] Set the delay time for HP channel.  
 0000 0000: 0 ms  
 0000 0001: 0.66 ms  
 ...  
 1011 0001: 116.82 ms (max)  
 Note: This value must be updated when AV\_DELAY\_ON = 0.

Note: 1 See [Table 14](#) for audio/video delay configuration.  
 2 The sum of AV\_DELAY\_TIME\_LS and AV\_DELAY\_TIME\_HP must not exceed:

- 177 (116.82 ms) if DOLBY\_DELAY\_ON = 0
- 100 (66.66 ms) if DOLBY\_DELAY\_ON = 1

Table 14. Audio/Video delay (lip sync) configuration

Input source	Register values										Output				
	AV_DELAY_CO_NFIG(ADh)		AV_DELAY_TIME_LS(AEh)		AV_DELAY_TIME_HP(AFh)		PCM_SRND_DELAY(B5h)		PCM_CENTER_DELAY(B6h)		LS_L	LS_R	HP_R/L	Scart_L	Scart_R
	DOLBY_DELAY_ON	AV_DELAY_ON	AV_DELAY_TIME_LS[7:0]		AV_DELAY_TIME_HP[7:0]		DOLBY_DELAY_SRND[4:0]		DOLBY_DELAY_CENTER[3:0]		Source SIF-SCART I2S	Source SIF-SCART I2S	Source SIF-SCART I2S	Source SIF-SCART I2S	Source SIF-SCART I2S
SIF or SCART or I2S (48kHz)	0	1	00000000	0	00000000	0	xxx00000	0	xxx0000	0	0	0	0	0	0
	0	1	10110001	117	00000000	0	xxx11110	30	xxx1010	10	117	117	0	0	0
	0	1	00000000	0	10110001	117	xxx00000	0	xxx0000	0	0	0	117	0	0
	0	1	01011000	58	01011000	58	xxx00000	0	xxx0000	0	58	58	58	0	0
	1	1	10110001	117	00000000	0	xxx00000	0	xxx0000	0	66	66	0	0	0
	1	1	00000000	0	10110001	117	xxx11110	30	xxx0000	10	0	0	66	0	0
	1	1	01011000	58	01011000	58	xxx00000	0	xxx0000	0	58	58	8	0	0
	1	1	01011000	58	01011000	58	xxx11110	30	xxx0000	0	58	58	8	0	0
	1	1	01011000	58	01011000	58	xxx00000	0	xxx1010	10	58	58	8	0	0
1	1	01011000	58	01011000	58	xxx11110	30	xxx1010	10	58	58	8	0	0	

### PRO\_LOGIC2\_CONTROL      Dolby Pro Logic 2 mode configuration

7	6	5	4	3	2	1	0
PL2_LFE	PL2_OUTPUT_DOWNMIX[2:0]			PL2_MODES[2:0]			PL2_ACTIVE
R/W							

**Address:** B0h

**Type:** R/W

**Reset:** 0000 0000

[7] 0: Reset the LFE channel  
1: Bypass the LFE channel

[6:4] 000: Not applicable  
001: Not applicable  
010: Not applicable  
011: 3/0 output mode (L,R,C)  
100: 2/1 output mode (L,R,Ls - phantom)  
101: 3/1 output mode (L,R,C,Ls)  
110: 2/2 output mode (L,R,Ls,Rs - phantom)  
111: 3/2 output mode (L,R,C,Ls,Rs)

[3:1] 000: Pro Logic 1 emulation  
001: Virtual  
010: Music  
011: Movie (standard)  
100: Matrix  
101: Custom  
110: Not applicable  
111: Not applicable

[0] 0: Dolby Pro Logic 2 is not active  
1: Dolby Pro Logic 2 is active

### PRO\_LOGIC2\_CONFIG      Dolby Pro Logic 2 configuration

7	6	5	4	3	2	1	0
PL2_LFE0	0	0	PL2_SRND_FILTER[1:0]	PL2_RS_POLARITY	PL2_PANORAMA	PL2_AUTOBALANCE	
R/W							

**Address:**      B1h  
**Type:**         R/W  
**Reset:**        0000 0000

[7] 0: Reset the LFE channel  
 1: Bypass the LFE channel

[6:5] Reserved

[4:3] 00: Off  
 01: Shelf  
 10: 7-kHz LP  
 11: Not applicable

[2] 0: Rs polarity normal  
 1: Rs polarity inverted

[1] 0: Panorama OFF  
 1: Panorama ON

[0] 0: Autobalance OFF  
 1: Autobalance ON

### PRO\_LOGIC2\_DIMENSION      Dolby Pro Logic 2 dimension

7	6	5	4	3	2	1	0
0	PL2_C_WIDTH			0	PL2_DIMENSION		
R/W							

**Address:**      B2h  
**Type:**         R/W  
**Reset:**        0000 0000

[7] Reserved

[6:5] Pro Logic 2 center width:  
 000: 0, no spread  
 001: 20.8  
 010: 28  
 011: 36  
 100: 54  
 101: 62  
 110: 69.2  
 111: 90, phantom

[3] Reserved

[2:0] Pro Logic 2 dimension:  
 000: -3, most surround  
 001: -2  
 010: -1  
 011: 0, neutral  
 100: 1  
 101: 2  
 110: 3, most center  
 111: Not used

**PRO\_LOGIC2\_LEVEL****Dolby Pro Logic 2 input level**

7	6	5	4	3	2	1	0
PL2_LEVEL							
R/W							

**Address:** B3h  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] Input gain attenuation:  
 0000 0000: 0 dB  
 0000 0001: -0.5 dB  
 ...  
 1111 1111: -127.5 dB

**NOISE\_GENERATOR****Pink noise generator**

7	6	5	4	3	2	1	0
10_DB_ATTENUATE	SRIGHT_NOISE	SLEFT_NOISE	SUB_NOISE	CENTER_NOISE	RIGHT_NOISE	LEFT_NOISE	NOISE_ON
R/W							

**Address:** b4H  
**Type:** R/W  
**Reset:** 0000 0000

[7] 0: Noise is output with full range  
 1: Noise is output with a 10dB attenuation  
 [6] 1: Generates noise on LS right surround output  
 [5] 1: Generates noise on LS left surround output  
 [4] 1: Generates noise on LS subwoofer output  
 [3] 1: Generates noise on LS center output  
 [2] 1: Generates noise on LS right output  
 [1] 1: Generates noise on LS left output



[0] 0: Noise generation not active  
1: Noise generation active

### PCM\_SRND\_DELAY                      Dolby surround delay

7	6	5	4	3	2	1	0
0	0	0	DOLBY_DELAY_SRND[4:0]				
R/W							

**Address:**        B5  
**Type:**            R/W  
**Reset:**          0000 0000

[7:5] Reserved  
[4:0] Surround channel delay:  
Range: 0 to 30 (in ms)

*Note:*    1    See [Table 14](#) for Audio/Video delay configuration.  
          2    To use this feature, set the DOLBY\_DELAY\_ON bit to 1 in register AV\_DELAY\_CONFIG (ADh).

### PCM\_CENTER\_DELAY                    Dolby center delay

7	6	5	4	3	2	1	0
0	0	0	0	DOLBY_DELAY_CENTER[3:0]			
R/W							

**Address:**        B6h  
**Type:**            R/W  
**Reset:**          0000 0000

[7:4] Reserved  
[3:0] Center channel delay:  
Range: 0 to 10 (in ms)

*Note:*    1    See [Table 14](#) for audio/video delay configuration.  
          2    To use this feature, set the DOLBY\_DELAY\_ON bit to 1 in register AV\_DELAY\_CONFIG (ADh).

**TRUSRND\_CONTROL      SRS TruSurround control**

7	6	5	4	3	2	1	0
DIALOG_CLARITY_ON	HEADPHONE_ON	TRUSRND_INPUT_MODE[3:0]				TRUSRND_BYPASS	TRUSRND_ON
R/W							

**Address:**      B7h  
**Type:**        R/W  
**Reset:**        0000 0000

- [7] Dialog clarity:  
0: Dialog clarity OFF  
1: Dialog clarity ON  
Note: The dialog clarity level is set in register 0xB8: TRUSRND\_DC\_ELEVATION
- [6] Process the sound especially for headphones. This option must be selected only if the TruSurround sound is redirected to the headphone output using the HP channel matrix.  
0: Standard mode for loudspeaker output  
1: Headphone mode for headphone output only
- [5:2] 0000: Mono on center channel  
0001: Mono on left channel  
0010: L/R stereo (SRS mode)  
0011: L/R/S (SRS mode, Pro Logic 1 process)  
0100: L/R/Ls/Rs (SRS mode)  
0110: L/R/C/S (TruSurround mode, Pro Logic 1 process)  
0111: L/R/C/Ls/Rs (TruSurround mode)  
1000: Lt/Rt (TruSurround mode)  
1001: L/R/C/Ls/Rs (SRS mode, BS digital broadcast)  
1010: L/R/C/Ls/Rs (TruSurround, Pro Logic 2 Music mode)
- [1] Bypass the TruSurround effect by applying a simple downmix on input channels.  
0: TruSurround mode  
1: Bypass mode (downmix to 2 channels)
- [0] 0: TruSurround OFF  
1: TruSurround ON

**Note:**      *Using TruSurround XT:*

- Implementation of TruSurround XT is done by setting the TRUSRND\_ON bit to 1.
- TruSurround XT mode must be selected by TRUSRND\_INPUT\_MODE[3:0] bits.
- Activation or non-activation of TruSurround XT must be done by using the TRUSRND\_MODE bit.

**TRUSRND\_DC\_ELEVATION**      **Set dialog clarity level**

7	6	5	4	3	2	1	0
TRUSRND_DC_ELEVATION[7:0]							
R/W							

**Address:**      B8h  
**Type:**          R/W  
**Reset:**        0000 1100I

[7:0] Dialog clarity elevation:  
0000 0000: 0 dB  
0000 0001: -0.5 dB  
...  
1111 1111: -127.5 dB

**TRUSRND\_INPUT\_GAIN**      **Input gain for TruSurround**

7	6	5	4	3	2	1	0
TRUSRND_INPUT_GAIN[7:0]							
R/W							

**Address:**      B9h  
**Type:**          R/W  
**Reset:**        0000 0000

[7:0] Input gain attenuation:  
0000 0000: 0 dB  
0000 0001: -0.5 dB  
...  
1111 1111: -127.5 dB

**TRUBASS\_LS\_CONTROL**      **LS configuration for SRS TruBass**

7	6	5	4	3	2	1	0
0	0	0	0	TRUBASS_LS_SIZE[2:0]		TRUBASS_LS_ON	
R/W							

**Address:**      BAh  
**Type:**          R/W  
**Reset:**        0000 0110

[7:4] Reserved

- [3:1] 000: LF response at 40 Hz
- 001: LF response at 60 Hz
- 010: LF response at 100 Hz
- 011: LF response at 150 Hz
- 100: LF response at 200 Hz
- 101: LF response at 250 Hz
- 110: LF response at 300 Hz
- 111: LF response at 400 Hz
- [0] 0: LS TruBass OFF
- 1: LS TruBass ON

**TRUBASS\_LS\_LEVEL            SRS TruBass LS level**

	7	6	5	4	3	2	1	0
TRUBASS_LS_LEVEL[7:0]								
R/W								

**Address:**        BBh  
**Type:**            R/W  
**Reset:**          0000 1001

- [7:0] Defines the amount of SRS TruBass effect for LS outputs:
- 0000 0000: 0 dB
- 0000 0001: -0.5 dB
- ...
- 1111 1111: -127.5 dB

**TRUBASS\_HP\_CONTROL        SRS TruBass HP configuration**

	7	6	5	4	3	2	1	0
SRS_TSXT_GAIN_ON	0	0	0	TRUBASS_HP_SIZE[2:0]			TRUBASS_HP_ON	

**Address:**        BCh  
**Type:**            R/W  
**Reset:**          0000 0110

- [7] Apply the TruSurround gain (register 0xB9) to the TruBass input block. This gain must be applied only if the TruSurround signal has been redirected to the TruBass HP via the HP channel matrix.
- 0: SXT input gain is not applied
- 1: TSXT input gain is applied. (this configuration must be used if the LS signal processed with TSXT is redirected to the HP channel)
- [6:4] Reserved

[3:10] 000: LF response at 40 Hz  
 001: LF response at 60 Hz  
 010: LF response at 100 Hz  
 011: LF response at 150 Hz  
 100: LF response at 200 Hz  
 101: LF response at 250 Hz  
 110: LF response at 300 Hz  
 111: LF response at 400 Hz

[0] 0: HP TruBass OFF  
 1: HP TruBass ON

**TRUBASS\_HP\_LEVEL****SRS TruBass HP level**

7	6	5	4	3	2	1	0
TRUBASS_HP_LEVEL[7:0]							
R/W							

**Address:** BDh  
**Type:** R/W  
**Reset:** 0000 1001

[7:0] Defines the amount of SRS TruBass effect for HP outputs:  
 0000 0000: 0 dB  
 0000 0001: -0.5 dB  
 ...  
 1111 1111: -127.5 dB

**SVC\_LS\_CONTROL****Smart volume control for LS**

**Address:** BEh  
**Type:** R/W  
**Reset:** 0000 0010

7	6	5	4	3	2	1	0
0	0	0	0	SVC_LS_INPUT[1:0]	SVC_LS_AMP	SVC_LS_ON	
R/W							

[7:4] Reserved  
 [3:2] Select input for peak detection in multi-channel mode:  
 00: Left/Right  
 01: Center  
 10: Left/Right/Center  
 11: Not used  
 [1] 0: 0 dB amplification in auto-mode  
 1: +6 dB amplification in auto-mode  
 [0] 0: Manual mode (simple prescaler)  
 1: Automatic mode

## SVC\_LS\_TIME\_TH

## Smart volume control parameters for LS

7	6	5	4	3	2	1	0
SVC_LS_TIME[2:0]			SVC_LS_THRESHOLD[4:0] (S)				
R/W							

**Address:** BFh

**Type:** R/W

**Reset:** 1001 1000

[7:6] Time constant for amplification (6-dB gain step) in automatic mode:

000: 30 ms

001: 200 ms

010: 500 ms

011: 1 s

100: 16 s

101: 32 s

110: 64 s

111: 128 s

[4:0] (S) See [Table 15](#) and [Table 16](#).

**Table 15. Gain (threshold field) values in manual mode**

Manual mode	Gain (dB)	Manual mode	Gain (dB0)
00101	+15.5	11101	-8.5
00100	+12	11100	-12
00011	+9.5	11011	-14.5
00010	+6	11010	-18
00001	+3.5	11001	-20.5
00000	0	11000	-24
11111	-2.5	10111	-26.5
11110	-6	10110	-30

**Table 16. Threshold values in automatic mode**

Automatic mode	Threshold (dB)	Automatic mode	Threshold (dB)
11111	-2.5	11010	-18
11110	-6	11001	-20.5
11101	-8.5	11000	-24
11100	-12	10111	-26.5
11011	-14.5	10110	-30

### SVC\_LS\_GAIN                      Make-up gain for SVC LS

7	6	5	4	3	2	1	0
0	0	SVC_LS_GAIN[5:0]					
R/W							

**Address:**        C0h  
**Type:**            R/W  
**Reset:**           0000 0000

- [7:6] Reserved  
 [5:0] Set "make-up" gain applied at SVC LS output:  
 000000: +0 dB  
 000001: + 0.5 dB  
 ...  
 101110: +23 dB  
 101111: +23.5 dB  
 110000: +24 dB

### SVC\_HP\_CONTROL                  Smart volume control for HP

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SVC_HP_AMP	SVC_HP_ON
R/W							

**Address:**        C1h  
**Type:**            R/W  
**Reset:**           0000 0010

- [7:2] Reserved  
 [1] 0: 0 dB amplification in auto-mode  
      1: +6 dB amplification in auto-mode  
 [0] 0: Manual mode (simple prescaler)  
      1: Automatic mode

### SVC\_HP\_TIME\_TH                  Smart volume control parameters for HP

7	6	5	4	3	2	1	0
SVC_HP_TIME[2:0]			SVC_HP_THRESHOLD[4:0] (S)				
R/W							

**Address:**        C2h  
**Type:**            R/W  
**Reset:**           1001 1000

[7:5] Time constant for amplification (6-dB gain step) in automatic mode:

000: 30 ms  
 001: 200 ms  
 010: 500 ms  
 011: 1 s  
 100: 6 s  
 101: 32 s  
 110: 64 s  
 111: 128 s

[4:0] (S) See [Table 15](#) and [Table 16](#)

**SVC\_HP\_GAIN****Make-up gain for SVC HP**

7	6	5	4	3	2	1	0
0	0	SVC_HP_GAIN[5:0]					
R/W							

**Address:** C3h

**Type:** R/W

**Reset:** 0000 0000

[7:6] Reserved

[5:0] Set “make-up” gain applied at SVC HP output:

000000: +0 dB  
 000001: 0.5 dB  
 ...  
 101110: +23 dB  
 101111: +23.5 dB  
 110000: +24 dB

**WIDESRND\_CONTROL****ST WideSurround sound control**

7	6	5	4	3	2	1	0
0	0	0	0	0	WIDESRND_ST EREO	WIDESRND_MO DE	WIDESRND_ON
R/W							

**Address:** C4h

**Type:** R/W

**Reset:** 0000 0100

[7:3] Reserved

[2] ST WideSurround sound stereo mode:

0: ST WideSurround sound in mono mode (default)  
 1: ST WideSurround Sound in stereo mode



[1] ST WideSurround sound stereo mode:

0: Movie mode

1: Music mode

[0] ST WideSurround sound enable:

0: ST WideSurround sound is disabled

1: ST WideSurround Sound is enabled

## WIDESRND\_FREQ ST WideSurround sound frequency

7	6	5	4	3	2	1	0
0	0	WIDESRND_BASS[1:0]	WIDESRND_MEDIUM[1:0]	WIDESRND_TREBLE[1:0]			
R/W							

**Address:** C5h

**Type:** R/W

**Reset:** 0001 0101

[7:6] Reserved

[5:4] Defines the bass frequency effect for ST WideSurround sound. Programmable values are listed in [Table 17](#).

[3:2] Defines the medium frequency effect for ST WideSurround sound in movie or mono mode (no effect in music mode). Programmable values are listed in [Table 17](#).

[1:0] Defines the treble frequency effect for ST WideSurround sound in movie or mono mode (no effect in music mode). Programmable values are listed in [Table 17](#).

**Table 17. Phase shifter center frequencies**

	Phase shifter center frequency		
	BASS_FREQ[1:0]	MEDIUM_FREQ[1:0]	TREBLE_FREQ[1:0]
00	40 Hz	202 Hz	2 kHz
01 (default)	90 Hz	416 Hz	4 kHz
10	120 Hz	500 Hz	5 kHz
11	160 Hz	588 Hz	6 kHz

## WIDESRND\_LEVEL ST WideSurround sound gain

7	6	5	4	3	2	1	0
WIDESRND_GAIN[7:0]							
R/W							

**Address:** C6h

**Type:** R/W

**Reset:** 1000 0000

[7:0] Defines the ST WideSurround sound component gain in linear scale:

	<u>Level (%)</u>
1000 0000 (default)	100%
0111 1111	99.2%
0111 1110	98.4%
0111 1101	97.6%
0000 0100	3.1%
0000 0011	2.3%
0000 0010	1.6%
0000 0001	0.8%
0000 0000	0%

## OMNISURROUND\_CONTROL      ST OmniSurround configuration

7	6	5	4	3	2	1	0
ST_VOICE[1:0]	SRND_PHASE_I NV	OMNISRND_INPUT_MODE[3:0]				OMNISRND_ON	
R/W							

**Address:**      C7h

**Type:**          R/W

**Reset:**          0000 1100

[7:6] 00: OFF

01: Low

10: Mid

11: High

[5] Invert right surround phase in 2\_2 or 3\_2 input mode:

0: Right Surround phase not inverted

1: Right Surround phase inverted

[4:1] 0000: Mono on center channel

0001: Mono on left channel

0010: L/R stereo

0011: L/R/S

0100: L/R/Ls/Rs

0101: L/R/C

0110: L/R/C/S

0111: L/R/C/Ls/Rs

1000: Lt/Rt (passive matrix)

[0] 0: OmniSurround OFF

1: OmniSurround ON

### DYNAMIC\_BASS\_LS      ST dynamic bass for LS

7	6	5	4	3	2	1	0
LS_BASS_LEVEL[4:0]					LS_BASS_FREQ[1:0]		LS_DYN_BASS_ON
R/W							

**Address:**      C8h  
**Type:**        R/W  
**Reset:**        0110 0010

[7:3] ST Dynamic Bass output gain:

00000: + 0dB

00001: +0.5dB

...

11101: +14.5dB

11110: +15dB

11111: +15.5dB

[2:1] 00: 100-Hz Cut-off frequency

01: 150-Hz Cut-off frequency

10: 200-Hz Cut-off frequency

11: 250-Hz Cut-off frequency

[0] 0: ST Dynamic Bass OFF

1: ST Dynamic Bass ON

### DYNAMIC\_BASS\_HP      ST Dynamic Bass for HP

7	6	5	4	3	2	1	0
HP_BASS_LEVEL[4:0]					HP_BASS_FREQ[1:0]		HP_DYN_BASS_ON
R/W							

**Address:**      C9h  
**Type:**        R/W  
**Reset:**        0110 0010

[7:3] ST Dynamic Bass output gain:

00000: +0dB

00001: +0.5dB

...

11101: +14.5dB

11110: +15dB

11111: +15.5dB

[2:1] 00: 100-Hz cut-off frequency

01: 150-Hz cut-off frequency

10: 200-Hz cut-off frequency

11: 250-Hz cut-off frequency

[0] 0: ST Dynamic Bass OFF

1: ST Dynamic Bass ON

**EQ\_BT\_CTRL****Loudspeakers equalizer control**

7	6	5	4	3	2	1	0
0	0	0	0	0	HP_BT_ON	LS_EQ_BT_SW	LS_EQ_ON
R/W							

**Address:** CCh**Type:** R/W**Reset:** 0000 0001

[7:3] Reserved

[2] Bass-treble for HP Enable

0: Bass-treble is disabled  
 1: Bass-treble is enabled

[1] 5- band equalizer or bass-treble for LS selection

0: 5-band equalizer is selected for loudspeakers.  
 1: Bass-treble is selected for loudspeakers.

[0] 5-band equalizer/bass-treble for LS enable

0: 5-band equalizer/bass-treble is disabled  
 1: 5-band equalizer/bass-treble is enabled

**LS\_EQ\_BANDX****Loudspeakers equalizer gain for bandX**

7	6	5	4	3	2	1	0
EQ_BANDX[7:0]							
R/W							

**Address:** CDh to D1h**Type:** R/W**Reset:** 0000 0000

[7:0] BandX gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB.

Band1: 100 Hz  
 Band2: 330 Hz  
 Band3: 1 kHz  
 Band4: 3.3 kHz  
 Band5: 10 kHz.

See [Table 18](#).

**Note:** *With positive equalizer settings, internal clipping can occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain*

**Table 18. Loudspeakers equalizer/bass-treble gain values (and headphone bass-treble gain values)**

Value	Gain G (dB)
00110000	+12
00101111	+11.75
00101110	+11.50
.....	.....
00000000 (default)	0
.....	.....
11010010	-11.50
11010001	-11.75
11010000	-12

**LS\_BASS\_GAIN****Loudspeakers bass gain**

7	6	5	4	3	2	1	0
LS_BASS[7:0]							
R/W							

**Address:** D2h  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] Gain tuning of loudspeakers bass frequency  
 Gain can be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB.  
 Programmable values are listed in [Table 18](#).

*Note:* With positive bass/treble settings, internal clipping can occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.

**LS\_TREBLE\_GAIN****Loudspeakers treble gain**

7	6	5	4	3	2	1	0
LS_TREBLE							
R/W							

**Address:** D3h  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] Gain tuning of loudspeakers treble frequency.  
Gain can be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB.  
Programmable values are listed in [Table 18](#).

**Note:** *With positive bass/treble settings, internal clipping can occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.*

## HP\_BASS\_GAIN                      Headphone bass gain

7	6	5	4	3	2	1	0
HP_BASS[7:0]							
R/W							

**Address:**        D4h  
**Type:**            R/W  
**Reset:**           0000 0000

[7:0] Gain tuning of headphone bass frequency.  
Gain can be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB.  
Programmable values are listed in [Table 18](#).

**Note:** *With positive bass/treble settings, internal clipping can occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.*

## HP\_TREBLE\_GAIN                    Headphone treble gain

7	6	5	4	3	2	1	0
HP_TREBLE							
R/W							

**Address:**        D5h  
**Type:**            R/W  
**Reset:**           0000 0000

[7:0] Gain tuning of headphone treble frequency.  
Gain can be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB.  
Programmable values are listed in [Table 18](#).

**Note:** *With positive bass/treble settings, internal clipping can occur even with an overall volume of less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass/treble bands to a value that, in conjunction with volume, would result in an overall positive gain.*

**OUTPUT\_BASS\_MNGT**      **Bass redirection**

7	6	5	4	3	2	1	0
BASS_MANAGE_ON	ST_LFE_ADD	DOLBY_PROLOGIC	SUB_ACTIVE	GAIN_SWITCH	OCFG_NUM[2:0]		
R/W							

**Address:**        D6h  
**Type:**            R/W  
**Reset:**           1000 0000

- [7] 0: Bass Management disabled  
     1: Bass Management enabled
- [6] Add the signal coming from the LFE input (MULTI\_I2S mode only) to the calculated subwoofer signal:  
     0: No LFE channel to add  
     1: Add LFE signal to the subwoofer computed signal
- [5] If Bass Management is used with the Dolby Pro Logic decoder, the surround channels must not be added to generate the subwoofer channel:  
     0: Standard configuration (Dolby Digital compliant), surround channels are used to generate the subwoofer channel.  
     1: Dolby Pro Logic configuration, surround channels are not used to generate the subwoofer channel.
- [4] In some configurations the subwoofer signal can be redirected to L/R channels if there is no Subwoofer output:.  
     0: No subwoofer output, the sub signal is added to L/R channels  
     1: Subwoofer signal is outputted on subwoofer output.
- [3] Gain switch available in some configurations:  
     0: Level adjustment ON  
     1: Level adjustment OFF
- [2:0] Select bass management configuration:  
     000: Output configuration 0  
     001: Output configuration 1  
     010: Output configuration 2  
     011: Output configuration 3  
     100: Output configuration 4 (simplified configuration)  
     101: Output configuration 5 (stereo full bandwidth speakers)  
     110: Output configuration 6 (stereo narrow bandwidth speakers)  
     111: Not used

**LS\_LOUDNESS****Loudness configuration for LS**

7	6	5	4	3	2	1	0
0	LS_LOUD_THRESHOLD[2:0]			LS_LOUD_GAIN_HR[2:0]			LS_LOUD_ON

**Address:** D7h**Type:** R/W**Reset:** 0000 0100

[7] Reserved

[6:4] Defines the volume threshold level at which the loudness effect is applied:

000: 0 dB  
 001: -6 dB  
 010: -12 dB  
 011: -18 dB  
 100: -24 dB  
 101: -32 dB  
 110: -36 dB  
 111: -42 dB

[3:1] Defines the amount of treble added by loudness effect:

000: 0 dB  
 001: 3 dB  
 010: 6 dB  
 011: 9 dB  
 100: 12 dB  
 101: 15 dB  
 110: 18 dB  
 111: Not used

[0] 0: Loudness is not active on LS output  
 1: Loudness is active on LS output

**HP\_LOUDNESS****Loudness configuration for HP**

7	6	5	4	3	2	1	0
0	HP_LOUD_THRESHOLD[2:0]			HP_LOUD_GAIN_HR[2:0]			HP_LOUD_ON

**Address:** D8h**Type:** R/W**Reset:** 0000 0100

[7] Reserved

[6:4] Defines the volume threshold level since which loudness effect is applied:

000: 0 dB  
 001: -6 dB  
 010: -12 dB  
 011: -18 dB  
 100: -24 dB  
 101: -32 dB  
 110: -36 dB  
 111: -42 dB



[3:1] Defines the amount of treble added by loudness effect:

000: 0 dB  
 001: 3 dB  
 010: 6 dB  
 011: 9 dB  
 100: 12 dB  
 101: 15 dB  
 110: 18 dB  
 111: Not used

[0] 0: Loudness is not active on HP output  
 1: Loudness is active on HP output

## VOLUME\_MODES

### Set the volume modes

7	6	5	4	3	2	1	0
ANTICLIP_HP_VOL_CLAMP	ANTICLIP_LS_VOL_CLAMP	0	SCART2_VOLUME_MODE	SCART1_VOLUME_MODE	HP_VOLUME_MODE	SRND_VOLUME_MODE	LS_VOLUME_MODE
R/W							

**Address:** D9h

**Type:** R/W

**Reset:** 1101 1111

[7] The output level is clamped depending on the HP bass-treble value to avoid any possible signal clipping on the HP output.

0: Volume clamp on HP output is not active  
 1: Volume clamp on HP output is active

[6] The output level is clamped depending on the LS equalizer or LS bass-treble value to avoid any possible signal clipping on the LS output.

0: Volume clamp on LS output is not active  
 1: Volume clamp on LS output is active

[5] Reserved

[4] Volume mode for SCART2 output:

0: Independent  
 1: Differential

[3] Volume mode for SCART1 output:

0: Independent  
 1: Differential

[2] Volume mode for headphone output:

0: Independent  
 1: Differential

[1] Volume mode for surround output:

0: Independent  
 1: Differential

[0] Volume mode for LS output:

0: Independent  
 1: Differential

- Note: 1 For the use of volume and balance control please refer to [Figure 13](#) and [Figure 14](#).  
 2 In differential mode the left register is used for volume control and the right register is used for balance control.

### LS\_L\_VOLUME\_MSB Loudspeaker left volume MSB

7	6	5	4	3	2	1	0
LS_L_VOLUME_MSB[7:0]							
R/W							

**Address:** DAh  
**Type:** R/W  
**Reset:** 1001 1000

[7:0] 8 MSBs of the 10-bit left loudspeaker volume

### LS\_L\_VOLUME\_LSB Loudspeaker left volume LSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_L_VOLUME_LSB[1:0]	
R/W							

**Address:** DBh  
**Type:** R/W  
**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit left loudspeaker volume

### LS\_R\_VOLUME\_MSB Loudspeaker right volume MSB

7	6	5	4	3	2	1	0
LS_R_VOLUME_MSB[7:0]							
R/W							

**Address:** DCh  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] 8 MSBs of the 10-bit right loudspeaker volume

**LS\_R\_VOLUME\_LSB Loudspeaker right volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_R_VOLUME_LSB[1:0]	
R/W							

**Address:** DDh**Type:** R/W**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit right loudspeaker volume

**LS\_C\_VOLUME\_MSB Loudspeaker center volume MSB**

7	6	5	4	3	2	1	0
LS_C_VOLUME_MSB[7:0]							
R/W							

**Address:** DEh**Type:** R/W**Reset:** 1001 1000

[7:0] 8 MSBs of the 10-bit center loudspeaker volume

**LS\_C\_VOLUME\_LSB Loudspeaker center volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_C_VOLUME_LSB[1:0]	
R/W							

**Address:** DFh**Type:** R/W**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit center loudspeaker volume

**LS\_SUB\_VOLUME\_MSB Loudspeaker subwoofer volume MSB**

7	6	5	4	3	2	1	0
LS_SUB_VOLUME_MSB[7:0]							
R/W							

**Address:** E0h**Type:** R/W**Reset:** 1001 1000

[7:0] 8 MSBs of the 10-bit subwoofer loudspeaker volume

**LS\_SUB\_VOLUME\_LSB Loudspeaker subwoofer volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_SUB_VOLUME_LSB[1:0]	
R/W							

**Address:** E1h**Type:** R/W**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit subwoofer loudspeaker volume

**LS\_SL\_VOLUME\_MSB Loudspeaker left surround volume MSB**

7	6	5	4	3	2	1	0
LS_SL_VOLUME_MSB[7:0]							
R/W							

**Address:** E2h**Type:** R/W**Reset:** 1001 1000

[7:0] 8 MSBs of the 10-bit left surround loudspeaker volume

**LS\_SL\_VOLUME\_LSB Loudspeaker left surround volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_SL_VOLUME_LSB[1:0]	
R/W							

**Address:** E3h  
**Type:** R/W  
**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit left surround loudspeaker volume

### LS\_SR\_VOLUME\_MSB Loudspeaker right surround volume MSB

7	6	5	4	3	2	1	0
LS_SR_VOLUME_MSB[7:0]							
R/W							

**Address:** E4h  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] 8 MSBs of the 10-bit right surround loudspeaker volume

### LS\_SR\_VOLUME\_LSB Loudspeaker right surround volume LSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_SR_VOLUME_LSB[1:0]	
R/W							

**Address:** E5h  
**Type:** R/W  
**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit right surround loudspeaker volume

### LS\_MASTER\_VOLUME\_MSB Loudspeaker master volume MSB

7	6	5	4	3	2	1	0
LS_MASTER_VOLUME_MSB[7:0]							
R/W							

**Address:** E6h  
**Type:** R/W  
**Reset:** 1110 1000

[7:0] 8 MSBs of the 10-bit master loudspeaker volume

**LS\_MASTER\_VOLUME\_LSB Loudspeaker master volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LS_MASTER_VOLUME_LSB[1:0]	
R/W							

**Address:** E7h**Type:** R/W**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit master loudspeaker volume

**HP\_L\_VOLUME\_MSB Headphone left volume MSB**

7	6	5	4	3	2	1	0
HP_L_VOLUME_MSB[7:0]							
R/W							

**Address:** E8h**Type:** R/W**Reset:** 1001 1000

[7:0] 8 MSBs of the 10-bit left headphone volume

**HP\_L\_VOLUME\_LSB Headphone left volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HP_L_VOLUME_LSB[1:0]	
R/W							

**Address:** E9h**Type:** R/W**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit left headphone volume

### HP\_R\_VOLUME\_MSB      Headphone right volume MSB

7	6	5	4	3	2	1	0
HP_R_VOLUME_MSB[7:0]							
R/W							

**Address:**      EAh  
**Type:**          R/W  
**Reset:**        0000 0000

[7:0] 8 MSBs of the 10-bit right headphone volume

### HP\_R\_VOLUME\_LSB      Headphone right volume LSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HP_R_VOLUME_LSB[1:0]	
R/W							

**Address:**      EBh  
**Type:**          R/W  
**Reset:**        0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit right headphone volume

### AUX\_VOLUME\_INDEX      Select the AUX to apply volume

7	6	5	4	3	2	1	0
0	0	0	0	0	0	AUX_VOLUME_SELECT[1:0]	
R/W							

**Address:**      ECh  
**Type:**          R/W  
**Reset:**        0000 0001

[7:2] Reserved

[1:0] Select the output on which the AUX\_VOLUME values will be applied:

00: No volume applied (*mandatory step to change selection from 01 to 10*)

01: Volume applied to SCART1 output

10: Volume applied to SCART2 output

11: Not used

**AUX\_L\_VOLUME\_MSB**      **Auxiliary left volume MSB**

7	6	5	4	3	2	1	0
AUX_L_VOLUME_MSB[7:0]							
R/W							

**Address:** EDh**Type:** R/W**Reset:** 1101 1101

[7:0] 8 MSBs of the 10-bit left auxiliary volume

**AUX\_L\_VOLUME\_LSB**      **Auxiliary left volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	AUX_L_VOLUME_LSB[1:0]	
R/W							

**Address:** EEh**Type:** R/W**Reset:** 0000 0000

[7:2] Reserved

[1:0] 2 LSBs of the 10-bit left auxiliary volume

**AUX\_R\_VOLUME\_MSB**      **Auxiliary right volume MSB**

7	6	5	4	3	2	1	0
AUX_R_VOLUME_MSB[7:0]							
R/W							

**Address:** EFh**Type:** R/W**Reset:** 0000 0000

[7:0] 8 MSBs of the 10-bit right auxiliary volume

**AUX\_R\_VOLUME\_LSB**      **Auxiliary right volume LSB**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	AUX_R_VOLUME_LSB[1:0]	
R/W							



**Address:** F0h  
**Type:** R/W  
**Reset:** 0000 0000

- [7:2] Reserved  
 [1:0] 2 LSBs of the 10-bit right auxiliary volume

## 10.15 Mute

### MUTE\_SOFTWARE                      Soft mute output by DSP

7	6	5	4	3	2	1	0
HP_D_MUTE	SPDIF_D_MUTE	SCART2_D_MUTE	SCART1_D_MUTE	SRND_D_MUTE	SUB_D_MUTE	C_D_MUTE	LS_D_MUTE
R/W							

**Address:** F1h  
**Type:** R/W  
**Reset:** 1111 1111

- [7] Digital soft mute for HP output:  
 0: Soft mute not active  
 1: Soft mute active
- [6] Digital soft mute for SPDIF output:  
 0: Soft mute not active  
 1: Soft mute active
- [5] Digital soft mute for SCART2 output:  
 0: Soft mute not active  
 1: Soft mute active
- [4] Digital soft mute for SCART1 output:  
 0: Soft mute not active  
 1: Soft mute active
- [3] Digital soft mute for SURROUND output:  
 0: Soft mute not active  
 1: Soft mute active
- [2] Digital soft mute for SUBWOOFER output:  
 0: Soft mute not active  
 1: Soft mute active
- [1] Digital soft mute for CENTER output:  
 0: Soft mute not active  
 1: Soft mute active
- [0] Digital soft mute for LOUDSPEAKER output:  
 0: Soft mute not active  
 1: Soft mute active

## 10.16 Beeper

### BEEPER\_ON Set beeper ON

7	6	5	4	3	2	1	0
0	0	0	0	0	BEEPER_SOUND_SELECT[1:0]	BEEPER_ON	
R/W							

**Address:** F2h  
**Type:** R/W  
**Reset:** 0000 0000

[7:3] Reserved

[2:1] Select the kind of sound generated by the beeper when BEEPER\_ON is set to 1:

00: Square wave signal. frequency and decay can be set in register 0xF4.  
 01: Wood block natural sound  
 10: Clic natural sound  
 11: Bleep natural sound.

[0] Control beeper sound Start/Stop:

0: Stop beeper  
 1: Start beeper

- Note:*
- 1 if BEEPER\_SOUND\_SELECT = 0 and BEEPER\_CONTINUOUS(reg 0xF3) is set to 1, the BEEPER\_ON needs to be set to 0 to stop the beeper sound; otherwise, the beeper is stopped automatically.
  - 2 On beeper STOP, the register 0xF2 is reset to 0. Take care to set bit[2:1] on each BEEPER\_ON action.
  - 3 Beeper parameters cannot be changed when BEEPER is ON.

### BEEPER\_MODE Beeper control

7	6	5	4	3	2	1	0
BEEPER_DECAY[2:0]			BEEPER_DURATION[1:0]		BEEPER_CONTINUOUS	BEEPER_PATH	
R/W							

**Address:** F3h  
**Type:** R/W  
**Reset:** 0100 0011

[7:5] Control the decay of the envelope of the beeper sound:

000: Short decay (sounds dry)  
 ...  
 111: Very long decay (sounds wet)

[4:3] Defines beeper duration when BEEPER\_CONTINUOUS is set to 0:

- 00: 0.1 sec.
- 01: 0.25 sec.
- 10: 0.5 sec.
- 11: 1 sec.

[2] Sets beeper mode:

- 0: Pulse mode selected, BEEPER\_ON is automatically reset to 0 after BEEPER\_DURATION.
- 1: Continuous mode selected, BEEPER\_ON must be set to 0 to stop the beeper sound.

[1:0] Sets the output channels when beeper is active:

- 00: No channels.
- 01: Loudspeakers only.
- 10: Headphone only.
- 11: Loudspeakers and headphone selected.

Note: *Beeper parameters cannot be changed when BEEPER is ON.*

### BEEPER\_FREQ\_VOL Beeper frequency and volume settings

	7	6	5	4	3	2	1	0
BEEP_FREQ[2:0]				BEEP_VOL[4:0]				
R/W								

**Address:** F4h  
**Type:** R/W  
**Reset:** 0111 0110

[7:5] Defines the frequency of the beeper tone from 62.5 Hz to 8 kHz in octaves:

- 000: 62.5 Hz
- 001: 125 Hz
- 010: 250 Hz
- 011: 00 Hz (default)
- 100: 1 kHz
- 101: 2 kHz
- 110: 4 kHz
- 111: 8 kHz

[4:0] Defines the beeper volume from 0 to -93 dB in steps of 3 dB.

- 11111: 0 dB (1 V<sub>RMS</sub>)      .....
- 11110: -3 dB                    00011
- 11101: -6 dB                    00010: -87 dB
- ...                                00001: -90 dB
- 10000: -48 dB (default)      00000: -93 dB

## 10.17 SPDIF output configuration

### SPDIF\_OUT\_CHANNEL\_STATUS SPDIF output channel configuration

	7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPDIF_COPYRI GHT	SPDIF_NO_PC M	SPDIF_CONSU MER_PRO
R/W								

**Address:** F5h  
**Type:** R/W  
**Reset:** 0000 0000

- [7:3] Reserved
- [2] 0: Copyright  
1: No copyright
- [1] 0: PCM format  
1: No PCM format
- [0] 0: Consumer format  
1: Professional format

## 10.18 Headphone configuration

### HEADPHONE\_CONFIG Headphone configuration

7	6	5	4	3	2	1	0
0	0	SCARTaux_OUT_SELECT[1:0]	HP_FORCE	HP_LS_MUTE	HP_DET_ACTIV E	HP_DETECTED	
R/W							

**Address:** F6h  
**Type:** R/W  
**Reset:** 0000 0010

- [7:6] Reserved
- [5:4] Select SCARTaux output:
  - 00: SCARTaux not output
  - 01: SCARTaux signal output on C/Sub DAC
  - 10: SCARTaux signal output on Srnd/HP DAC
  - 11: Not used
- [3] 1: Force to output the HP signal (bypass surround)  
 Note: When HP is forced, IRQ5 and HP/Srnd DAC automatic mute are not active.
- [2] 0: When HP is detected and active, LS is not muted  
 1: When HP is detected and active, LS is muted
- [1] 0: HP detection is not active  
 1: HP detection is active, when HP detected, surround signal is bypassed and HP signal is outputted on HP
- [0] 1: When a signal is detected on HP\_DET pin

## 10.19 DAC control

### DAC\_CONTROL DAC control

7	6	5	4	3	2	1	0
0	0	SPDIF_MUX	DAC_SCART_MUTE	DAC_SHP_MUTE	DAC_CSUB_MUTE	DAC_LSLR_MUTE	POWER_UP
R/W							

**Address:** F7h

**Type:** R/W

**Reset:** 0001 1111

[7:6] Reserved

[5] Redirect external or internal source i2s to i2s output:

0: Internal source (PCM format)  
1: External source on SPDIF\_IN pin

[4] SCART left/right analog soft mute:

0: Soft mute not active  
1: Soft mute active

[3] Surround/HP left/right analog soft mute:

0: Soft Mute not active  
1: Soft Mute active

[2] Center/Subwoofer analog soft mute:

0: Soft mute not active  
1: Soft mute active

[1] LS left/right analog soft mute

0: Soft mute not active  
1: Soft mute active

[0] 0: DACs power OFF

1: Power ON

### SW1\_CHANNELS DAC SW channel

7	6	5	4	3	2	1	0
C_SUB_SW	SUR_HP_SW		SCART_SW		SPDIF_SW		
R/W							

**Address:** F8h

**Type:** R/W

**Reset:** 0000 0000

[7:6] Center/Sub DAC:

00: Left/Right channels non inverted  
11: Left/Right channels inverted

- [5:4] Surround/HP DAC:  
 00: Left/Right channels non inverted  
 11: Left/Right channels inverted
- [3:2] SCART DAC:  
 00: Left/Right channels non inverted  
 11: Left/Right channels inverted
- [1:0] SPDIF:  
 00: Left/Right channels non inverted  
 11: Left/Right channels inverted

**SW2\_CHANNELS****SPDIF SW channel**

7	6	5	4	3	2	1	0
0	0	0	0	DELAY_SW		LS_L_R_SW	
R/W							

**Address:** F9h  
**Type:** R/W  
**Reset:** 0000 0000

- [7:4] Reserved
- [3:2] Delay output:  
 00: Left/Right channels non inverted  
 11: Left/Right channels inverted
- [1:0] Loudspeaker L/R output:  
 00: Left/Right channels non inverted  
 11: Left/Right channels inverted

- Note:**
- 1 To switch the outputs between non-inverted and inverted mode it is necessary to stop and start the DSP with the *HOST\_RUN* bit while keeping *REGISTERS\_RESET* bit on (*I<sup>2</sup>C* register table not initialized).
  - 2 These bits can be used to swap the outputs on corresponding DAC outputs or on *I<sup>2</sup>S* outputs.
  - 3 Non-inverted or inverted modes are the same on all *I2S* outputs (*I2S\_DATA0*, *I2S0\_DATA0*, *I2S0\_DATA1*).

## 10.20 Autostandard coefficients settings

### AUTOSTD\_COEFF\_CTRL Autostandard coefficients control

7	6	5	4	3	2	1	0
0	0	0	0	0	0	AUTOSTD_COEFF_CTRL[1:0]	
R/W							

**Address:** FBh  
**Type:** R/W  
**Reset:** 0000 0001

[7:2] Reserved

[1:0] Control the demod filter coefficients table settings:

00: No action

01: Init coefficients to ROM values

10: Update coefficients with I<sup>2</sup>C values (set to 0 by DSP to acknowledge)

### AUTOSTD\_COEFF\_INDEX\_MSB Autostandard coefficients index MSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	AUTOSTD_COEFF_INDEX_MSB
R/W							

**Address:** FCh  
**Type:** R/W  
**Reset:** 0000 0000

[7:1] Reserved

[0] FIR coefficients table index (MSB)

### AUTOSTD\_COEFF\_INDEX\_LSB Autostandard coefficients index LSB

7	6	5	4	3	2	1	0
AUTOSTD_COEFF_INDEX_LSB[7:0]							
R/W							

**Address:** FDh  
**Type:** R/W  
**Reset:** 0000 0000

[7:0] FIR coefficients table index (LSB)

**AUTOSTD\_COEFF\_VALUE      Autostandard coefficient value**

7	6	5	4	3	2	1	0
AUTOSTD_COEFF_VALUE[7:0]							
R/W							

**Address:**      FEh  
**Type:**          R/W  
**Reset:**          0000 0000

[7:0] FIR coefficients table value to update

*Note:*      *These four registers (AUTOSTD\_COEFF\_CTRL, AUTOSTD\_COEFF\_INDEX\_MSB, AUTOSTD\_COEFF\_INDEX\_LSB and AUTOSTD\_COEFF\_VALUE) can be used to change parameter settings for the following parts of channel 1 or channel 2:*

- Channel carrier DCO frequency (register CARFQxx)
- Channel filter coefficients (registers FIRxCx)
- PLL baseband AM/FM demodulators proportional and integral coefficients (registers ACOEFFx or BCOEFFx)
- Demodulator mode selection (register DEMOD\_CTRL)
- IF AGC control (AGC\_CTRL)
- Channel 2 symbol tracking loop parameters (register SCOEFF)
- Zweiton control (register ZWT\_CTRL)

**While keeping the AUTOSTANDARD function always active.**

New values for all parameters mentioned above are kept instead of the values automatically sent by the AUTOSTANDARD function.

One application is for example to implement OVERMODULATION recovery mode for any sound standard supported by the device (B/G, I, M/N, DK1, DK2, or DK3).

*See Technical Note for instructions on how to update the coefficient table settings.*

**PATCH\_VERSION                  Patch version**

7	6	5	4	5	2	1	0
PATCH_VERSION[7:0]							
R/W							

**Address:**      FFh  
**Type:**          R/W  
**Reset:**          0000 0000

[7:0] Indicates the patch version which has been loaded in the device (can be used to check if the patch has been correctly loaded)



## 11 Pin descriptions

### 11.1 TQFP 80-pin package

- AP = Analog power
- DP = Digital power
- I= Input
- O = Output
- OD = Open-drain
- B = Bi-directional
- A = Analog

**Table 19. TQFP80 pin description**

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8 (function for STV82x6 in italic characters)	STV82x6 pin name
1	SC1_OUT_L	A	SCART1 audio output left	AO1L
2	SC1_OUT_R	A	SCART1 audio output right	AO1R
3	VCC_H	AP	8V power for audio I/O & ESD	Not connected
4	GND_H	AP	High current ground for audio outputs	Connected to ground
5	SC3_OUT_L	A	SCART3 audio output left	Not connected
6	SC3_OUT_R	A	SCART3 audio output right	Not connected
7	VCC33_SC	AP	3.3V power for audio buffers & DAC / ADC	VDDC
8	GND33_SC	AP	Ground for audio buffers & DAC / ADC	GNDC
9	SC1_IN_L	A	SCART1 audio input left	AI1L
10	SC1_IN_R	A	SCART1 audio input right	AI1R
11	VREFA	A	Audio bias voltage decoupling 1.55V (Switched $V_{REF}$ decoupling pin for Audio Converters (VMCP))	VMC1
12	NC (GND_SA in STV82x7)	AP		Connected to ground
13	VBG	A	Bandgap voltage reference decoupling 1.2V ( $V_{REF}$ decoupling pin for Audio Converters (VMC))	VMC2
14	SC2_IN_L	A	SCART 2 audio input left	AI2L
15	SC2_IN_R	A	SCART 2 audio input right	AI2R
16	VCC33_LS	AP	3.3V power for audio DACs (3.3V power supply for audio buffers and SCART)	VDDA
17	GND33_LS	AP	Ground for audio DACs (ground for audio buffers and SCART)	GNDAH
18	SC2_OUT_L	A	SCART 2 audio output left	AO2L
19	SC2_OUT_R	A	SCART 2 audio output right	AO2R

Table 19. TQFP80 pin description (continued)

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8 (function for STV82x6 in italic characters)	STV82x6 pin name
20	GND_SA (VCC_NISO in STV82x7)	AP	Ground for DACs	VDDH
21	VSS33_CONV	AP	Ground for DAC 1.8 to 3.3V converters	Connected to Ground
22	VDD33_CONV	AP	3.3V Power for DAC 1.8 to 3.3V converters <i>(voltage reference for audio buffers)</i>	VREFA
23	SC3_IN_L	A	SCART 3 audio Input left	AI3L
24	SC3_IN_R	A	SCART 3 audio Input right	AI3R
25	SCL_FLT	A	SCART filtering left	Not connected
26	SCR_FLT	A	SCART filtering right <i>(bandgap voltage source decoupling)</i>	BGAP
27	LS_C	A	Center output	Not connected
28	LS_L	A	Left loudspeaker output	LSL
29	LS_R	A	Right loudspeaker output	LSR
30	LS_SUB	A	Subwoofer output	SW
31	HP_LSS_L	A	Left headphone output or left surround output	HPL
32	HP_LSS_R	A	Right headphone output or right surround output	HPR
33	VSS18_CONV	DP	Ground for digital part of the DAC/ADC <i>(Substrate analog/digital shield)</i>	GNDSA
34	VDD18_CONV	DP	1.8V power for digital part of the DAC/ADC	Not connected
35	HP_DET	I	Headphone detection	HPD
36	ADR_SEL	I	Hardware address selection for I <sup>2</sup> C bus	ADR
37	VSS18	DP	Ground for digital part	Connected to ground
38	VDD18	DP	1.8V power for digital part	Not connected
39	SCL	OD	I <sup>2</sup> C clock Input	SCL
40	SDA	OD	I <sup>2</sup> C data I/O	SDA
41	VSS18	DP	Ground for digital part	Connected to Ground
42	VDD18	DP	1.8V power for digital part <i>(5V power regulator control)</i>	REG
43	RST_N	I	Main reset input	RESET
44	S/PDIF_IN	I	Serial audio data input <i>(System clock output)</i>	SYSCK
45	S/PDIF_OUT	O	Serial audio data output <i>(I<sup>2</sup>S master clock output)</i>	MCK
46	VDD33_IO1	DP	3.3V power for digital IO	VDD1
47	VSS33_IO1	DP	Ground for digital IO	GND1

Table 19. TQFP80 pin description (continued)

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8 (function for STV82x6 in italic characters)	STV82x6 pin name
48	CK_TST_CTRL	D	To be grounded	Not connected
49	VSS18	DP	Ground for digital part	GNDSP
50	VDD18	DP	1.8V power for digital part	Not connected
51	CLK_SEL	I	Clock Input format selection	Not connected
52	XTALIN_CLKXTP	I	Crystal oscillator input or differential input positive <i>(Crystal oscillator input)</i>	XTI
53	XTALOUT_CLKX TM	O	Crystal oscillator output or differential input negative <i>(Crystal oscillator output)</i>	XTO
54	VCC18_CLK1	AP	1.8V Power for Clock PLL Analog & Crystal Oscillator 1/2 <i>(3.3V Power supply for analog PLL clock)</i>	VDDP
55	GND18_CLK1	AP	Ground for clock PLL analog & crystal oscillator 1/2	GNDP
56	GND18_CLK2	DP	Ground for clock PLL digital 1/2	GND2
57	VCC18_CLK2	DP	1.8V power for clock PLL digital 1/2 <i>(3.3V Power supply for digital core, DSPs &amp; IO cells)</i>	VDD2
58	VSS33_IO2	DP	Ground for digital IO	Connected to Ground
59	VDD33_IO2	DP	3.3V power for digital IO	Not connected
60	I2S_PCM_CLK	I/O	I <sup>2</sup> S master clock input/output channel 0, 1 & 2	Not connected
61	I2S_SCLK	I/O	I <sup>2</sup> S serial clock input/output channel 0, 1 & 2 (I <sup>2</sup> S bus data output)	SDO
62	I2S_LR_CLK	I/O	I <sup>2</sup> S word select input/output channel 0, 1 & 2 <i>(Stereo detection output / I<sup>2</sup>S bus data input)</i>	ST/SDI
63	I2S_DATA0	I/O	I <sup>2</sup> S data input/output stereo channel 0 <i>(I<sup>2</sup>S bus word select output)</i>	WS
64	I2S_DATA1	I	I <sup>2</sup> S data input stereo channel 1 <i>(I<sup>2</sup>S bus clock output)</i>	SCK
65	I2S_DATA2	I	I <sup>2</sup> S Data Input Stereo Channel 2 <i>(Bus expander output 1)</i>	BUS1
66	VDD18	DP	1.8V power for digital core & I/O cells pin	Not connected
67	VSS18	DP	Ground for digital core & I/O cells pin	Connected to ground
68	BUS_EXP	O	Bus expander function <i>(Bus expander output 2)</i>	BUS0
69	IRQ	O	Interrupt request to microprocessor	IRQ
70	GND_PSUB	AP	Ground substrate connection	Connected to ground
71	VDD18_ADC	DP	VDD 1.8V for ADC (digital part)	Not connected
72	VSS18_ADC	DP	Ground to Complement 1.8V VDD for ADC	Connected to ground
73	SIF_P	A	Sound IF input	SIF

Table 19. TQFP80 pin description (continued)

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8 (function for STV82x6 in italic characters)	STV82x6 pin name
74	SIF_N	A	ADC $V_{TOP}$ decoupling pin	VTOP
75	GNDPW_IF	AP	Polarization for the IF block <i>(Voltage reference for AGC decoupling pin)</i>	VREFIF
76	VCC18_IF	AP	1.8V power for IF AGC & ADC	VDDIF
77	GND18_IF	AP	Ground for IF AGC & ADC	GNDIF
78	MONO_IN	A	Mono input (for AM mono)	MONOIN
79	SC4_IN_L	A	SCART4 audio input left	Not connected
80	SC4_IN_R	A	SCART4 audio input right	Not connected

## 11.2 TQFP 100-pin package

- AP = Analog Power
- DP = Digital Power
- I= Input
- O = Output
- OD = Open-Drain
- B = Bi-Directional
- A = Analog

Table 20. TQFP100 pin description

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8
1	SC1_OUT_L	A	SCART1 audio output left
2	SC1_OUT_R	A	SCART1 audio output right
3	VCC_H	AP	8V power for audio I/O & ESD
4	GND_H	AP	High current ground for audio outputs
5	SC3_OUT_L	A	SCART3 audio output left
6	SC3_OUT_R	A	SCART3 audio output right
7	VCC33_SC	AP	3.3V power for audio buffers & DAC / ADC
8	GND33_SC	AP	Ground for audio buffers & DAC / ADC
9	SC1_IN_L	A	SCART1 audio Input left
10	SC1_IN_R	A	SCART1 audio Input right
11	VREFA	A	Audio bias voltage decoupling 1.55V
12	VBG	A	Bandgap voltage reference decoupling 1.2V
13	SC2_IN_L	A	SCART 2 audio input left
14	SC2_IN_R	A	SCART 2 audio input right

Table 20. TQFP100 pin description (continued)

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8
15	VCC33_LS	AP	3.3V power for audio DACs
16	GND33_LS	AP	Ground for audio DACs
17	SC2_OUT_L	A	SCART 2 audio output left
18	SC2_OUT_R	A	SCART 2 audio output right
19	SC5_IN_L	A	SCART 5 audio Input left
20	SC5_IN_R	A	SCART 5 audio Input right
21	NC		Not to be connected
22	NC		Not to be connected
23	GND_SA	AP	Ground for DACs
24	NC		Not to be connected
25	NC		Not to be connected
26	VSS33_CONV	AP	Ground for DAC 1.8 to 3.3V converters
27	VDD33_CONV	AP	3.3V Power for DAC 1.8 to 3.3V converters
28	SC3_IN_L	A	SCART 3 audio Input left
29	SC3_IN_R	A	SCART 3 audio Input right
30	SCL_FLT	A	SCART filtering left
31	SCR_FLT	A	SCART filtering right
32	LS_C	A	Center output
33	NC		Not to be connected
34	LS_L	A	Left loudspeaker output
35	NC		Not to be connected
36	LS_R	A	Right loudspeaker output
37	NC		Not to be connected
38	LS_SUB	A	Subwoofer output
39	NC		Not to be connected
40	HP_LSS_L	A	Left headphone output or left surround output
41	NC		Not to be connected
42	HP_LSS_R	A	Right headphone output or right surround output
43	NC		Not to be connected
44	NC		Not to be connected
45	VSS18_CONV	DP	Ground for digital part of the DAC/ADC
46	VDD18_CONV	DP	1.8V power for digital part of the DAC/ADC
47	HP_DET	I	Headphone detection
48	ADR_SEL	I	Hardware address selection for I <sup>2</sup> C Bus

Table 20. TQFP100 pin description (continued)

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8
49	VSS18	DP	Ground for digital part
50	VDD18	DP	1.8V power for digital part
51	SCL	OD	I <sup>2</sup> C clock input
52	SDA	OD	I <sup>2</sup> C Data I/O
53	RST_N	I	Main reset input
54	I2SD_DATA	I	I <sup>2</sup> S data delay input stereo channel
55	I2SO_DATA1	O	I <sup>2</sup> S data output stereo channel O_1
56	I2SO_LR_CLK	O	I <sup>2</sup> S word select output channel O_0 & O_1
57	I2SO_SCLK	O	I <sup>2</sup> S serial clock output channel O_0 & O_1
58	I2SO_DATAO	O	I <sup>2</sup> S data output stereo channel O_0
59	S/PDIF_IN	I	Serial audio data input
60	S/PDIF_OUT	O	Serial audio data output
61	VDD33_IO1	DP	3.3V power for digital IO
62	VSS33_IO1	DP	Ground for digital IO
63	CK_TST_CTRL	D	To be grounded
64	VSS18	DP	Ground for digital part
65	VDD18	DP	1.8V power for digital part
66	CLK_SEL	I	Clock input format selection
67	XTALIN_CLKXTP	I	Crystal oscillator input or differential input positive
68	XTALOUT_CLKXTM	O	Crystal oscillator output or differential input negative
69	VCC18_CLK1	AP	1.8V power for clock PLL analog & crystal oscillator 1/2
70	GND18_CLK1	AP	Ground for clock PLL analog & crystal oscillator 1/2
71	GND18_CLK2	DP	Ground for clock PLL digital 1/2
72	VCC18_CLK2	DP	1.8V power for clock PLL digital 1/2
73	VSS33_IO2	DP	Ground for digital IO
74	VDD33_IO2	DP	3.3V power for digital IO
75	I2S_PCM_CLK	I/O	I <sup>2</sup> S master clock input/output channel 0, 1 & 2
76	I2S_SCLK	I/O	I <sup>2</sup> S serial clock input/output channel 0, 1 & 2
77	I2S_LR_CLK	I/O	I <sup>2</sup> S word select input/output channel 0,1 & 2
78	I2S_DATA0	I/O	I <sup>2</sup> S data input/output stereo channel 0
79	I2S_DATA1	I	I <sup>2</sup> S data input stereo channel 1
80	I2S_DATA2	I	I <sup>2</sup> S data input stereo channel 2
81	NC		Not to be connected
82	NC		Not to be connected

Table 20. TQFP100 pin description (continued)

Pin no.	STV82x8 pin name	Type (STV82x8)	Function for STV82x8
83	NC		Not to be connected
84	NC		Not to be connected
85	VDD18	DP	1.8V power for digital core & I/O cells pin
86	VSS18	DP	Ground for digital core & I/O cells pin
87	BUS_EXP	O	Bus expander function
88	IRQ	O	Interrupt request to microprocessor
89	GND_PSUB	AP	Ground substrate connection
90	VDD18_ADC	DP	VDD 1.8V for ADC (Digital Part)
91	VSS18_ADC	DP	Ground to complement 1.8V VDD for ADC
92	SIF_P	A	Sound IF input 1
93	SIF_N	A	ADC $V_{TOP}$ decoupling pin
94	SIF2_P	A	Sound IF input 2
95	GNDPW_IF	AP	Polarization for the IF block
96	VCC18_IF	AP	1.8V power for IF AGC & ADC
97	GND18_IF	AP	Ground for IF AGC & ADC
98	MONO_IN	A	Mono input (for AM mono)
99	SC4_IN_L	A	SCART 4 audio input left
100	SC4_IN_R	A	SCART 4 audio input right

Note: Pins indicated as **Not to be Connected** should have no connection at all even to ground.

# 12 Application diagrams

Figure 29. STV82x8 TQFP80 application diagram

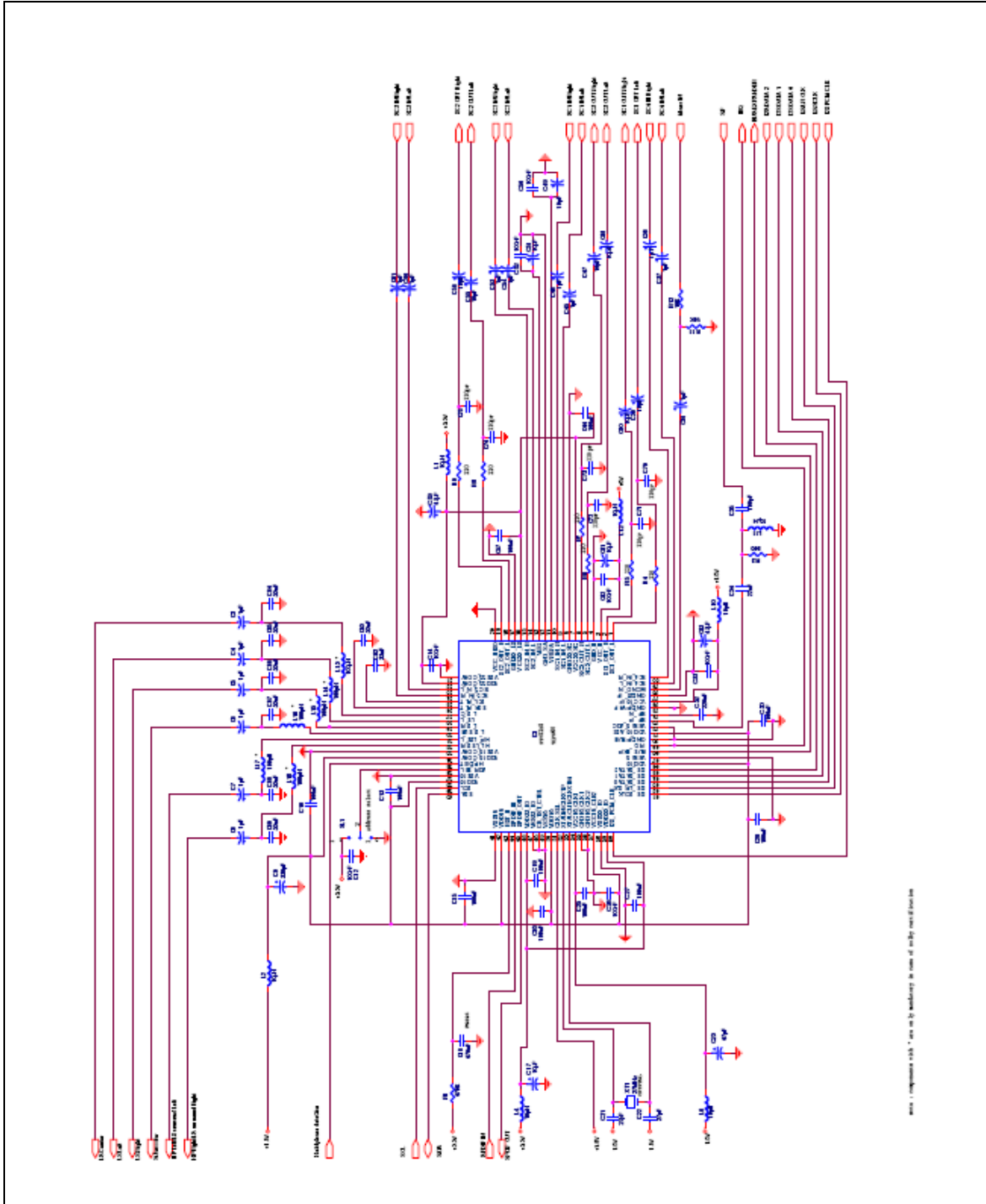




Figure 30. STV82x8 TQFP100 application diagram

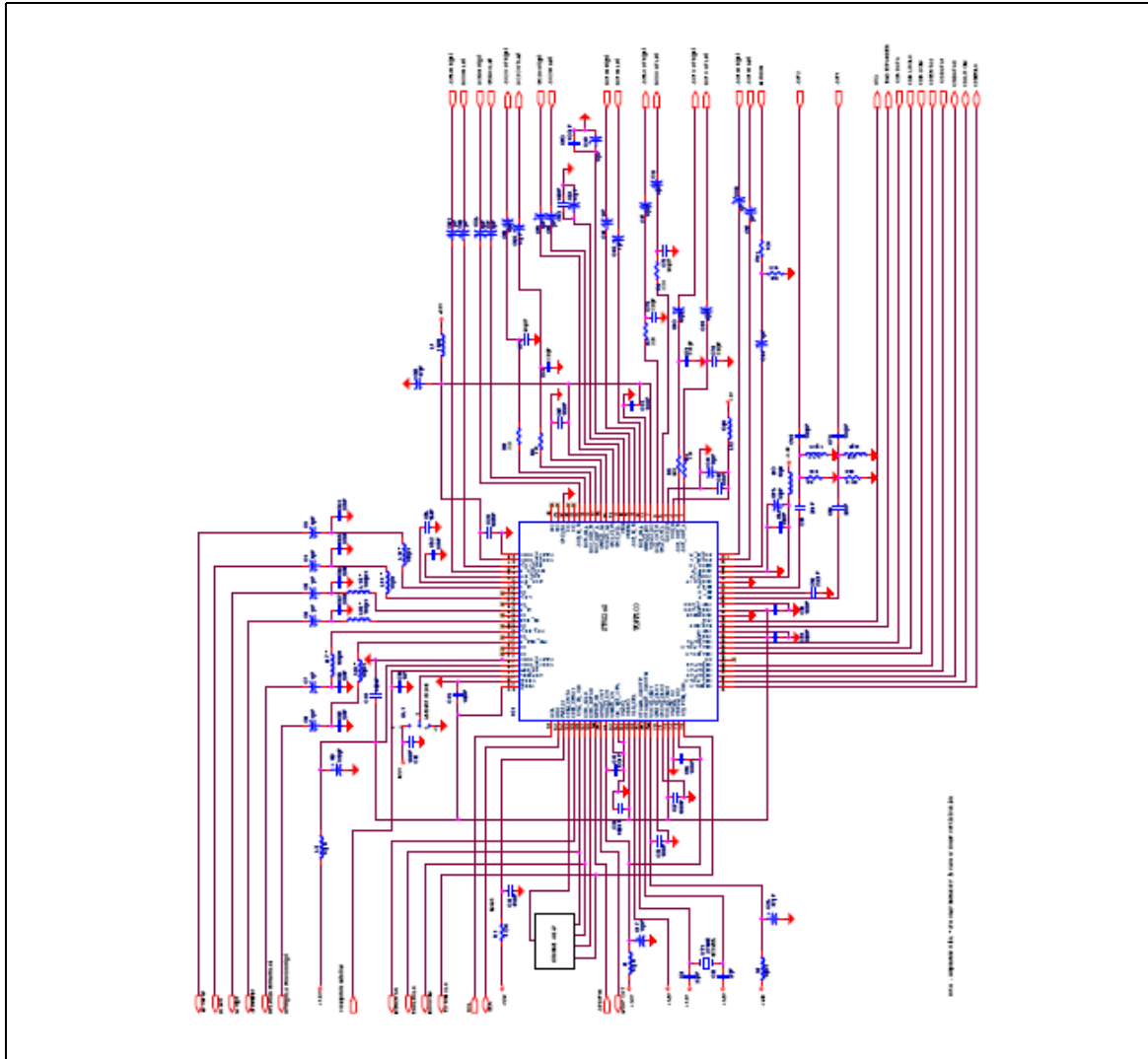
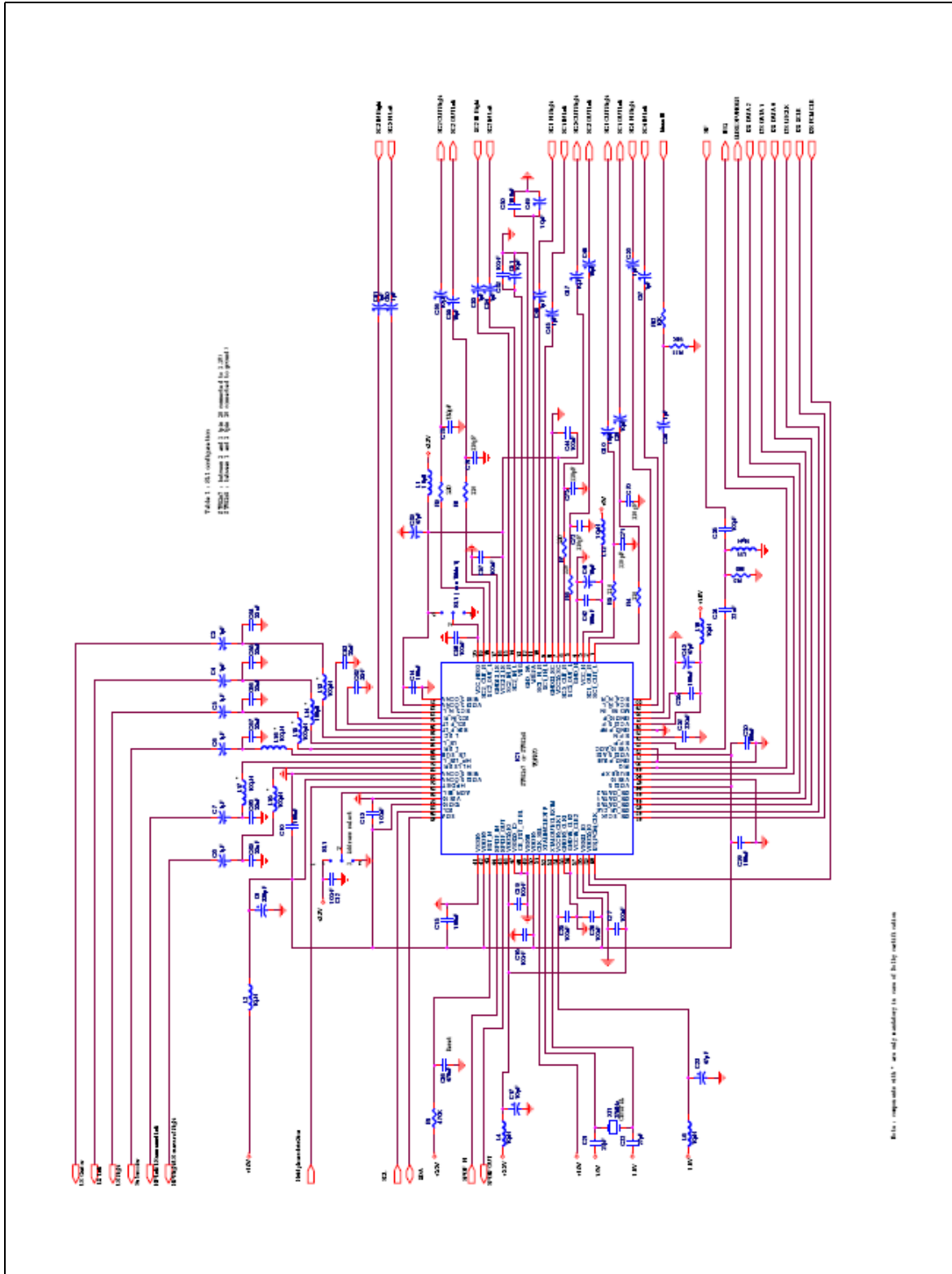
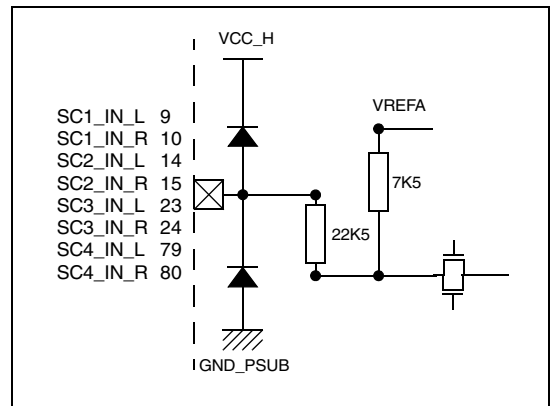
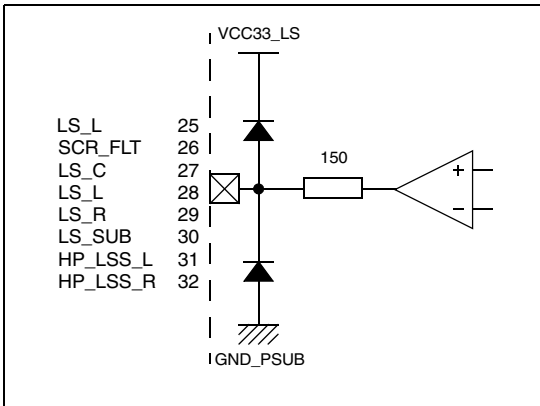
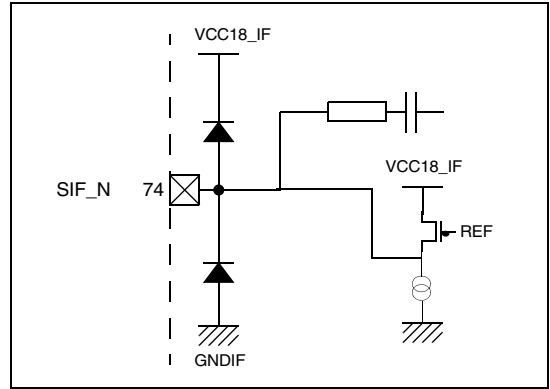
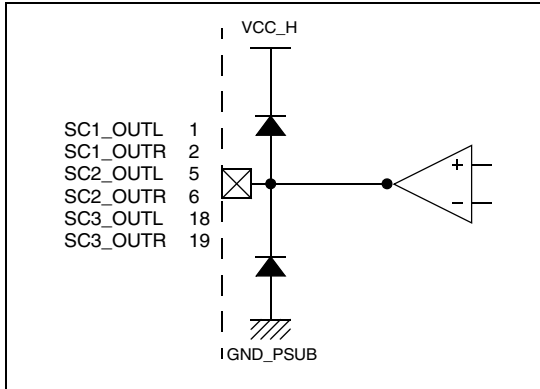
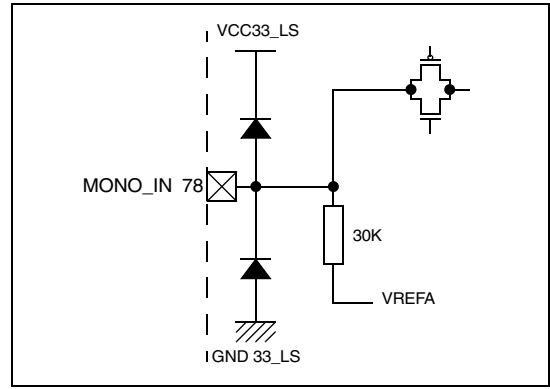
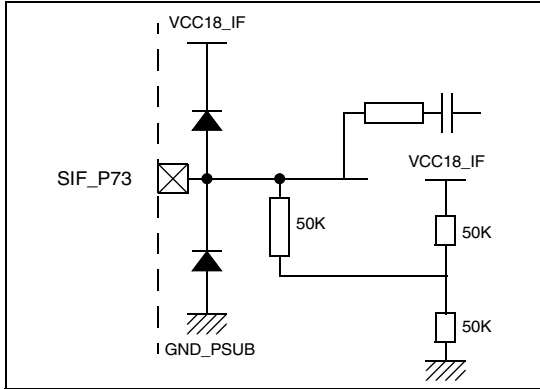


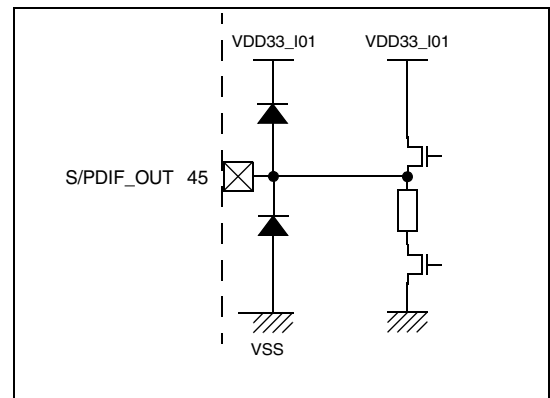
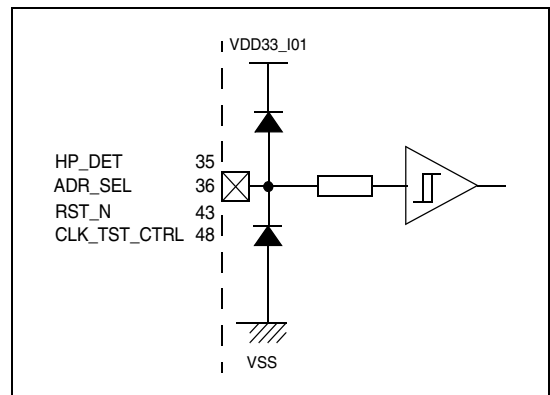
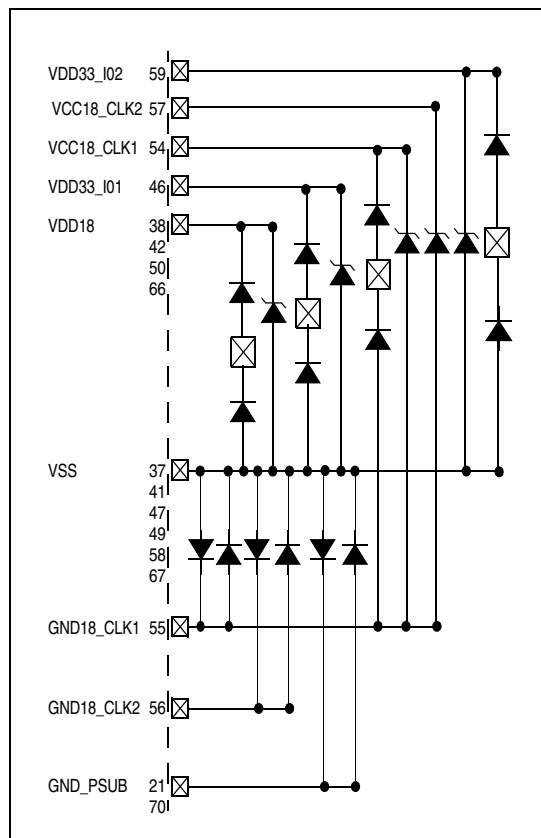
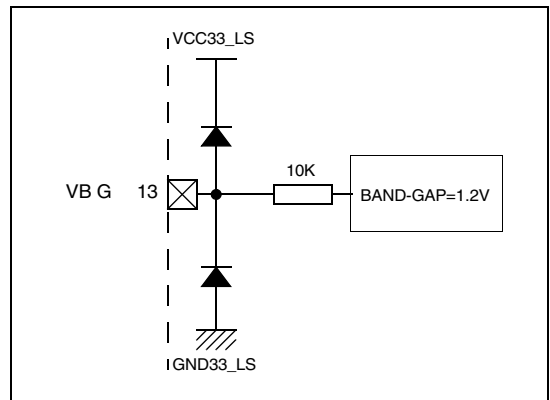
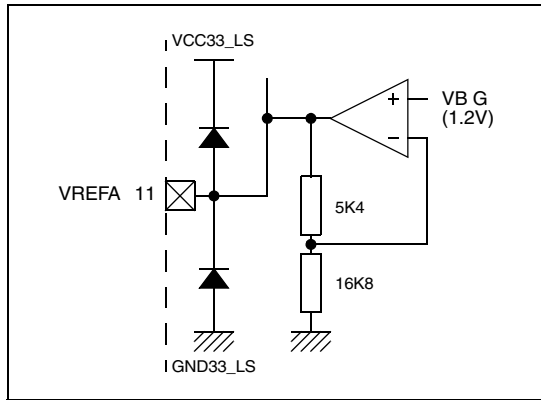
Figure 31. STV82x7/STV82x8 TQFP80 compatibility application diagram

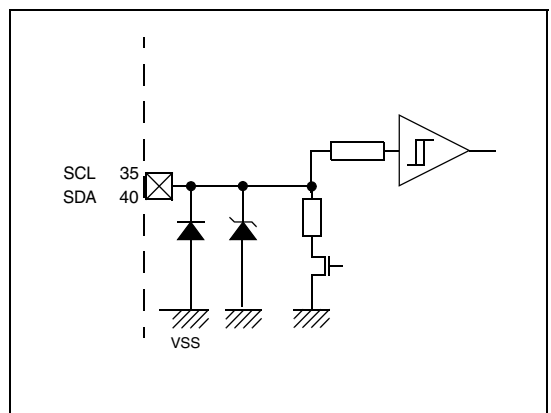
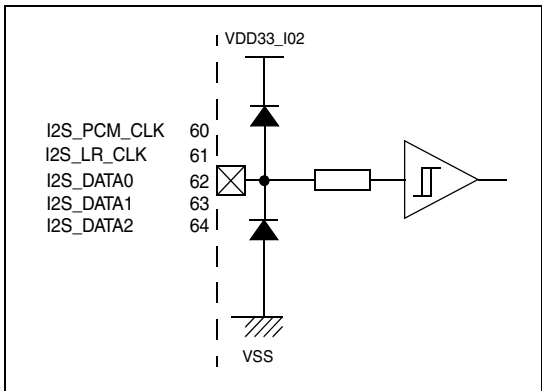
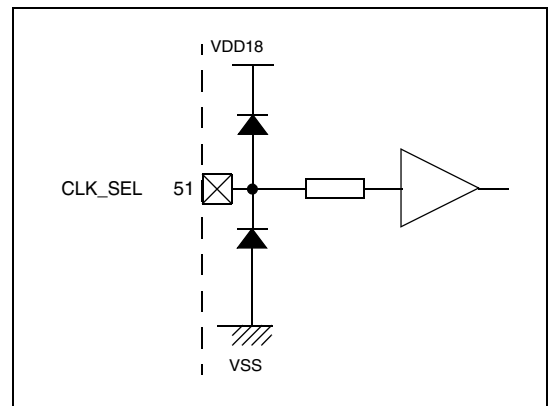
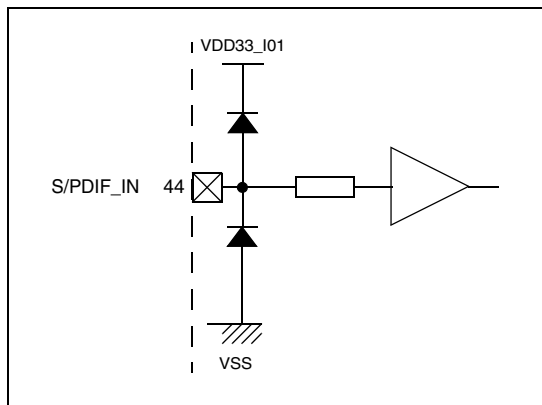
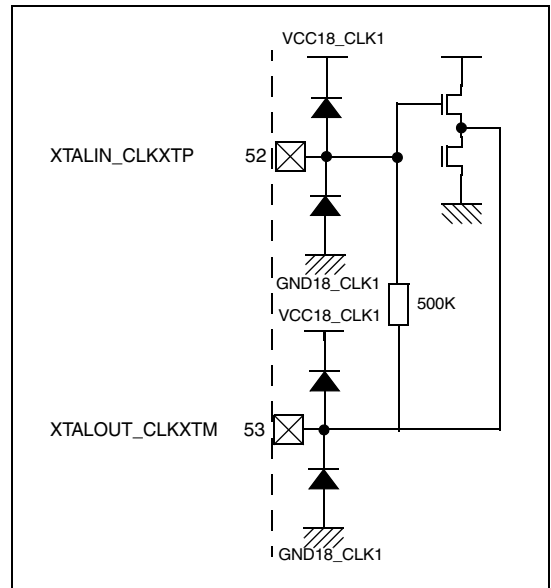
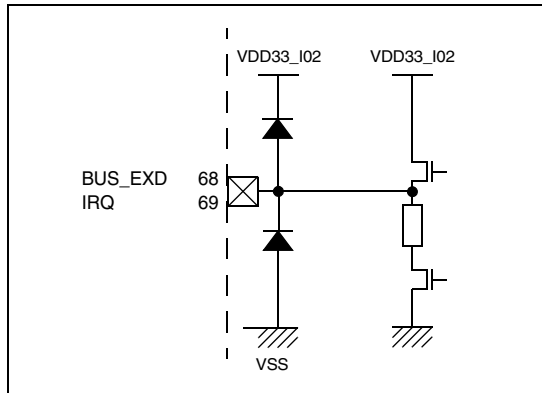


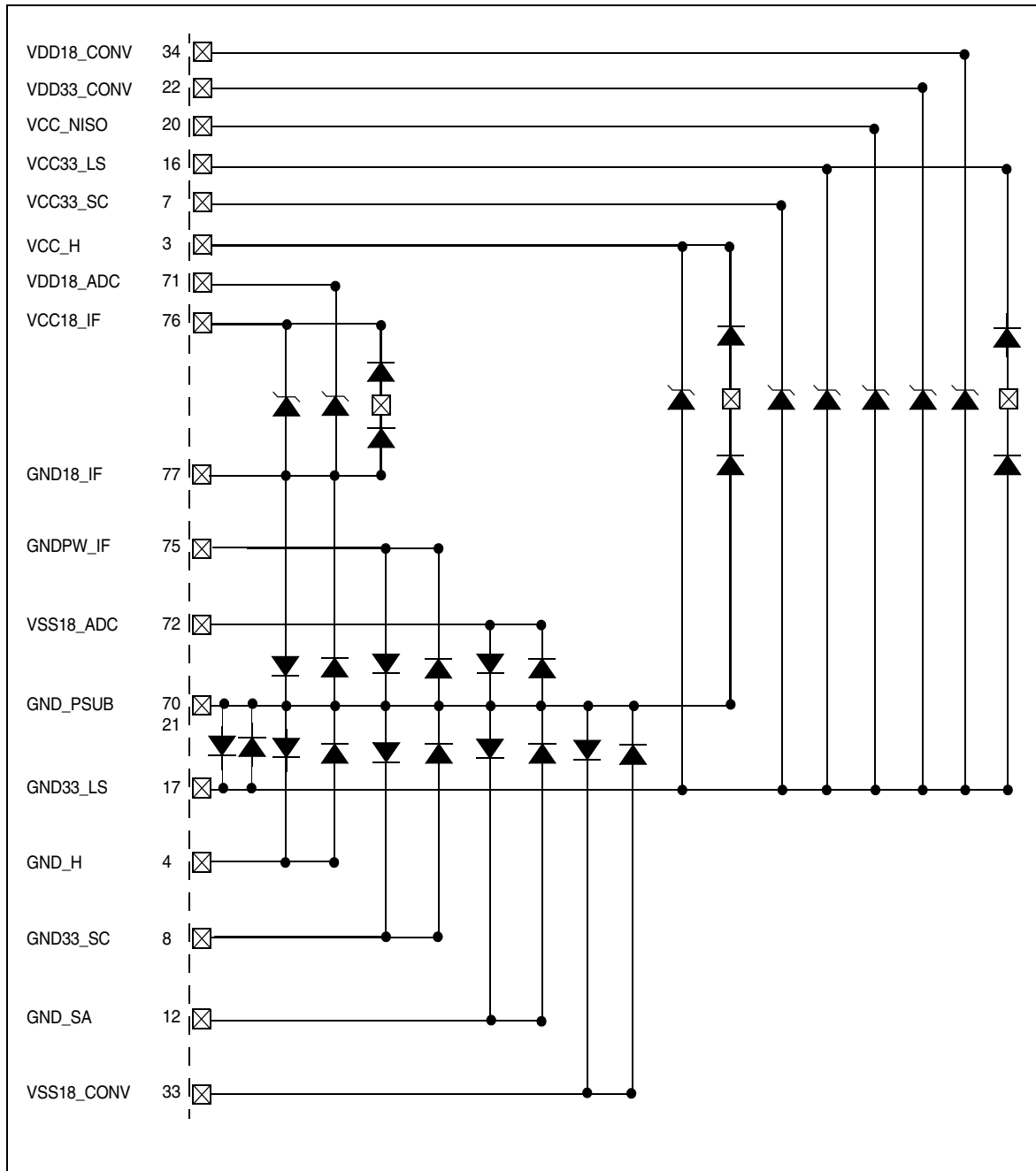
# 13 Input/Output groups

Pin numbers apply to TQFP80 package only.









# 14 General description

This chip performs BTSC stereo and SAP analog TV stereo sound identification and demodulation (no specific I<sup>2</sup>C programming is required). It offers various audio processing functions such as equalization, loudness, beeper, volume, balance, and surround effects. It provides a cost-effective solution for analog and digital TV designs.

The STV82x8 is an audio processor which integrates SRS<sup>®</sup>, WOW<sup>™</sup>, SRS<sup>®</sup> TruSurround XT<sup>™</sup>, Dolby<sup>®</sup>, Pro Logic<sup>®</sup>, Dolby<sup>®</sup>, Pro Logic II<sup>®</sup>, Virtual Dolby<sup>®</sup>, Surround (VDS) and Virtual Dolby<sup>®</sup>, Digital (VDD) capabilities.

Advanced ST royalty-free algorithms such as ST OmniSurround<sup>™</sup>, ST WideSurround<sup>™</sup>, ST Dynamic Bass<sup>™</sup> are also available in this audio sound processor. ST OmniSurround<sup>™</sup> is a certified Dolby<sup>®</sup>, algorithm for the Virtual Dolby<sup>®</sup>, Digital (VDD) and the Virtual Dolby<sup>®</sup>, Surround (VDS). When using VDD or VDS, either an external Dolby<sup>®</sup>, Digital or an internal Pro Logic<sup>®</sup>, (or Pro Logic II<sup>®</sup>) decoder must be used respectively.

The STV82x8 is perfectly suited to current and future digital TV platforms, based on audio/video digital chips (STD2000 - DTV100 platform) which include an internal digital decoder (MPEG, Dolby<sup>®</sup>, Digital...). In the case where a Dolby<sup>®</sup>, Digital decoder is embedded in the audio/video digital chip, Virtual Dolby<sup>®</sup>, Digital certification could be obtained.

**Table 21. STV8x8 version list (TQFP 80)**

	S T V 8 2 1 8	S T V 8 2 3 8	STV8248		STV8258			STV8268		STV8278		STV8288	
			S T V 8 2 4 8 D S X	S T V 8 2 4 8 D S X	S T V 8 2 5 8 D S X	S T V 8 2 5 8 D S X	S T V 8 2 5 8 D S X	S T V 8 2 6 8 D S X	S T V 8 2 6 8 D S X	S T V 8 2 7 8 D S X	S T V 8 2 7 8 D S X	S T V 8 2 8 8 D S X	S T V 8 2 8 8 D S X
<b>Demodulation</b>													
BTSC & DBX Noise Reduction	X	X	X	X	X	X	X	X	X	X	X	X	X
<b>Multi-channel capabilities</b>													
Analog loudspeakers output number	2.1	2.1	2.1	2.1	2.1	2.1	2.1	5.1	5.1	5.1	5.1	5.1	5.1
I <sup>2</sup> S In ( <u>exclusive</u> with I <sup>2</sup> S out)	1	1	1	1	3	3	3	1	1	3	3	3	3
S/PDIF (pass-thru or output)	1	1	1	1	1	1	1	1	1	1	1	1	1
Virtual Dolby <sup>®</sup> Surround			X	X	X	X		X	X	X	X	VDS PLII	VDS PLII

Table 21. STV8x8 version list (TQFP 80) (continued)

	S T V 8 2 1 8	S T V 8 2 3 8	STV8248		STV8258			STV8268		STV8278		STV8288	
			S T V 8 2 4 8 D	S T V 8 2 4 8 D S X	S T V 8 2 5 8 D	S T V 8 2 5 8 D S X	S T V 8 2 5 8 S X	S T V 8 2 6 8 D	S T V 8 2 6 8 D S X	S T V 8 2 7 8 D	S T V 8 2 7 8 D S X	S T V 8 2 8 8 D	S T V 8 2 8 8 D S X
Virtual Dolby® Digital capability <sup>(1)</sup>					X	X	X			X	X	X	X
Dolby® Pro Logic® (DPLI) or Dolby® Pro Logic II® (DPLII)			DPLI (internal)	DPLI (internal)	DPLI (internal)	DPLI (internal)		DPL I	DPL I	DPL I	DPL I	DPL II	DPL II
<b>Audio processing</b>													
SRS® WOW™ (WOW)		X											
SRS® TruSurround XT™				X		X	X		X		X		X
ST Voice™, ST Dynamic Bass™	X	X	X	X	X	X	X	X	X	X	X	X	X
ST WideSurround™ ST OmniSurround™ <sup>(2)</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X

1. Dolby® Digital bypass capability or Virtual Dolby® Digital are obtained with the use of an external Dolby® Digital decoder (for example STD2000)

2. When using Virtual Dolby® Digital or Virtual Dolby® Surround with ST OmniSurround™ or SRS® TruSurround XT™ a Dolby® Digital or a Pro Logic® (or Pro Logic II®) decoder is mandatory respectively

Table 22. STV82x8 version list (TQFP 100)

	S T V 8 2 1 8 F	S T V 8 2 3 8 F	STV8248		STV8258			STV8268		STV8278		STV8288	
			S T V 8 2 4 8 F D	S T V 8 2 4 8 F D S X	S T V 8 2 5 8 F D	S T V 8 2 5 8 F D S X	S T V 8 2 5 8 F S X	S T V 8 2 6 8 F D S X	S T V 8 2 6 8 F D S X	S T V 8 2 7 8 F D S X	S T V 8 2 7 8 F D S X	S T V 8 2 8 8 F D S X	S T V 8 2 8 8 F D S X
<b>Demodulation</b>													
BTSC & DBX noise reduction	X	X	X	X	X	X	X	X	X	X	X	X	X



Table 22. STV82x8 version list (TQFP 100) (continued)

	S T V 8 2 1 8 F	S T V 8 2 3 8 F	STV8248		STV8258			STV8268		STV8278		STV8288	
			S T V 8 2 4 8 F D	S T V 8 2 4 8 F D S X	S T V 8 2 5 8 F D	S T V 8 2 5 8 F D S X	S T V 8 2 5 8 F S X	S T V 8 2 6 8 F D S X	S T V 8 2 7 8 F D S X	S T V 8 2 8 8 F D S X			
<b>Multi-channel capabilities</b>													
Analog loudspeakers output number	2.1	2.1	2.1	2.1	2.1	2.1	2.1	5.1	5.1	5.1	5.1	5.1	5.1
I <sup>2</sup> S In	1	1	1	1	3	3	3	1	1	3	3	3	3
S/PDIF (Pass-thru or Output)	1	1	1	1	1	1	1	1	1	1	1	1	1
2nd SIF input	X	X	X	X	X	X	X	X	X	X	X	X	X
I <sup>2</sup> S Output (always available)	1	1	1	1	1	1	1	1	1	1	1	1	1
Virtual Dolby® Surround			X	X	X	X		X	X	X	X	VDS PLII	VDS PLII
Virtual Dolby® Digital capability <sup>(1)</sup>					X	X	X			X	X	X	X
Dolby® Pro Logic® (DPLI) or Dolby® Pro Logic II® (DPLII) 5.1 output			DPLI (inter nal)	DPLI (inter nal)	DPLI (inter nal)	DPLI (inter nal)		DPL I	DPL I	DPL I	DPL I	DPL II	DPL II
<b>Audio processing</b>													
SRS® WOW™ (WOW)		X											
SRS® TruSurround XT™				X		X	X		X		X		X
ST Voice™, ST Dynamic Bass™	X	X	X	X	X	X	X	X	X	X	X	X	X
ST WideSurround™, ST OmniSurround™ <sup>(2)</sup>	X	X	X	X	X	X	X	X	X	X	X	X	X

1. Dolby® Digital bypass capability or Virtual Dolby® Digital are obtained with the use of an external Dolby® Digital decoder (for example STD2000).

2. When using Virtual Dolby® Digital or Virtual Dolby® Surround with ST OmniSurround™ or SRS® TruSurround XT™ a Dolby® Digital or a Pro Logic® (or Pro Logic II®) decoder is mandatory respectively

## 14.1 STV82x8 overview

### 14.1.1 Core features

- Single audio source processing:
  - IF source and/or analog stereo input (SCART)
  - One digital source with a maximum of 6 synchronous channels (5.1 is obtained across three I<sup>2</sup>S)
- SIF input signal with automatic gain control (AGC)
- BTSC and SAP demodulator, FM mono
- Audio processor working at 48 kHz with specific features:
  - For loudspeakers (L, R, L<sub>S</sub>, R<sub>S</sub>, SubW, C):  
Dolby<sup>®</sup> Pro Logic II<sup>®</sup> speakers (L, R, L<sub>S</sub>, R<sub>S</sub>, SubW, C):  
Dolby<sup>®</sup> decoder with bass management  
SRS<sup>®</sup> WOW<sup>™</sup> or TruSurround XT<sup>™</sup> including Virtual Dolby<sup>®</sup> Surround and Virtual Dolby<sup>®</sup> Digital  
ST WideSurround<sup>™</sup>  
ST OmniSurround<sup>™</sup>  
ST Dynamic Bass<sup>™</sup>  
5-band equalizer or bass / treble controls  
Loudness  
SVC (smart volume control)  
Volume/balance/soft-mute  
Three different types of bips  
Video processing delay compensation
  - For headphones:  
SRS<sup>®</sup> TruBass<sup>™</sup>  
ST Dynamic Bass<sup>™</sup>  
SVC (smart volume control)  
Bass/treble controls  
Loudness  
Volume/balance/soft-mute  
Three different types of bips  
Video processing delay compensation
- Shared outputs for headphone and certain loudspeakers (surround channels);
- Analog matrix with:
  - Five external inputs:  
Four SCART inputs (2 V<sub>RMS</sub> capable)  
One analog mono input (0.5 V<sub>RMS</sub>)
  - One internal input from a digital matrix via a DAC
  - Three external outputs (2 V<sub>RMS</sub> capable)
  - One internal output for the digital matrix (using an internal ADC)
- Digital matrix with:
  - Three input modes (demodulator/SCART, SCART only and I<sup>2</sup>S)
  - Three stereo outputs (loudspeakers, headphone and SCART)
- High-end audio DAC

- S/PDIF output for connection with an external amplifier/decoder
- Internal multiplexer for the S/PDIF output (to share the internal S/PDIF output and the S/PDIF output generated by the external decoder of the digital broadcast)
- Specific stand-by mode (loop-through)
- Control by I<sup>2</sup>C bus (two I<sup>2</sup>C addresses)
- System PLL and clock generation using either a single crystal oscillator or a differential clock input

### 14.1.2 Software information

The different software combinations are listed in [Table 23](#).

**Table 23. Input/Output software configurations**

Input (number of channels)	Output (number of channels)		
	2 (+1)	4 (+1)	5.1
1 (mono)	ST WideSurround™ or SRS® WOW™		
2 (L <sub>O</sub> & R <sub>O</sub> )	ST WideSurround™ or ST OmniSurround™ or SRS® TruSurround XT™ or SRS® WOW™ or Dolby® Pro Logic® II	Dolby® Pro Logic® II	Dolby® Pro Logic® II
2 (L <sub>T</sub> & R <sub>T</sub> )	ST WideSurround™ or ST OmniSurround™ or SRS® TruSurround XT™ or SRS® WOW™ or Dolby® Pro Logic® I or II	Dolby® Pro Logic® I or II	Dolby® Pro Logic® II
4 (+1)	ST OmniSurround™ or SRS® TruSurround XT™	No processing	
5.1	ST OmniSurround™ or SRS® TruSurround XT™	Downmix	No processing

- Note:*
- 1 In addition to the above sound processing, it is always possible to add ST Voice™ and also ST Dynamic Bass™ algorithms.
  - 2 The SRS® TruSurround® and ST OmniSurround™ are approved by Dolby® Labs as Virtual Dolby® Surround (VDS) and Virtual Dolby® Digital (VDD).

The SRS® TruSurround XT™ system is composed of:

- SRS® TruSurround™
- SRS® WOW™
- The SRS® WOW™ system also includes:
  - SRS® Dialog Clarity™
  - SRS® TruBass™
  - SRS® 3D Mono/Stereo™

### 14.1.3 Electrical features

Multi power supplies: 1.8 V, 3.3 V and 8 V.

Power consumption:

- lower than 800mW in functional mode (full features)
- 200 mW in loop-through mode corresponding to the switch-off of all digital blocks

## 14.2 Typical applications

The STV82x8 is specified to enable flexible, analog and digital TV chassis design (refer to [Figure 32](#), [Figure 33](#), [Figure 34](#), and [Figure 35](#)).

The main considerations are:

- all necessary connections between devices can be provided through the TV set,
- pseudo stand-by mode used to copy to VCR or the DVD sources when the TV set is OFF,
- pin compatibility with previous STV82x7 (TQFP80 package) TV design.

The STV82x8 can be used to process dual audio sources (one analog and one digital in parallel).

*Note: Headphone and loudspeakers can be used simultaneously for dual-language purpose. In this case, certain restrictions occur (see [Section 2.2: Audio processing](#)).*

*For more connections, the SCART-to-SCART path can be used. The use of these full analog paths implies that the sound is not digitally processed.*

**Figure 32. STV8238 typical application (enhanced stereo)**

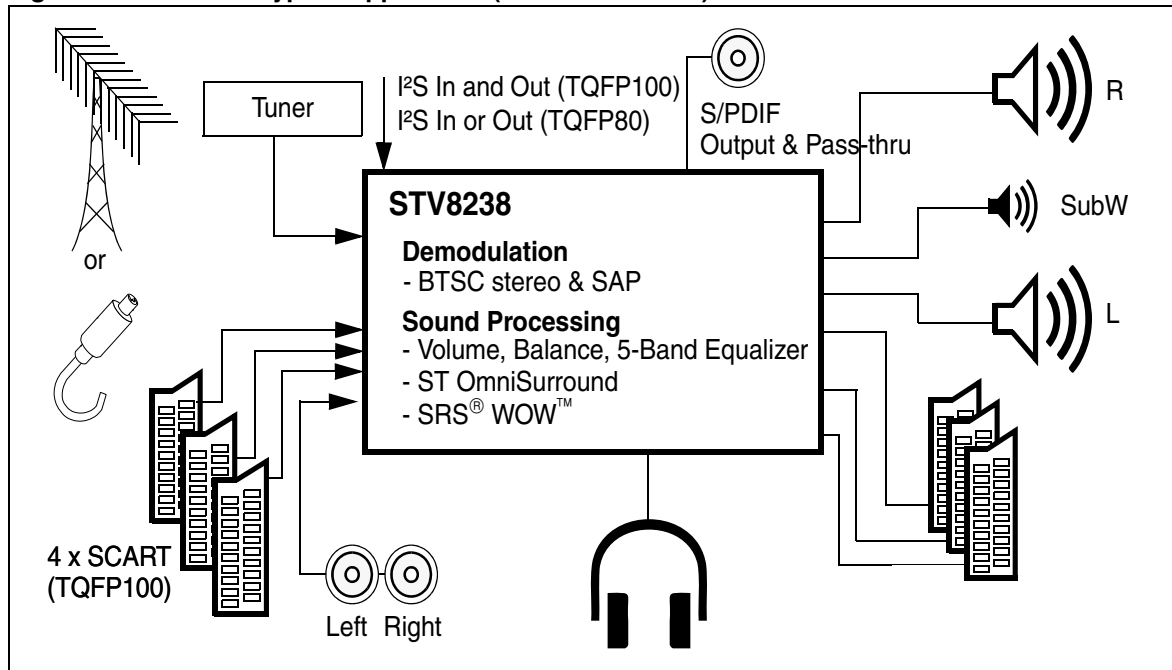


Figure 33. STV8248 typical application (analog virtual sound)

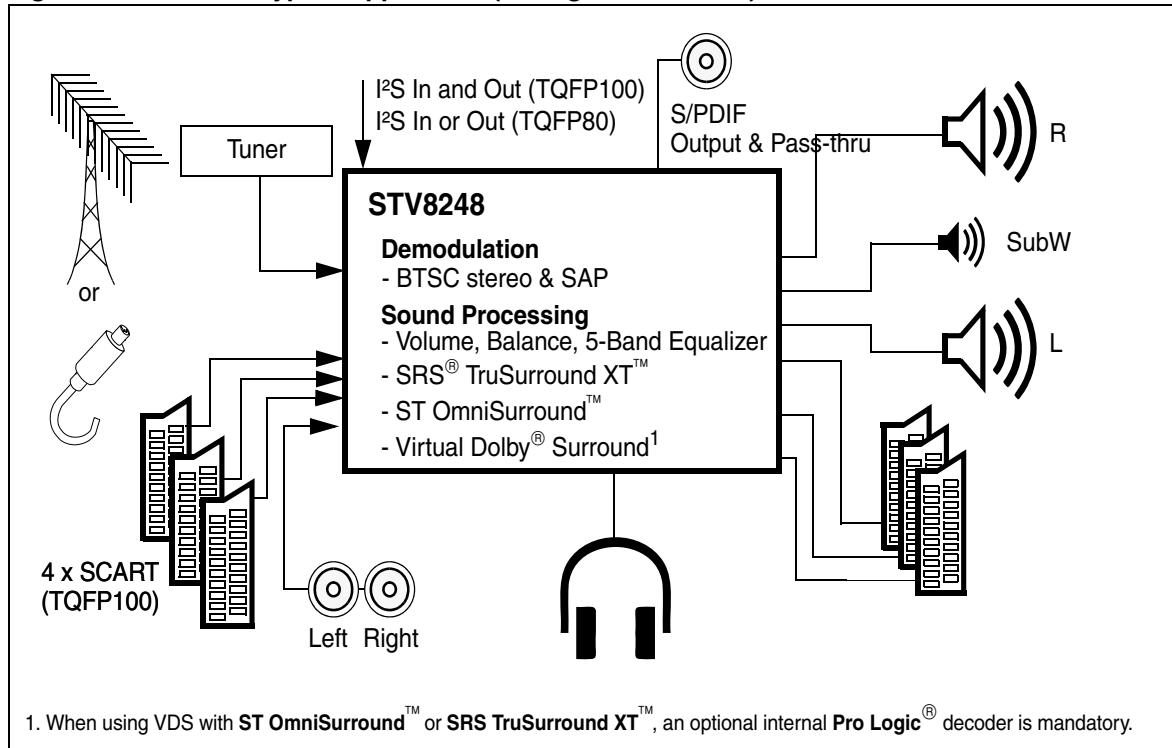


Figure 34. STV8258 typical application (digital virtual sound)

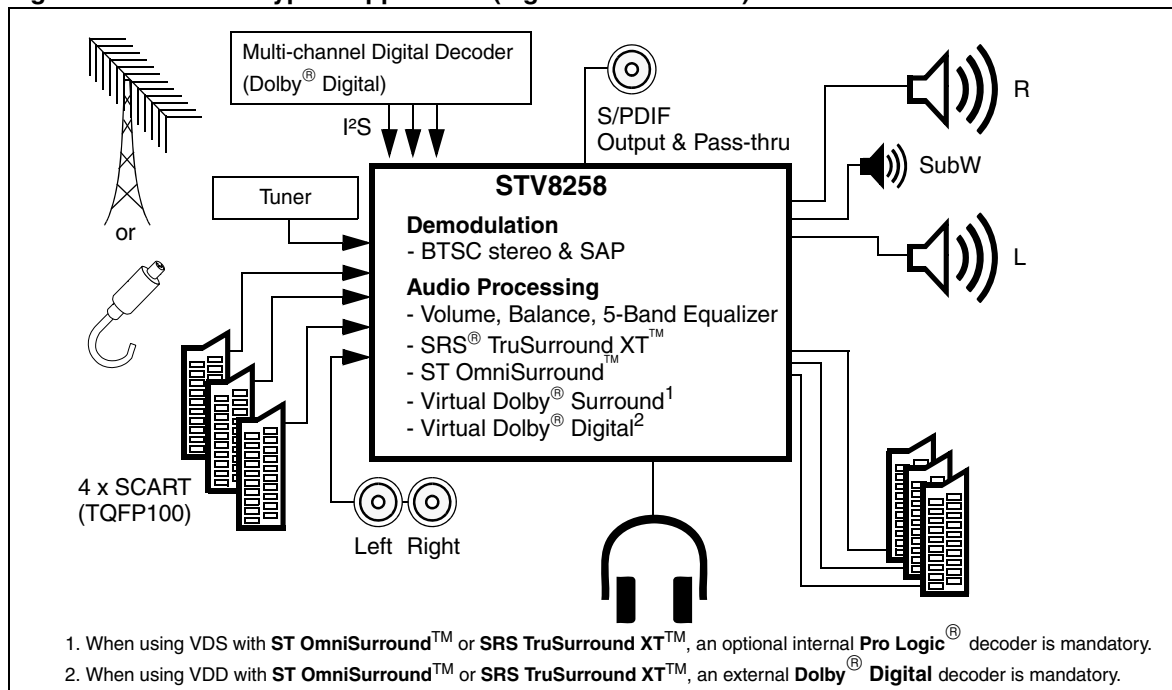


Figure 35. STV8288 typical application (digital TV: multi-channel and virtual sound)

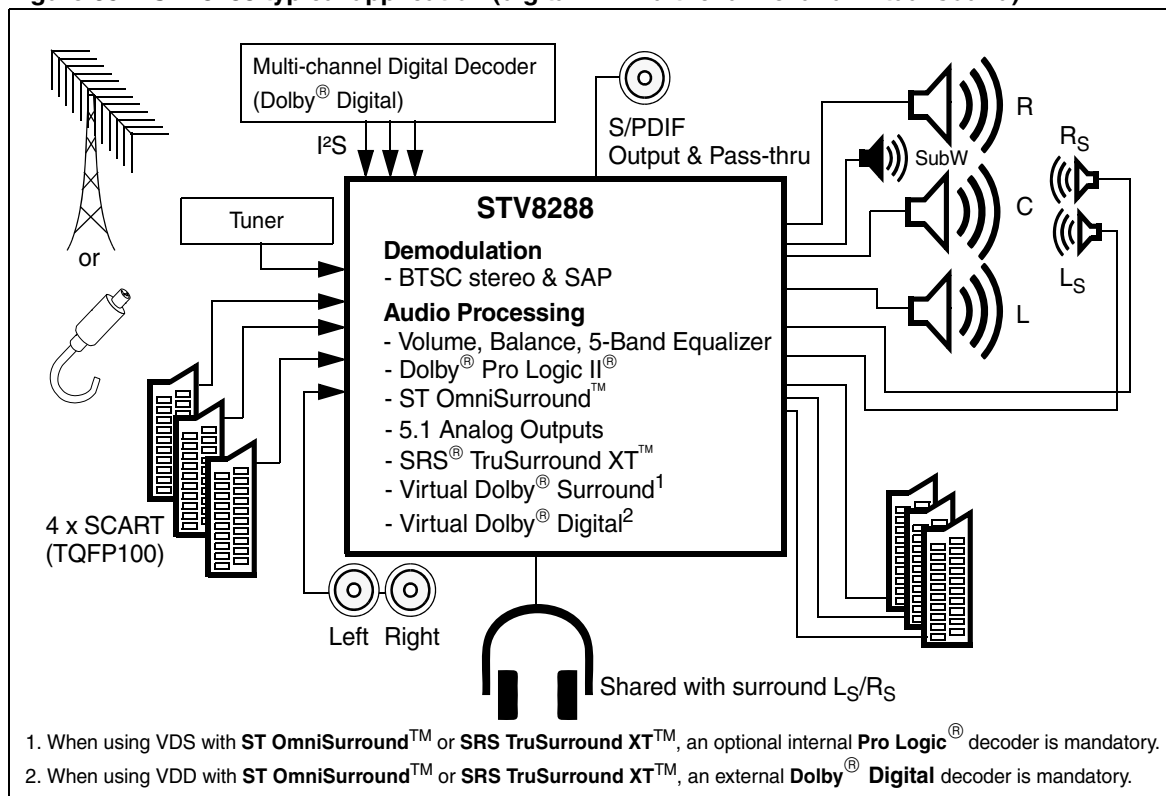
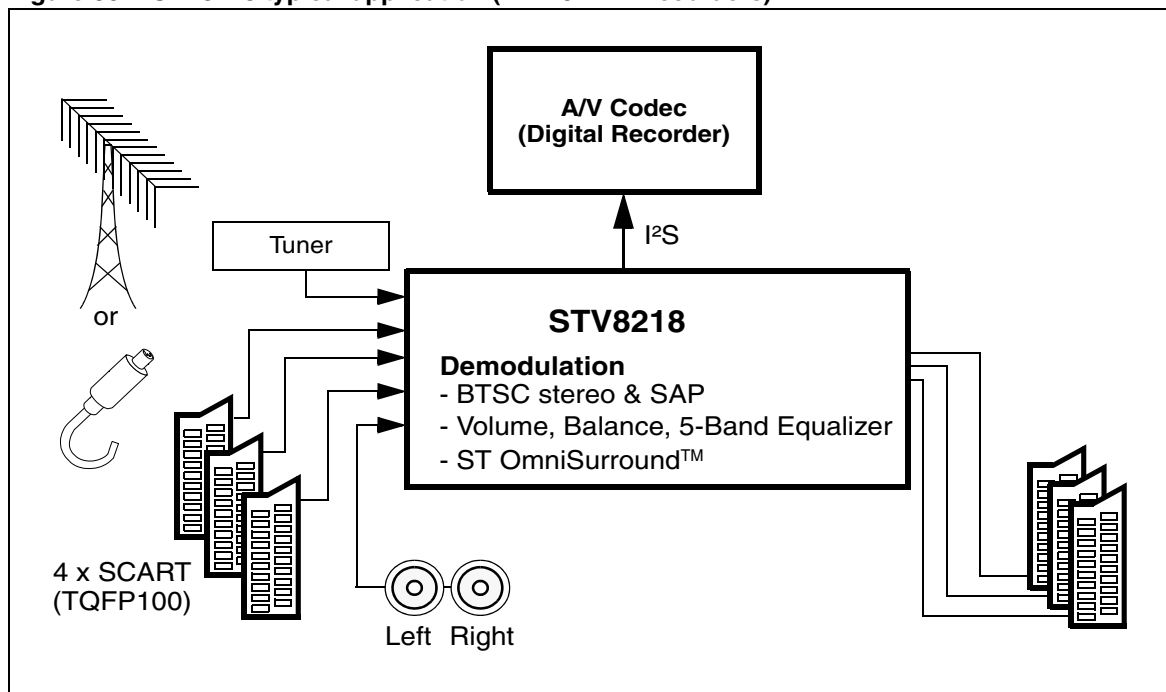


Figure 36. STV8218 typical application (DVD & HDD recorders)



## 15 System clock

The System Clock integrates 2 independent frequency synthesizers.

The first frequency synthesizer is used by the demodulator at a frequency of 24.576 MHz.

The second frequency synthesizer is used by the DSP core and can be adjusted between 100 and 150 MHz depending on the application.

The default values are designed for a standard 27-MHz reference frequency provided by a stable single crystal oscillator or an external differential clock signal (for example, from the STV35x0) depending on the CLK\_SEL pin configuration (CLK\_SEL = 1 means a single crystal oscillator, 0 means an external differential clock).

The 27-MHz value is the recommended frequency for minimizing potential RF interference in the application. The sinusoidal clock frequency, and any harmonic products, remain outside the TV picture and sound IFs (PIF/SIF) and Band-I RF.

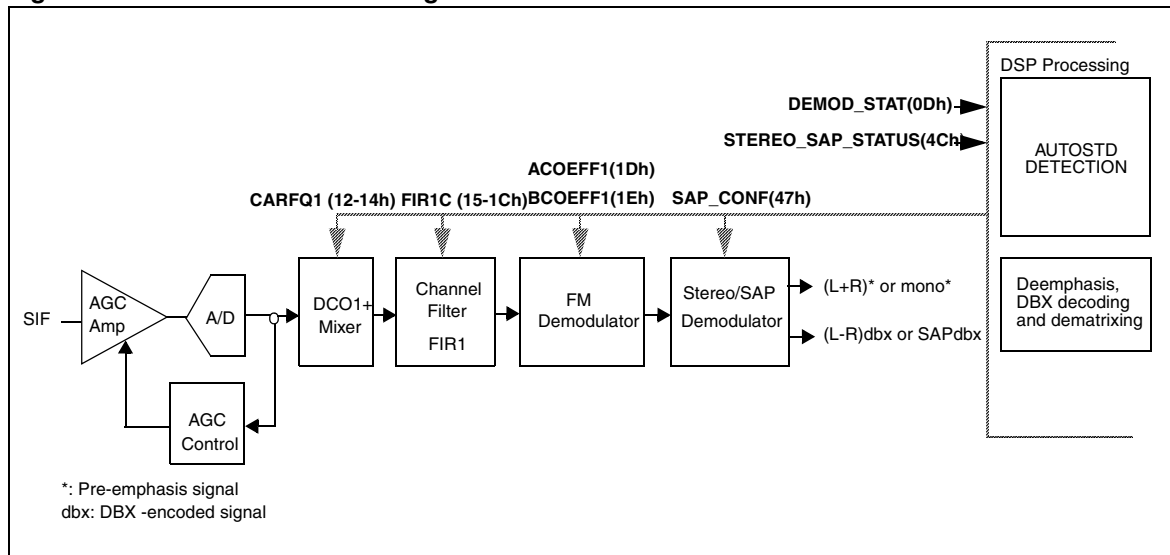
*Note:* A change in the reference frequency is compatible with other default I<sup>2</sup>C programming values, including those of the built-in Automatic Standard Recognition System.

## 16 Digital demodulator

The digital demodulator (see [Figure 37](#)) consists of a channel demodulator and a stereo/SAP decoder.

All channel parameters are programmed automatically by the built-in Automatic Standard Recognition System (Autostandard) in order to find the STEREO or the SAP modes. Channel parameters can also be programmed manually via the I<sup>2</sup>C interface for very specific standards not included among the known standards.

**Figure 37. Demodulator block diagram**



## 16.1 Sound IF signal

The analog sound carrier IF is connected to the STV82x8 via the SIF pin. Before ADC (analog-to-digital conversion), an AGC (automatic gain control) is performed to adjust the incoming IF signal to the full scale of the ADC. A preliminary video rejection is recommended to optimize conversion and demodulation performances. The AGC system provides a gain value allowing for a wide range of SIF input levels.

The TQFP100 package provides a second SIF input.

## 16.2 Demodulation

The demodulation system operates by default in Automatic mode. In this mode, the STV82x8 is able to identify and demodulate the BTSC TV sound standard including stereo and SAP modes without any external control via the I<sup>2</sup>C interface.

The built-in Automatic Standard Recognition System (Autostandard) automatically programs the appropriate bits in the I<sup>2</sup>C registers which are forced to read-only mode for users.

STEREO and SAP modes can be removed (or added) from the List of modes to be recognized by programming registers AUTOSTD\_CTRL. The identified standard is displayed in register [AUTOSTD\\_STATUS](#) and any change to standard is flagged to the host system via pin IRQ. This flag must be reset by re-programming the LSB of register IRQ\_STATUS while checking the detected standard status by reading registers [AUTOSTD\\_STATUS](#).

**Table 24. BTSC Standard**

Source	Modulation	Frequency range	Audio pre-processing	Sub-carrier	Modulation type	Sub-carrier deviation	Aural carrier (4.5 MHz) peak deviation
Mono	L+R	0.05 -15 kHz	75 μs Pre-emphasis				25 kHz (1)
Pilot				Fh*			5 kHz
Stereo	L-R	0.05 -15 kHz	DBX Compression	2 x Fh*	AM DSB SC		50 kHz(1)
SAP	2nd Channel	0.05 -15 kHz	DBX Compression	5 x Fh*	FM	10 kHz	15 kHz

\* Fh = Line Frequency

(1) L+R and L-R must not exceed 50 kHz

**Sound carrier frequency offset recovery:** IF carrier frequency can be adjusted with register [CAROFFSET1](#) within a large range (up to 120 kHz ) while the Automatic Standard Recognition System remains active. The frequency offset estimation is written in registers DEMOD\_DC\_LEVEL and can be used to implement the Automatic Frequency Control (AFC) via an external I<sup>2</sup>C control.

**Manual mode:** If required, the Automatic Standard Recognition System system can be disabled (Manual mode) and the user can control all registers including those only controlled by the Automatic Standard Recognition System function when active. Manual mode is



selected in register AUTOSTD\_CTRL by setting to 0 bits SAP\_CHECK, STEREO\_CHECK and MONO\_CHECK.

## 17 Electrical characteristics

Test conditions:  $T_{\text{OPER}} = 25^{\circ}\text{C}$ ,  $V_{\text{CC}_H} = 8\text{V}$ ,  $V_{\text{XX}_{18}} = 1.8\text{V}$ ,  $V_{\text{XX}_{33}} = 3.3\text{V}$ , crystal oscillator at 27 MHz, default register values for synthesizer, unless otherwise specified

### 17.1 Absolute maximum ratings

Symbol	Parameter	Value	Units
$V_{\text{XX}_{18}}$	Analog and digital 1.8 V supply voltage ( $V_{\text{CC}_{18\_CLK1}}$ , $V_{\text{CC}_{18\_CLK2}}$ , $V_{\text{CC}_{18\_IF}}$ , $V_{\text{DD}_{18}}$ , $V_{\text{DD}_{18\_CONV}}$ , $V_{\text{DD}_{18\_ADC}}$ )	2.5	V
$V_{\text{XX}_{33}}$	Analog and digital 3.3 V supply voltage ( $V_{\text{CC}_{33\_SC}}$ , $V_{\text{CC}_{33\_LS}}$ , $V_{\text{DD}_{33\_IO1}}$ , $V_{\text{DD}_{33\_IO2}}$ , $V_{\text{DD}_{33\_CONV}}$ , $V_{\text{CC}_{NISO}}$ )	4.0	V
$HV_{\text{CC}}$	Analog supply high voltage ( $V_{\text{CC}_H}$ )	8.8	V
$V_{\text{ESD}}$	Capacitor 100 pF discharged via 1.5 k $\Omega$ serial resistor (human body model)	4	kV
$T_{\text{OPER}}$	Operating ambient temperature	0, +70	$^{\circ}\text{C}$
$T_{\text{STG}}$	Storage temperature	-55 to +150	$^{\circ}\text{C}$

### 17.2 Thermal data

Symbol	Parameter	Value	Units
$R_{\text{thJA}}$	Junction-to-ambient thermal resistance	42	$^{\circ}\text{C}/\text{W}$

### 17.3 Power supply data

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{\text{XX}_{18}}$	Analog and digital 1.8 V supply voltage ( $V_{\text{CC}_{18\_CLK1}}$ , $V_{\text{CC}_{18\_CLK2}}$ , $V_{\text{CC}_{18\_IF}}$ , $V_{\text{DD}_{18}}$ , $V_{\text{DD}_{18\_CONV}}$ , $V_{\text{DD}_{18\_ADC}}$ )	1.70	1.80	1.90	V
$V_{\text{XX}_{33}}$	Analog and digital 3.3 V supply voltage ( $V_{\text{CC}_{33\_SC}}$ , $V_{\text{CC}_{33\_LS}}$ , $V_{\text{DD}_{33\_IO1}}$ , $V_{\text{DD}_{33\_IO2}}$ , $V_{\text{DD}_{33\_CONV}}$ , $V_{\text{CC}_{NISO}}$ )	3.13	3.30	3.47	V
$HV_{\text{CC}}$	Analog supply high voltage ( $V_{\text{CC}_H}$ )	7.6	8.0	8.4	V
$I_{\text{VDD}_{18}}$	Current consumption for digital 1.8 V supply ( $V_{\text{CC}_{18\_CLK2}}$ , $V_{\text{DD}_{18}}$ , $V_{\text{DD}_{18\_CONV}}$ , $V_{\text{DD}_{18\_ADC}}$ )		210		mA
$I_{\text{VDD}_{33}}$	Current consumption for digital 3.3 V supply ( $V_{\text{DD}_{33\_IO1}}$ , $V_{\text{DD}_{33\_IO2}}$ )		10		mA
$I_{\text{VCC}_{18}}$	Current consumption for analog 1.8 V supply ( $V_{\text{CC}_{18\_CLK1}}$ , $V_{\text{CC}_{18\_IF}}$ )		50		mA
$I_{\text{VCC}_{33}}$	Current consumption for analog 3.3 V supply ( $V_{\text{CC}_{33\_SC}}$ , $V_{\text{CC}_{33\_LS}}$ , $V_{\text{DD}_{33\_CONV}}$ , $V_{\text{CC}_{NISO}}$ )		70		mA

Symbol	Parameter	Min.	Typ.	Max.	Units
$I_{VCC\_H}$	Current consumption for analog supply high voltage (8 V)		4		mA
$P_{DTOT}$	Total power dissipation		760		mW

## 17.4 Crystal oscillator

Symbol	Parameter	Min.	Typ.	Max.	Units
$f_P$	Crystal series resonance frequency (at $C_{21} = C_{22} = 27$ pF load capacitor)		27		MHz
$DF/F_P$	Frequency tolerance at 25 °C	-30		+30	ppm
$DF/F_T$	Frequency stability versus temperature within a range from 0 to 70 °C	-30		+30	ppm
$C_1$	Motional capacitor			15	fF
$R_S$	Serial resistance			30	W
$C_S$	Shunt capacitance			7	pF

## 17.5 Analog sound IF signal

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
$BAND_{SIF}$	SIF frequency flatness	AGC_ERR at 0, frequency range from 4 to 7MHz		0.6	3	dB
$R_{INSIF}$	SIF input resistance		60	72	85	k $\Omega$
$DC_{INSIF}$	SIFinput DC level			0.9		V
$C_{INSIF}$	SIF input capacitance			3		pF
<b>FM carrier</b>						
$VSIF_{FM}$	SIF input sensitivity	SNR 40 dB RMS unweighted 20 Hz to 15 kHz Standard M/N 27 kHz FM Deviation 1 kHz	350			$\mu V_{PP}$
<b>AGC</b>						
$AGC_{step}$	IF AGC step		1.4	1.5	1.6	dB
$AGC_{dyn}$	Relative maximum gain to step 0	Valid from step 21 to step 31	29	30	31	dB

## 17.6 SIF to I<sup>2</sup>S output path characteristics

Test conditions: SIF amplitude = 100 mVpp, unless otherwise specified, I<sup>2</sup>S output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
<b>FM Demodulation</b>						
BAND <sub>FM</sub>	Frequency response	20 Hz to 14 kHz			±1	dB
SNR <sub>FM</sub>	Signal to noise	RMS unweighted, 20 Hz to 15 kHz, Standard M/N 27 kHz FM Deviation, 1 kHz	66			dB
THD <sub>FM</sub>	Total harmonic distortion				0.05	%
SEP <sub>FM</sub>	Stereo channel separation	Standard M/N BTSC stereo, FM deviation, 1 kHz	30			dB

## 17.7 SCART to SCART analog path characteristics

Test conditions: Rload<sub>MAX</sub> = 10 kΩ, Cload<sub>MAX</sub> = 330 pF, MONO\_IN voltage = 0.5 V<sub>RMS</sub>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units	
<b>Analog-to-analog STEREO and MONO</b>							
R <sub>INSCART</sub>	SCART Input Resistance			34		kΩ	
R <sub>OUTSCART</sub>	Output Resistance for SCARTs			40		W	
VDC <sub>INSCART</sub>	SCART Input DC Level			1.57		V	
VDC <sub>OUTSCART</sub>	SCART Output DC Level			3.64		V	
CLIP <sub>SCART</sub>	Clipping SCART	Clipping input level from SCART input	At 1 kHz 1% THD	2		V <sub>RMS</sub>	
		Clipping input level from MONO_IN input		0.5		V <sub>RMS</sub>	
THD <sub>SCART</sub>	THD SCART	THD from SCART input	1 V <sub>RMS</sub> , at 1 KHz		0.02	0.05	%
		THD from MONO_IN input	0.25 V <sub>RMS</sub> , at 1 KHz		0.02	0.05	%
SNR <sub>SCART</sub>	Signal to Noise Ratio	SCART input	1 V <sub>RMS</sub> , 20 Hz to 20 kHz Bandwidth, RMS unweighted		82		dB
		MONO_IN input	0.25 V <sub>RMS</sub> , 20 Hz to 20 kHz Bandwidth, RMS unweighted		76		dB
BAND <sub>SCART</sub>	Frequency Flatness	SCART input	20 Hz to 20 kHz	-0.5	0	0.5	dB
		MONO_IN input	20 Hz to 20 kHz	11.5	12	12.5	dB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
XTALK <sub>L/R</sub>	Left/Right crosstalk	1 V <sub>RMS</sub> @ 1 kHz on ref signal, the other one grounded	80	90		dB
XTALK <sub>IN</sub>	Audio crosstalk from input channel <i>n</i> to input channel <i>m</i>	1 V <sub>RMS</sub> @ 1 kHz on ref signal, all other inputs grounded	80	90		dB
XTALK <sub>OUT</sub>	Audio crosstalk from output channel <i>n</i> to output channel <i>m</i>	1 V <sub>RMS</sub> @ 1 kHz on reference output, signal on a single input, all other inputs grounded	80	90		dB

## 17.8 SCART and MONO IN to I<sup>2</sup>S path characteristics

Test conditions: sampling frequency = 48 kHz, maximum MONO\_IN voltage = 0.5 V<sub>RMS</sub>

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
THD <sub>ADC</sub>	THD ADC	THD from SCART input V <sub>IN</sub> = 2 V <sub>RMS</sub> at 1 KHz		0.006	0.05	%
		THD from MONO_IN input V <sub>IN</sub> = 0.5 V <sub>RMS</sub> at 1 KHz		0.006	0.05	%
SNR <sub>ADC</sub>	Signal to noise ratio	20 to 15 kHz bandwidth, RMS unweighted V <sub>IN</sub> = 200 mV <sub>RMS</sub> SCART input	62			dB
BAND <sub>ADC</sub>	Frequency flatness	20 Hz to 15 kHz			±0.5	dB
XTALK <sub>ADC</sub>	Left/Right crosstalk	at 1 KHz, V <sub>IN</sub> = 1 V <sub>RMS</sub>	95			dB

## 17.9 I<sup>2</sup>S to LS/HP/SUB/C path characteristics

Test conditions: sampling frequency = 48KHz, L<sub>LOAD</sub> = 100 μH, C<sub>LOAD</sub> = 33nF, R<sub>LOAD</sub> = 30KΩ

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R <sub>OUTDAC</sub>	Output resistance for main outputs	LS_L, LS_R, LS_SUB, LS_C, HP_LSS_R and HP_LSS_L pins		90	140	W
VDC <sub>OUTDAC</sub>	MAIN output DC level			1.54		V
THD <sub>DAC</sub>	Total harmonic distortion	90% full-scale range at 1 kHz			0.06	%
SNR <sub>DAC</sub>	Signal to noise ratio	20 to 15 kHz bandwidth, RMS unweighted, at -20dB full range	75			dB
V <sub>OUTAMPDA C</sub>	MAIN output amplitude	100% full-scale range at 1 kHz		900		mV <sub>RMS</sub>
XTALK <sub>DAC</sub>	Left/Right cCrosstalk	at 1 KHz, -20dBFS	87			dB

## 17.10 I<sup>2</sup>S to SCART path characteristics

Test conditions: sampling frequency = 48 kHz, C<sub>LOAD</sub> = 33 nF on DAC SCART pins, DAC SCART prescale at -5.5 dB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
THD <sub>DACSCART</sub>	Total harmonic distortion	50% full-scale range at 1 kHz		0.08	0.2	%
SNR <sub>DACSCART</sub>	Signal to noise ratio	20 Hz to 15 kHz bandwidth unweighted, -20dB full range	73			dB
V <sub>ODACSCART</sub>	MAIN output amplitude	100% full-scale range at 1 kHz		2		V <sub>RMS</sub>
XTALK <sub>DACSCART</sub>	Left/Right crosstalk	at 1 KHz, -20 dBFS	80			dB

## 17.11 MUTE characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
MUTE <sub>DAC</sub>	DAC mute analog	I <sup>2</sup> S to DAC at 1 kHz	90			dB
MUTE <sub>SCART</sub>	SCART mute	2 V <sub>RMS</sub> @ 1 kHz on ref signal, all other inputs grounded	81			dB

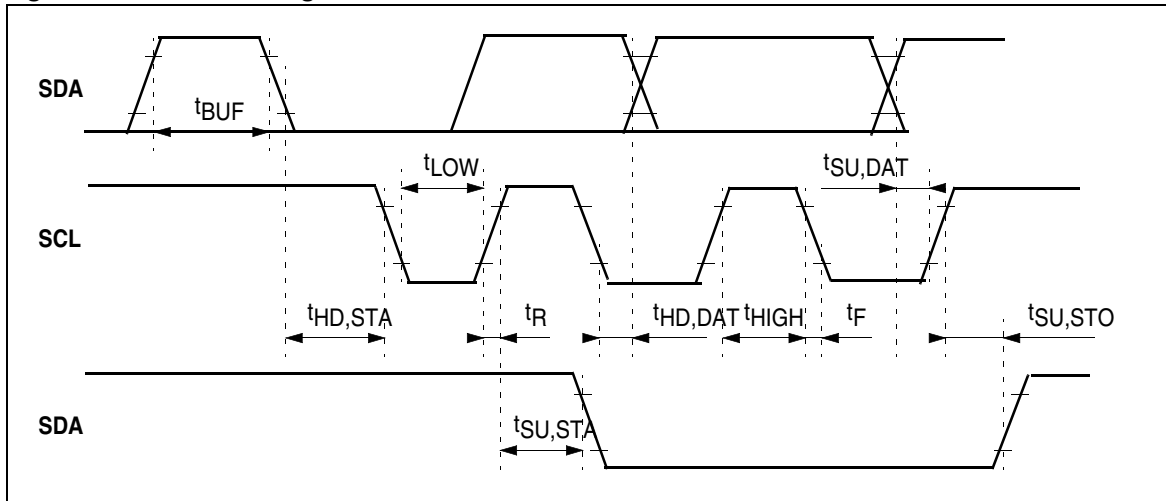
## 17.12 Digital I/Os characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
V <sub>IL</sub>	Low level input voltage	Except SDA, SCL and CLK_SEL, 3.3V power supply			0.5	V
V <sub>IH</sub>	High level input voltage	Except SDA, SCL and CLK_SEL, 3.3V power supply	2.0			V
I <sub>IN</sub>	Input current				1	μA
V <sub>ILCLK_SEL</sub>	CLK_SEL low level input voltage	1.8V power supply			0.3	V
V <sub>IHCLK_SEL</sub>	CLK_SEL high level input voltage	1.8V power supply	1.2			V
V <sub>OL</sub>	Low level output voltage	S/PDIF_OUT, IRQ, BUS_EXP			0.3	V
V <sub>OH</sub>	High level output voltage	S/PDIF_OUT, IRQ, BUS_EXP	3.0			V

## 17.13 I<sup>2</sup>C bus characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Unit
<b>SCL</b>						
V <sub>IL</sub>	Low level input voltage		-0.3		1.5	V
V <sub>IH</sub>	High level input voltage		2.3		5.5	V
I <sub>IL</sub>	Input leakage current	V <sub>IN</sub> = 0 to 5.0 V	-10		10	μA
f <sub>SCL</sub>	Clock frequency				400	kHz
t <sub>R</sub>	Input rise time	1 V to 2 V			300	ns
t <sub>F</sub>	Input fall time	2 V to 1 V			300	ns
C <sub>I</sub>	Input capacitance				10	pF
<b>SDA</b>						
V <sub>IL</sub>	Low level input voltage		-0.3		1.5	V
V <sub>IH</sub>	High level input voltage		2.3		5.5	V
I <sub>IL</sub>	Input leakage current	V <sub>IN</sub> = 0 to 5.0 V	-10		10	μA
t <sub>R</sub>	Input rise time	1 V to 2 V			300	ns
t <sub>F</sub>	Input fall time	2 V to 1 V			300	ns
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 3 mA			0.4	V
t <sub>F</sub>	Output fall time	2 V to 1 V			250	ns
C <sub>L</sub>	Load capacitance				400	pF
C <sub>I</sub>	Input capacitance				10	pF
<b>I<sup>2</sup>C Timing</b>						
t <sub>LOW</sub>	Clock low period		1.3			μs
t <sub>HIGH</sub>	Clock high period		0.6			μs
t <sub>SU,DAT</sub>	Data set-up time		100			ns
t <sub>HD,DAT</sub>	Data hold time		0		900	ns
t <sub>SU,STO</sub>	Set-up time from clock high to stop		0.6			μs
t <sub>BUF</sub>	Start set-up time following a stop		1.3			μs
t <sub>HD,STA</sub>	Start hold time		0.6			μs
t <sub>SU,STA</sub>	Start set-up time following clock low to high transition		0.6			μs

Figure 38. I<sup>2</sup>C bus timing



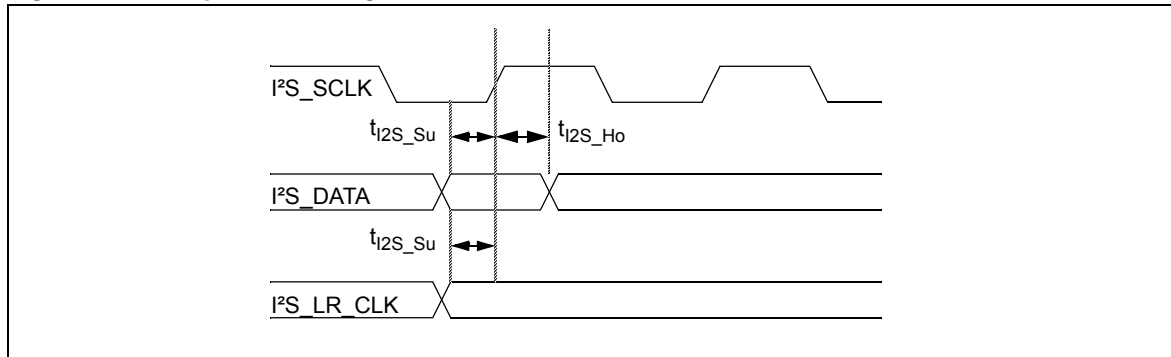
### 17.14 I<sup>2</sup>S bus interface

I<sup>2</sup>S Bus Interface timing values shown in [Figure 39](#).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>I<sup>2</sup>S Input</b>						
$V_{I2S\_IL}$	Input I <sup>2</sup> S low level voltage				0.8	V
$V_{I2S\_IH}$	Input I <sup>2</sup> S high level voltage		2			V
$Z_{I2S}$	Input I <sup>2</sup> S impedance				5	pF
$I_{I2S\_Leak}$	I <sup>2</sup> S leakage current		-1		1	μA
$t_{I2S\_Su}$	I <sup>2</sup> S input setup time before rising edge of clock	See <a href="#">Figure 39</a>	30			ns
$t_{I2S\_Ho}$	I <sup>2</sup> S input hold time after rising edge of clock	See <a href="#">Figure 39</a>	100			ns
$f_{I2S\_LR0}$	I <sup>2</sup> S left/right strobe input frequency (I <sup>2</sup> S_DATA0 with SRC)		30		49	kHz
$f_{I2S\_SCL0}$	I <sup>2</sup> S serial clock input frequency (I <sup>2</sup> S_DATA0 with SRC)		1.092		3.136	MHz
$f_{I2S\_LR}$	I <sup>2</sup> S left/right strobe input frequency (I <sup>2</sup> S_DATA0 with PLL, I <sup>2</sup> S_DATA1,2)	Deviation = ±250 ppm		48		kHz
$f_{I2S\_SCL}$	I <sup>2</sup> S serial clock input frequency (I <sup>2</sup> S_DATA0 with PLL, I <sup>2</sup> S_DATA1,2)			3.072		MHz
$R_{I2S\_SCL}$	I <sup>2</sup> S serial clock input ratio		0.9		1.1	



Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>I<sup>2</sup>S Output (I<sup>2</sup>S_DATA0 only)</b>						
V <sub>I2SOL</sub>	Output I <sup>2</sup> S low level voltage	I <sub>OL</sub> = 2 mA			0.4	V
V <sub>I2SOH</sub>	Output I <sup>2</sup> S high level voltage	I <sub>OH</sub> = 2 mA	2.4			V
f <sub>I2S_OLR</sub>	I <sup>2</sup> S left/right strobe output frequency (I <sup>2</sup> S_DATA0 and I <sup>2</sup> SO_DATA0,1)			48		kHz
f <sub>I2S_OSCL</sub>	I <sup>2</sup> S serial clock output frequency (I <sup>2</sup> S_DATA0 and I <sup>2</sup> SO_DATA0,1)			3.072		MHz
R <sub>I2S_SCL</sub>	I <sup>2</sup> S serial clock output ratio		0.9		1.1	
t <sub>I2S_DEL</sub>	I <sup>2</sup> S output delay after falling edge of clock	See <a href="#">Figure 39</a> , C <sub>I</sub> = 30 pF			30	ns

**Figure 39. IS input bus timings**

# 18 Package mechanical data

## 18.1 TQFP80 package

Figure 40. 80-pin thin plastic flat package

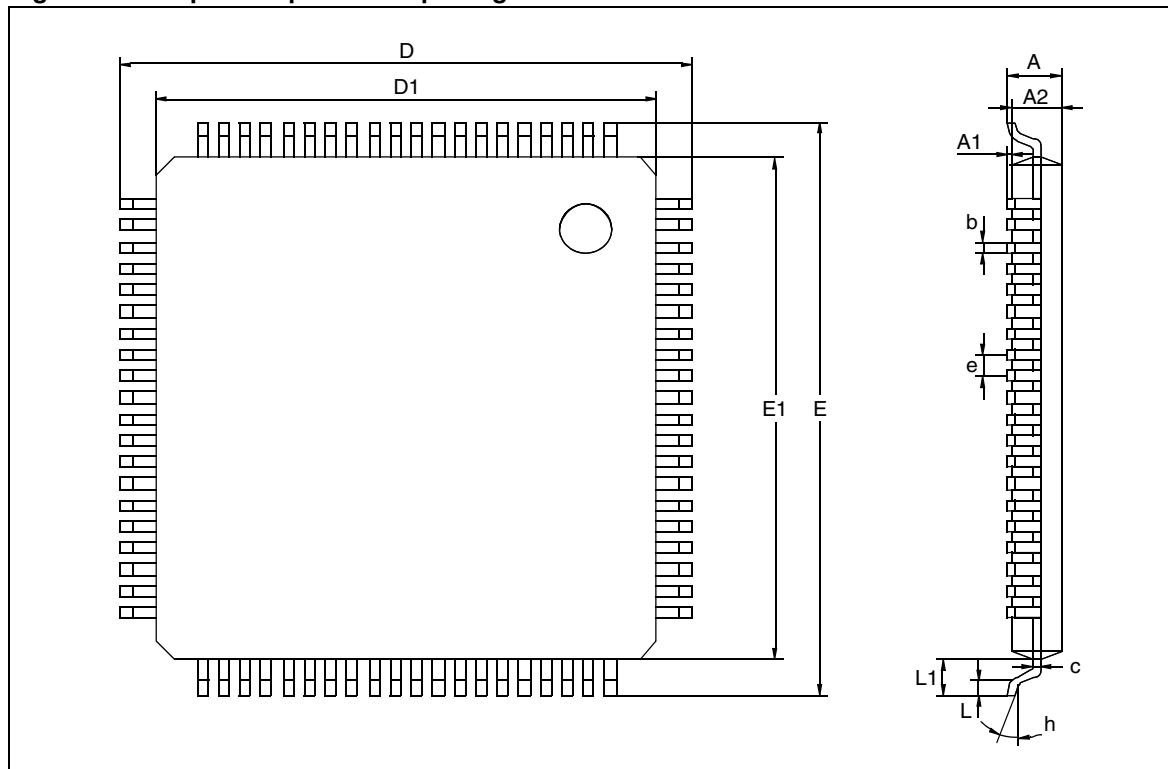


Table 25. Package mechanical dimensions

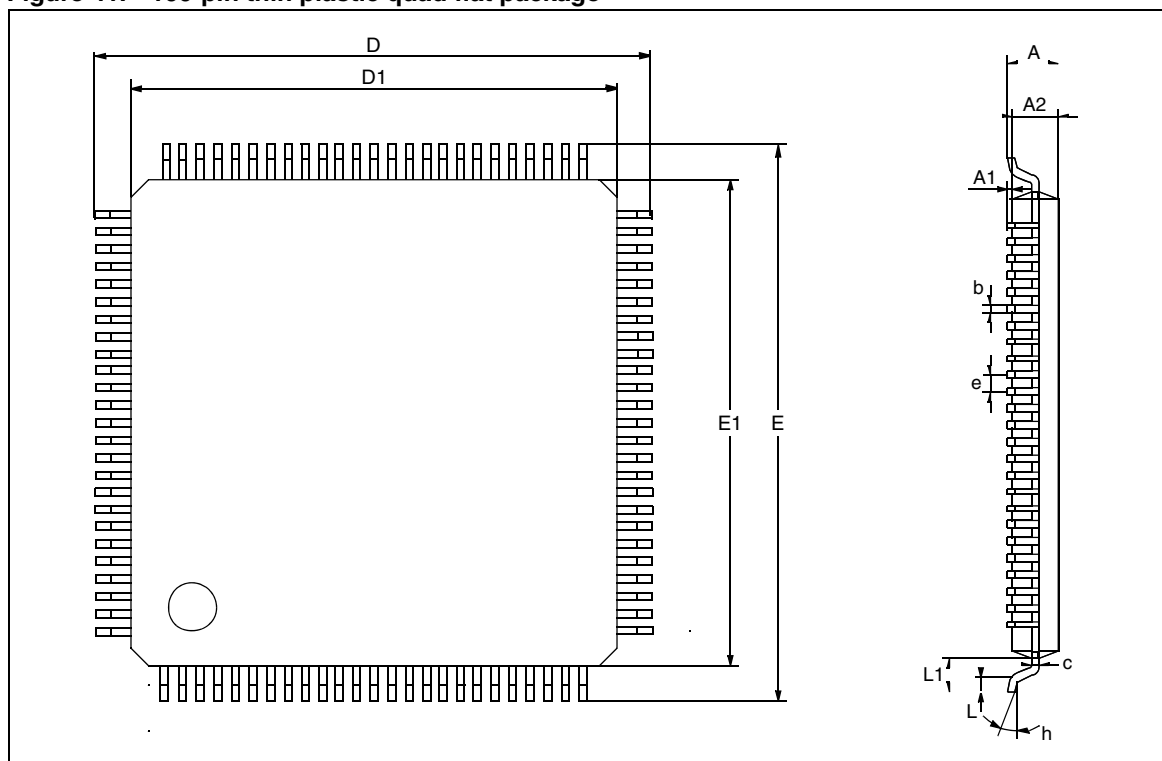
Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.65			0.026	

Table 25. Package mechanical dimensions (continued)

K	0°	3.5°	0.75°	0°	3.5°	0.75°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
e		0.65			0.026	
K	0°	3.5°	0.75°	0°	3.5°	0.75°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	

## 18.2 TQFP100 package

Figure 41. 100-pin thin plastic quad flat package



Package mechanical dimensions

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057

## Package mechanical dimensions (continued)

<b>b</b>	0.17	0.22	0.27	0.007	0.009	0.011
<b>C</b>	0.09		0.20	0.004		0.008
<b>D</b>		16.00			0.630	
<b>D1</b>		14.00			0.551	
<b>E</b>		16.00			0.630	
<b>E1</b>		14.00			0.551	
<b>e</b>		0.50			0.020	
$\theta$	0°	3.5°	7°	0°	3.5°	7°
<b>L</b>	0.45	0.60	0.75	0.018	0.024	0.030
<b>L1</b>		1.00			0.039	
	Number of Pins					
<b>N</b>	100					

### 18.3 Environmentally-friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 19 Order information

**Table 26. Order codes**

Part number	Package	Conditioning
STV82x8	TQFP80	Tray
STV82x8/T	TQFP80	Tape & reel
STV82x8F	TQFP100	Tray
STV82x8F/T	TQFP100	Tape & reel

*Note:* For example: *STV8258DSX/T* will be delivered in a *TQFP80* package with *tape & reel* conditioning

## 20 Revision history

**Table 27. Document revision history**

Date	Revision	Changes
15-Nov-2004	0.1	Initial release.
19-Nov-2004	0.2	Major updates to <i>Features</i> , and <i>General description</i>
07-Jan-2005	0.3	Addition of TQFP100 information
23-Feb-2005	1.0	Updated <i>Figure 1: STV82x8 block diagram (TQFP80)</i> , <i>Figure 2: STV82x8 block diagram (TQFP100)</i> , <i>Section 17.5: Analog sound IF signal</i> and <i>Section 17.6: SIF to I<sup>2</sup>S output path characteristics</i>
01-Jun-2006	1.1	Reordering of chapters
31-Mar-2009	2	Preliminary banner removed, <i>Section 18.3: Environmentally-friendly packages</i> added

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