

DISCONTINUED

SED1601

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- 80-bit High Voltage Resistant Output
- 1/100 to 1/300 In Display Duty
- CMOS High Voltage Resistant Process

DESCRIPTION

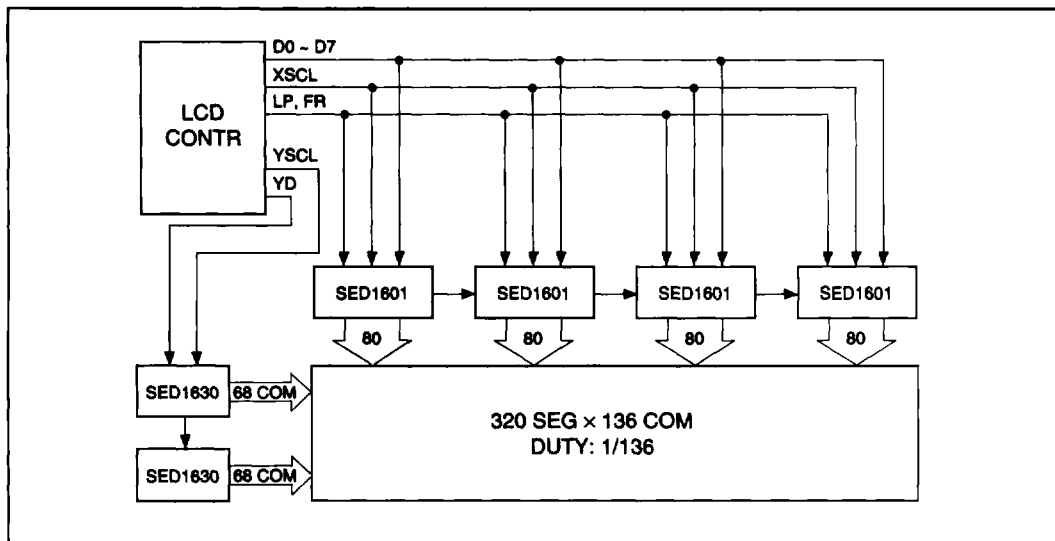
The SED1601 is an 80-output dot matrix LCD segment (column) driver for driving a high-capacity LCD panel at duty cycles higher than 1/100 (up to 1/300). The LSI has a wide range of the LCD driving voltages. Due to the architecture of the SED1601, the LCD driving voltage, V_0 , is isolated from V_{DD} supply. This provides the ability to adjust the offset bias independently of V_{DD} . These unique features allow the SED1601 to interface with a variety of LCD panels. The SED1601 does not require a controller to output an enable signal to implement daisy chain technology. This provides for easy interfacing with LCD controllers such as the SED1330, SED1351, SED1335 or the SED1341.

The SED1601 is used in conjunction with the SED1610 (86 row driver) or the SED1630 (68-bit row driver) and SED1631 (100 row driver) or the SED1632 (86-bit row driver), SED1633 (100-bit row driver) and SED1634 (100-bit row driver) to drive a large-capacity dot matrix LCD panel.

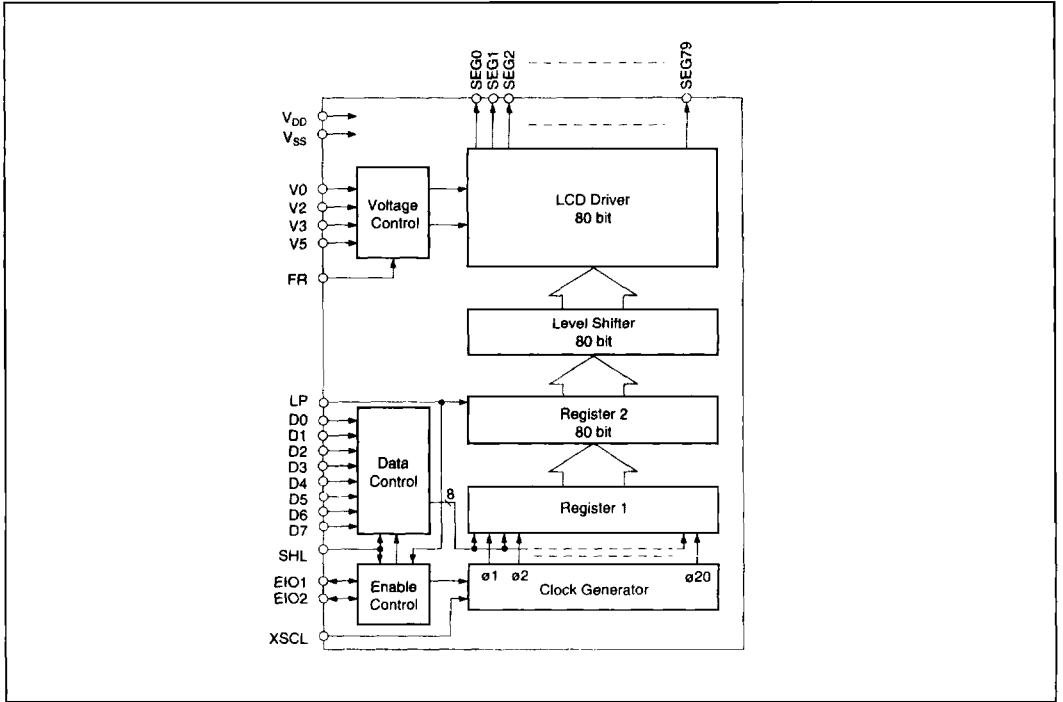
FEATURES

- Low-power CMOS technology
- 80-bit segment (column) driver
- High-speed 8-bit bus
- Duty cycle 1/100 to 1/300
- Output shift direction pin selectable
- Shift clock frequency 6.5MHz max
- Ability to adjust offset bias of the LCD source from V_{DD}
- Daisy chain enable support
- No enable signal by controller is required
- Wide range of LCD voltage -12V to -28V
- Supply voltage 5.0V \pm 10%
- Package QFP5-100 pin (FAA)
DIE: Al pad chip (DAA)

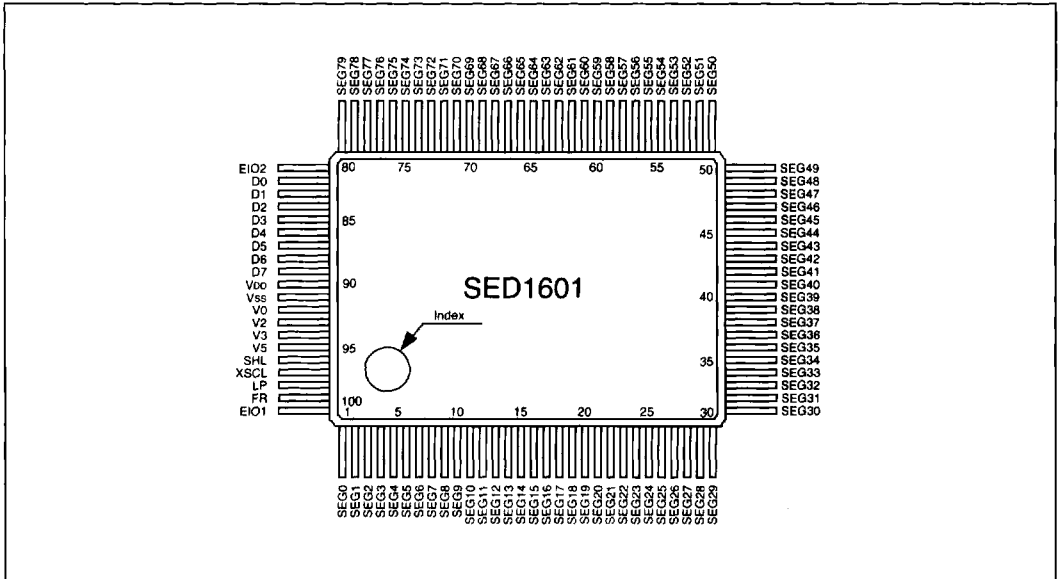
SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTION

Pin Name	I/O	Function																																																																
SEG0 to SEG79	O	LCD driving segment (column) outputs. Each output changes at the falling edge of LP.																																																																
D0 TO D7	I	Display data inputs.																																																																
XSCL	I	Shift clock of display data (falling edge trigger).																																																																
LP	I	Latch pulse of display data (falling edge trigger).																																																																
EI01, EI02	I/O	Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 80 bits of data are taken in.																																																																
SHL	I	Shift direction selection and EIO pin I/O control. When data (a, b, c, d, e, f, g, h) (i, j, k, l, m, n, o, p).....(s, t, u, v, w, x, y, z) are input to pins (D7, D6, D5, D4, D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="14">SEG</th> <th colspan="2">EIO</th> </tr> <tr> <th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>74</th><th>73</th><th>72</th><th>.....</th><th>3</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>.....</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td> </tr> <tr> <td>H</td> <td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>.....</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td> </tr> </tbody> </table>	SHL	SEG														EIO		79	78	77	76	75	74	73	72	3	2	1	0	1	2	L	a	b	c	d	e	f	g	h	w	x	y	z	Output	Input	H	z	y	x	w	v	u	t	s	d	c	b	a	Input	Output
SHL	SEG														EIO																																																			
	79	78	77	76	75	74	73	72	3	2	1	0	1	2																																																			
L	a	b	c	d	e	f	g	h	w	x	y	z	Output	Input																																																			
H	z	y	x	w	v	u	t	s	d	c	b	a	Input	Output																																																			
FR	I	AC signal of LCD driving outputs.																																																																
V _{DD} , V _{SS}	Power Supplies	Logic circuit power. V _{DD} : 0 V (GND) V _{SS} : -5.0 V																																																																
V ₀ , V ₂ , V ₃ , V ₅	Power Supplies	LCD driving power. V ₅ : -12 to -28 V V _{DD} ≥ V ₀ ≥ V ₂ > V ₃ ≥ V ₅																																																																

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{SS}	-7.0 to +0.3	V
Supply voltage (2)	V ₅	-30.0 to +0.3	V
Supply voltage (2)	V ₀ , V ₂ , V ₃ *	V ₅ -0.3 to +0.3	V
Input voltage (1)	V _I	V _{SS} -0.3 to +0.3	V
Output voltage (1)	V _O	V _{SS} -0.3 to +0.3	V
Output current (1)	I _O	20	mA
Output current (2)	I _O SEG	20	mA
Allowable power dissipation	P _D	300	mW
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-65 to +150	°C
Soldering temperature, time	T _{sol}	260°C, 10 s (at lead)	—

* V₀, V₂ and V₃ must always satisfy the condition: V_{DD} ≥ V₀ ≥ V₂ ≥ V₃ ≥ V₅.

● DC Electrical Characteristics

(Unless otherwise specified, $V_{DD} = V_0 = 0V$,
 $V_{SS} = -5.0 V \pm 10\%$, $T_a = -20$ to $75^\circ C$)

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit		
Operating voltage (1)	V_{SS}		V_{SS}	-5.5	-5.0	-4.5	V		
Recommended op. voltage	V_5		V_5	-28.0	—	-12.0	V		
Minimum operating voltage						-8.0			
Operating voltage (2)	V_0	Recommended value	V_0	-2.5	—	0	V		
Operating voltage (3)	V_2	Recommended value	V_2	5/9- V_5	—	V_0	V		
Operating voltage (4)	V_3	Recommended value	V_3	V_5	—	4/9- V_5	V		
"H" input voltage	V_{IH}		E101, E102, XSCL, LP, D0 to D7, FR, SHL	0.2 V_{SS}	—	—	V		
"L" input voltage	V_{IL}			—	—	0.8 V_{SS}	V		
"H" output voltage	V_{OH}	$I_{OH} = -0.6$ mA	E101, E102	-0.4	—	—	V		
"L" output voltage	V_{OL}	$I_{OL} = 0.6$ mA		—	—	$V_{SS} + 0.4$	V		
Input leakage current	I_{LI}	$V_{SS} \leq V_i \leq 0$ V	D0 to D7, LP, XSCL, SHL, FR	—	—	2.0	μA		
	$I_{LI/O}$	$V_{SS} \leq V_i \leq 0$ V	E101, E102	—	—	5.0	μA		
Stand-by current	I_{D0S}	$V_5 = -12.0$ to -28.0 V $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	V_{DD}	—	—	25	μA		
Output resistance	R_{SEG}	$ \Delta V_{ON} = 0.5V$	V_5	-20.0V	SEG0 to SEG79	—	1.4	3.5	$k\Omega$
				-14.0V		—	1.7	4.5	
				-8.0V		—	2.7	8.0	
Current dissipation (1)	I_{SSO1}	$V_{SS} = -5.0$ V, $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$, $f_{XSCL} = 1.92$ MHz $f_{LP} = 12$ kHz, Frame period = 60 Hz; Input data: Inverted bit by bit; No-load	V_{SS}	—	120	500	μA		
Current dissipation (2)	I_{SSO2}	$V_{SS} = -5.0$ V, $V_2 = -4.0$ V $V_3 = -16.0$ V, $V_5 = -20.0$ V All other conditions are same as I_{SSO1}	V_5	—	20	100	μA		
Input capacitance	C_i	$T_a = 25^\circ C$	D0 to D7, LP, XSCL, SHL, FR	—	—	8.0	pF		
	$C_{I/O}$		E101, E102	—	—	15.0	pF		

● AC Electrical Characteristics

(V_{SS} = -5.0 V ±10%, T_a = -20 to 75°C)

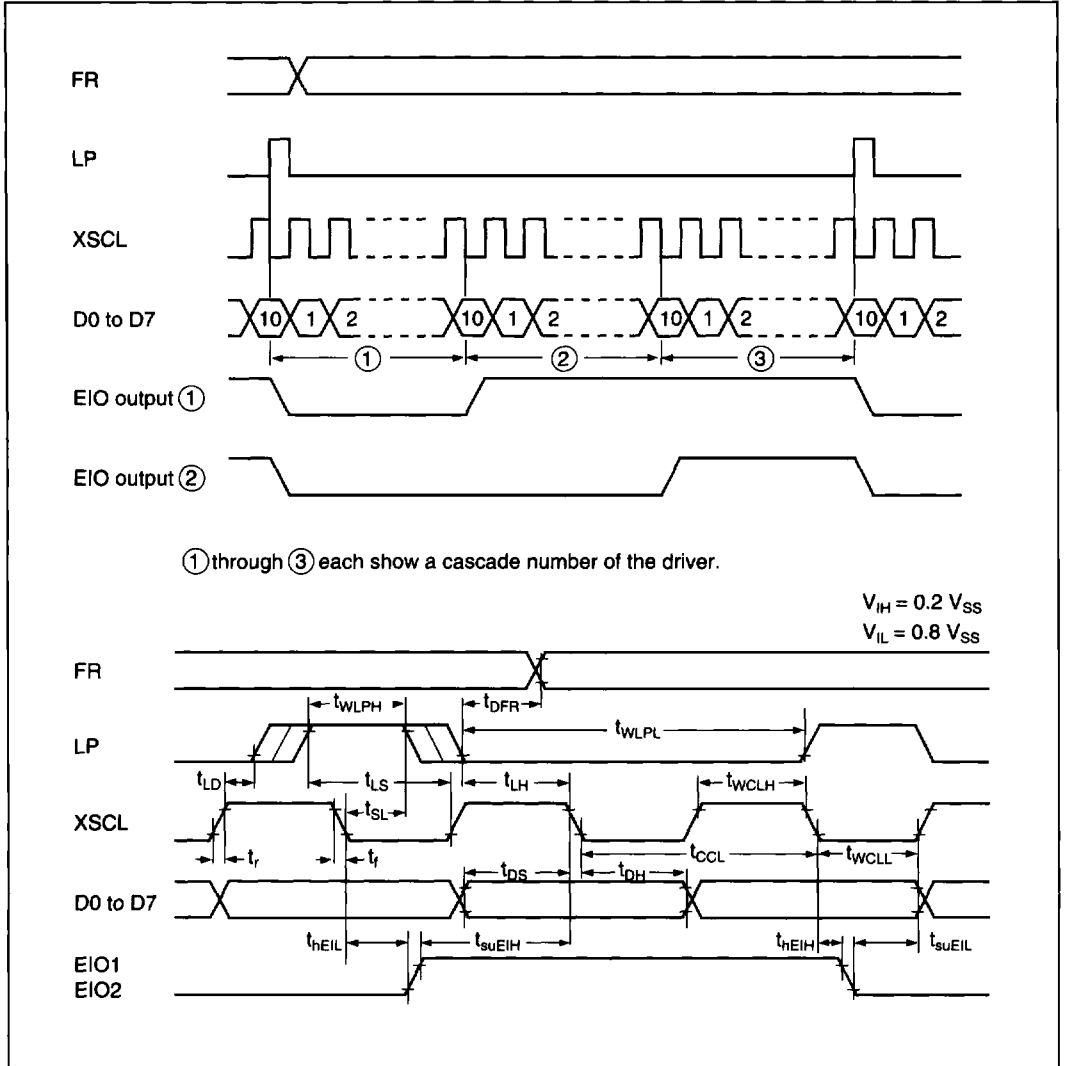
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t _{CCL}	t _r , t _f ≤ 10 ns	166	—	—	ns
XSCL "H" pulse width	t _{WCLH}		70	—	—	ns
XSCL "L" pulse width	t _{WCLL}		70	—	—	ns
Data setup time	t _{DS}		60	—	—	ns
Data hold time	t _{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t _{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t _{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t _{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t _{LH}		70	—	—	ns
LP "H" pulse width	t _{WLPH}		70	—	—	ns
LP "L" pulse width	t _{WLPL}		230	—	—	ns
Allowable FR delay time	t _{DFR}		-500	—	500	ns
Enable "H" setup time	t _{SUEIH}		40	—	—	ns
Enable "H" hold time	t _{HEIH}		0	—	—	ns
Enable "L" setup time	t _{SUEIL}		0	—	—	ns
Enable "L" hold time	t _{HEIL}		0	—	—	ns
Input signal rise time	t _r		—	—	50*	ns
Input signal fall time	t _f		—	—	50*	ns

* Note:

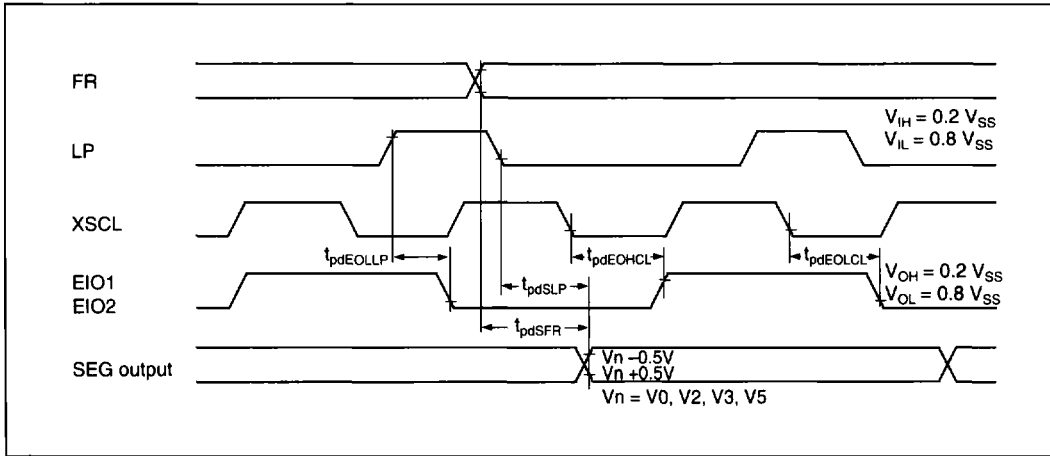
The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

- Timing Chart
- Input Timing



○ Output Timing

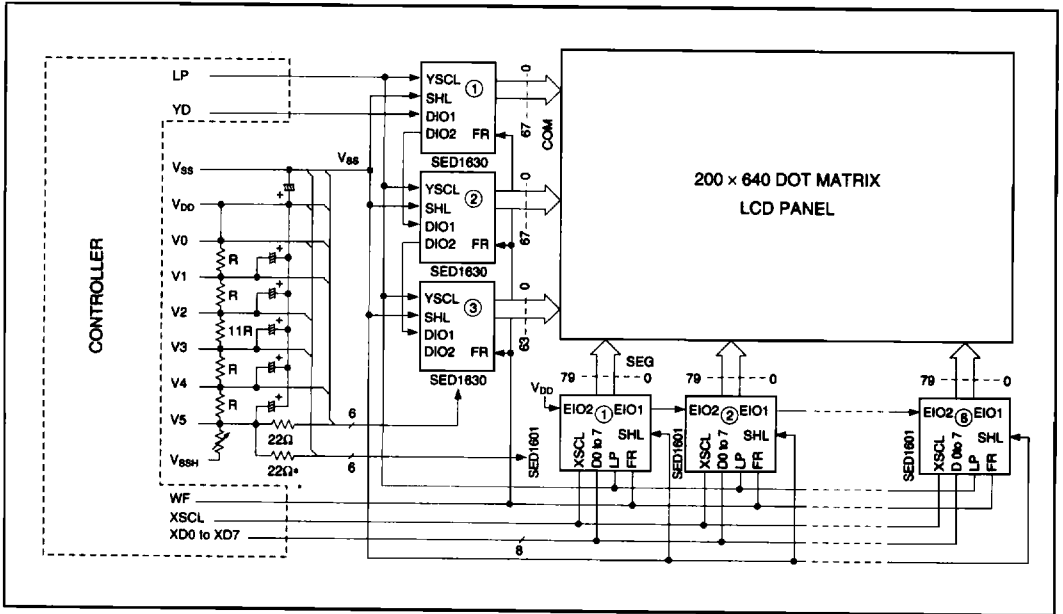


($V_{SS} = -5.0 V \pm 10\%$, $T_a = -20$ to $75^\circ C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H"	—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = -12.0 to -28.0 V	—	—	4.5	μs
(FR to SEG output) delay time	t_{pdSFR}	CL = 100 pF	—	—	4.5	μs

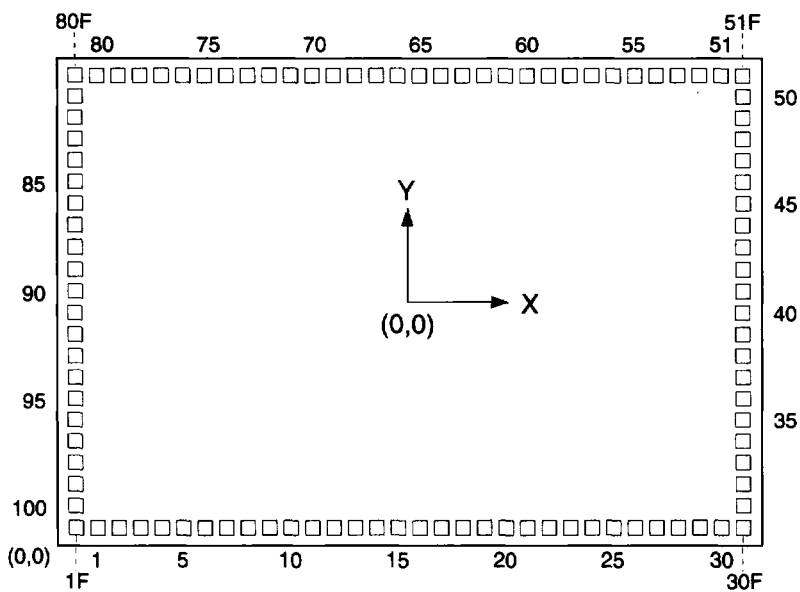
■ EXAMPLE OF APPLICATION (SED1601)

(for 200 × 640 DOT MATRIX LCD)



* Note: Be sure to connect a current limiter resistor. Also, connect decoupling capacitors (0.01μF) near pins Vss and V5 of each LSI for noise protection.

■ PAD LAYOUT (SED1601DAA)



Chip Size 6.20mm × 4.59mm
 Pad Pitch 0.18mm (MIN.)
 Pad Dimension 0.1mm × 0.1mm
 Chip Thickness 0.4mm±0.025mm

■ PAD COORDINATES (SED1601D_{AA})

Pad No.	Pad Name	X	Y
1	SEG0	-2700	-2120
2	SEG1	-2503	-2120
3	SEG2	-2306	-2120
4	SEG3	-2109	-2120
5	SEG4	-1912	-2120
6	SEG5	-1714	-2120
7	SEG6	-1534	-2120
8	SEG7	-1354	-2120
9	SEG8	-1174	-2120
10	SEG9	-994	-2120
11	SEG10	-813	-2120
12	SEG11	-633	-2120
13	SEG12	-453	-2120
14	SEG13	-273	-2120
15	SEG14	-93	-2120
16	SEG15	88	-2120
17	SEG16	268	-2120
18	SEG17	448	-2120
19	SEG18	628	-2120
20	SEG19	808	-2120
21	SEG20	989	-2120
22	SEG21	1169	-2120
23	SEG22	1349	-2120
24	SEG23	1529	-2120
25	SEG24	1709	-2120
26	SEG25	1907	-2120
27	SEG26	2104	-2120
28	SEG27	2301	-2120
29	SEG28	2498	-2120
30	SEG29	2695	-2120
31	SEG30	2925	-1895
32	SEG31	2925	-1669
33	SEG32	2925	-1443
34	SEG33	2925	-1217
35	SEG34	2925	-991
36	SEG35	2925	-811
37	SEG36	2925	-631
38	SEG37	2925	-450
39	SEG38	2925	-270
40	SEG39	2925	-90

Pad No.	Pad Name	X	Y
41	SEG40	2925	90
42	SEG41	2925	270
43	SEG42	2925	451
44	SEG43	2925	631
45	SEG44	2925	811
46	SEG45	2925	991
47	SEG46	2925	1217
48	SEG47	2925	1443
49	SEG48	2925	1689
50	SEG49	2925	1896
51	SEG50	2685	2120
52	SEG51	2498	2120
53	SEG52	2301	2120
54	SEG53	2104	2120
55	SEG54	1907	2120
56	SEG55	1709	2120
57	SEG56	1529	2120
58	SEG57	1349	2120
59	SEG58	1169	2120
60	SEG59	989	2120
61	SEG60	808	2120
62	SEG61	628	2120
63	SEG62	448	2120
64	SEG63	268	2120
65	SEG64	88	2120
66	SEG65	-93	2120
67	SEG66	-273	2120
68	SEG67	-453	2120
69	SEG68	-633	2120
70	SEG69	-813	2120
71	SEG70	-994	2120
72	SEG71	-1174	2120
73	SEG72	-1354	2120
74	SEG73	-1534	2120
75	SEG74	-1714	2120
76	SEG75	-1912	2120
77	SEG76	-2109	2120
78	SEG77	-2306	2120
79	SEG78	-2503	2120
80	SEG79	-2700	2120

Pad No.	Pad Name	X	Y
81	EIO2	-2925	1896
82	D0	-2925	1669
83	D1	-2925	1443
84	D2	-2925	1217
85	D3	-2925	991
86	D4	-2925	811
87	D5	-2925	631
88	D6	-2925	451
89	D7	-2925	270
90	VDD	-2925	90
91	VSS	-2925	-90
92	V0	-2925	-270
93	V2	-2925	-450
94	V3	-2925	-631
95	V5	-2925	-811
96	SHL	-2925	-991
97	XSCL	-2925	-1217
98	LP	-2925	-1443
99	FR	-2925	-1669
100	EIO1	-2925	-1895

*1

Pad No.	Pad Name	X	Y
1F	SEG0	-2925	-2120
30F	SEG29	2925	-2120
51F	SEG50	2925	2120
80F	SEG79	-2925	2120

*1 These pads are located at the corner: Pad Nos. 1F, 30F, 51F, and 80F. They have the same function as Pad Nos. 1, 30, 51, and 80.