Data Sheet | October 1, 2007 | FN6417.0

Dual 19V, 60MHz Rail-to-Rail Input-Output Operational Amplifier

The ISL24026 is a low power, high supply voltage, rail-to-rail input-output dual amplifier. Operating on supplies ranging from 5V to 19V while consuming only 3mA per amplifier, the ISL24026 has a bandwidth of 60MHz (-3dB) and provides common-mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables the ISL24026 to offer maximum dynamic range at any supply voltage.

The ISL24026 also features fast slewing and settling times, as well as a high output drive capability of 65mA (sink and source). These features make the ISL24026 ideal for high speed filtering and signal conditioning applications. Other applications include battery-powered, portable devices and anywhere low power consumption is important.

The ISL24026 is available in the 8 Ld HMSOP package, features a standard operational amplifier pinout, and is specified for operation over a temperature range of -40°C to +85°C.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL24026IUEZ	BBBEA	8 Ld HMSOP	MDP0050
ISL24026IUEZ-T13*	BBBEA	8 Ld HMSOP	MDP0050

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

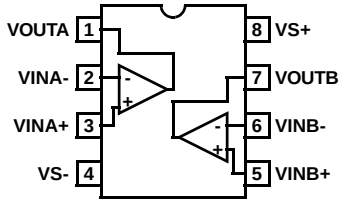
- 60MHz -3dB bandwidth
- Power supply operating range = 5V to 19V
- Low supply current (per amplifier) = 3mA
- High slew rate = 85V/µs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- ±140mA output short current
- Pb-free (RoHS compliant)

Applications

- TFT-LCD panels
- V_{COM} amplifiers
- Reference buffers
- Drivers for A-to-D converters
- Data acquisition
- Video processing
- Audio processing
- Active filters
- Test equipment
- Battery-powered applications
- Portable equipment

Pinout

ISL24026
(8 LD HMSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . +20V
Input Voltage . . . . . V_S- - 0.5V, V_S +0.5V
Maximum Continuous Output Current 65mA
Maximum Die Temperature . . . . . +150°C

Thermal Information

Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.
3. NTSC signal generator used.
4. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +18V, V_S- = 0V, R_L = 1kΩ to 9.0V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 9V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 9V		2	60	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.3		+18.3	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.3V to 18.3V	50	72		dB
A_{VOL}	Open-Loop Gain	0.5V ≤ V_{OUT} ≤ 18.5V	60	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		100	200	mV
V_{OH}	Output Swing High	I_L = 5mA	17.8	17.9		V
I_{SC}	Short-Circuit Output Current			±140		mA
I_{OUT}	Continuous Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 18.5V	60	80		dB
I_S	Total Supply Current	No load		6.6	8.5	mA
V_S	Power Supply Range		4.5		19	V
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	1V ≤ V_{OUT} ≤ 17V, 20% to 80%	65	85		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.16		%
d_P	Differential Phase (Note 3)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.22		°

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $R_L = 1k\Omega$ to 0V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	$V_{CM} = 0V$		2		nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.3		+5.3	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.3V to 5.3V		65		dB
A_{VOL}	Open-Loop Gain	$-4.5V \le V_{OUT} \le 4.5V$		80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		-4.9		V
V_{OH}	Output Swing High	$I_L = 5mA$		4.9		V
I_{SC}	Short-Circuit Output Current			±140		mA
I_{OUT}	Continuous Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
I_S	Total Supply Current	No load		6	7.8	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$-4.0V \le V_{OUT} \le 4.0V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.17		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.24		°

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 2.5V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2		nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.3		+5.3	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.3V to 5.3V		65		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUT} \le 4.5V$		84		dB

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 1k\Omega$ to 2.5V, $T_A = +25°C$, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		100		mV
V_{OH}	Output Swing High	$I_L = 5mA$		4.9		V
I_{SC}	Short-Circuit Output Current			±140		mA
I_{OUT}	Continuous Output Current			±65		mA
POWER SUPPLY PERFORMANCE						
I_S	Supply Current	No load		6	7.8	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$1V \le V_{OUT} \le 4V$, 20% to 80%		75		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		80		ns
BW	-3dB Bandwidth			60		MHz
GBWP	Gain-Bandwidth Product			32		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.17		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.24		°

Typical Performance Curves

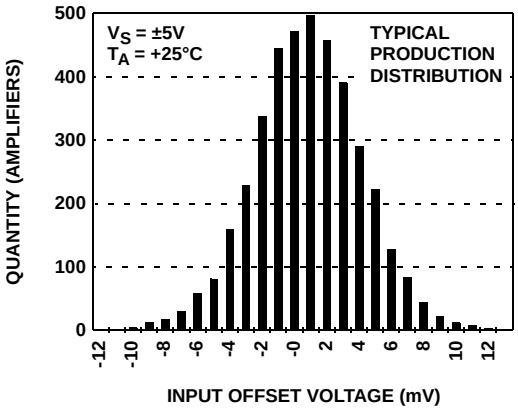


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

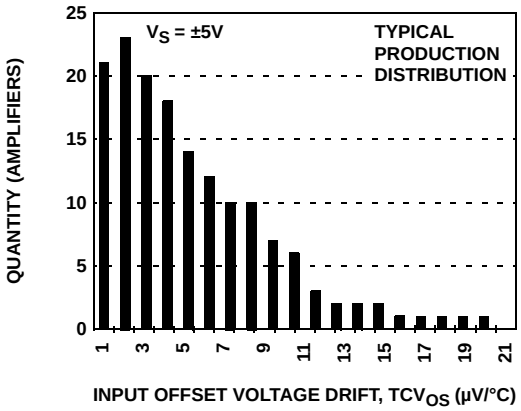


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

Typical Performance Curves (Continued)

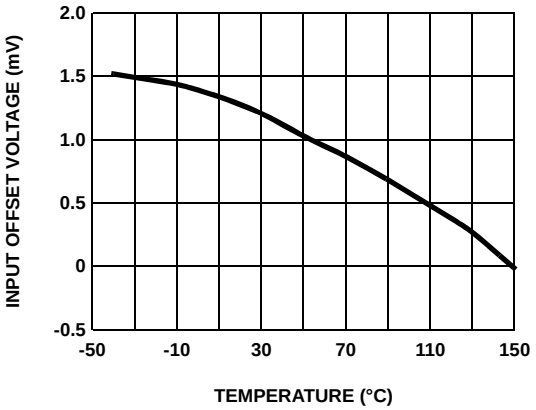


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

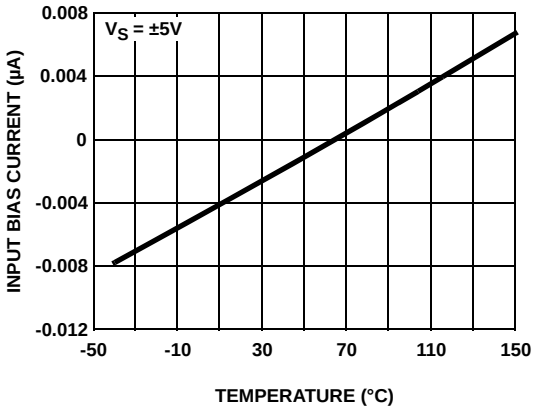


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

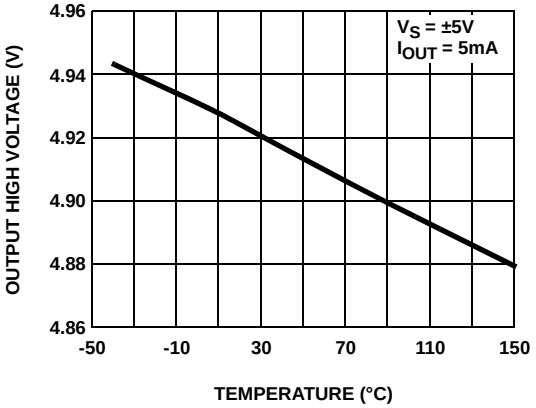


FIGURE 5. OUTPUT HIGH VOLTAGE vs TEMPERATURE

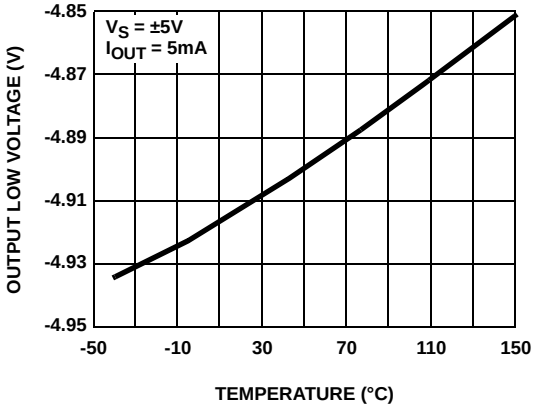


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

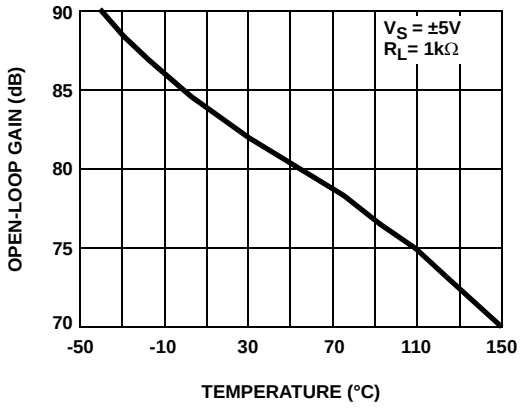


FIGURE 7. OPEN-LOOP GAIN vs TEMPERATURE

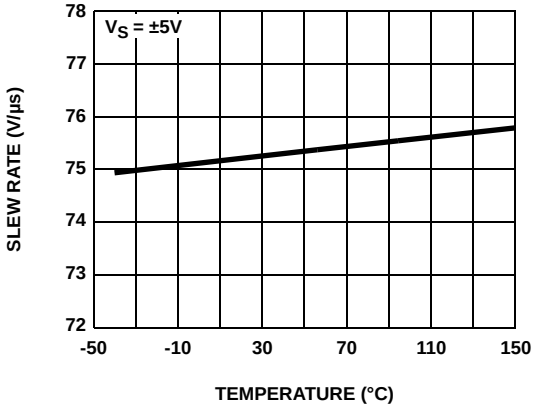


FIGURE 8. SLEW RATE vs TEMPERATURE

Typical Performance Curves (Continued)

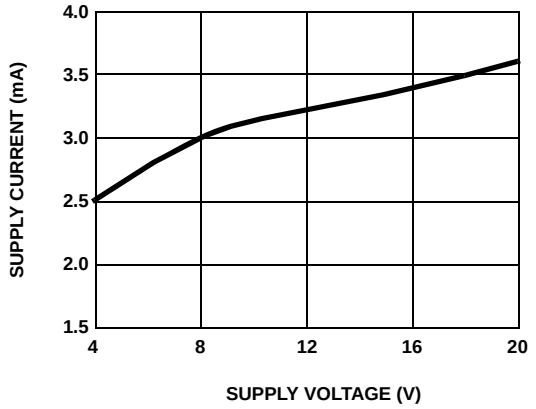


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

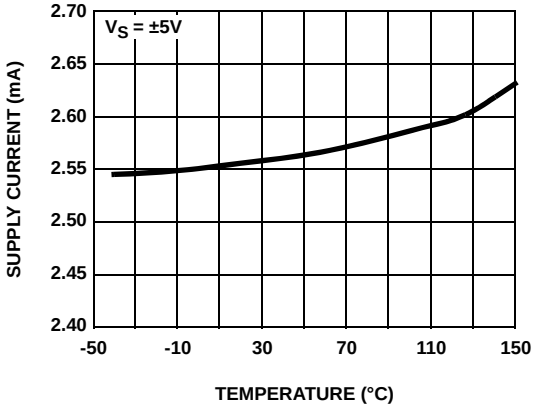


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

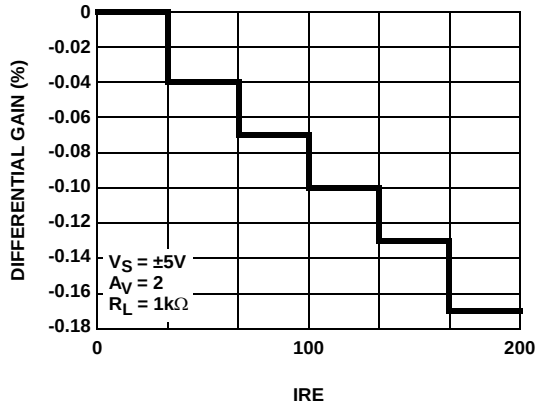


FIGURE 11. DIFFERENTIAL GAIN

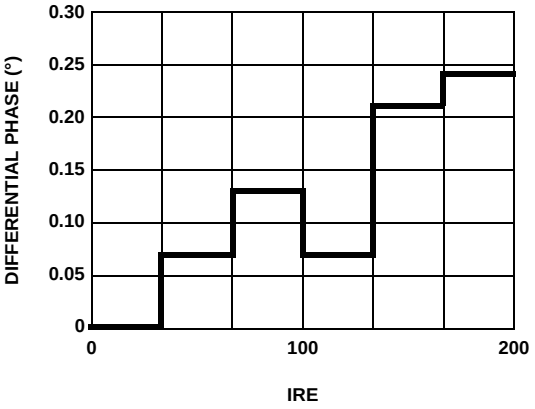


FIGURE 12. DIFFERENTIAL PHASE

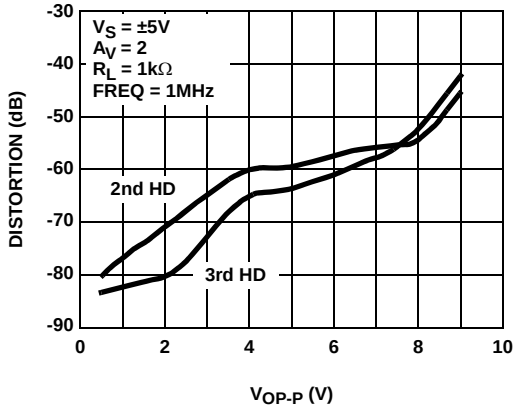


FIGURE 13. HARMONIC DISTORTION vs V_{OP-P}

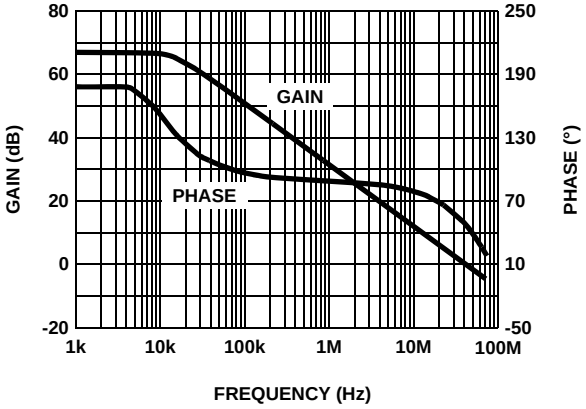


FIGURE 14. OPEN LOOP GAIN AND PHASE

Typical Performance Curves (Continued)

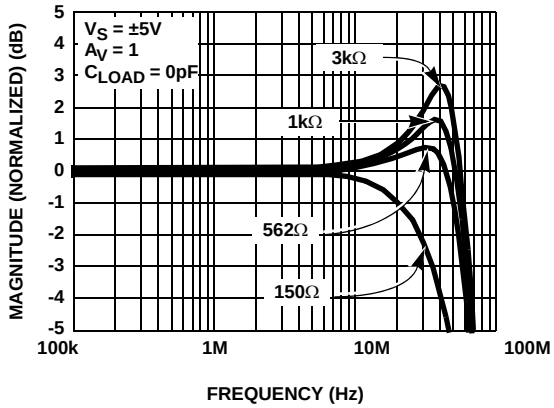


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS R_L

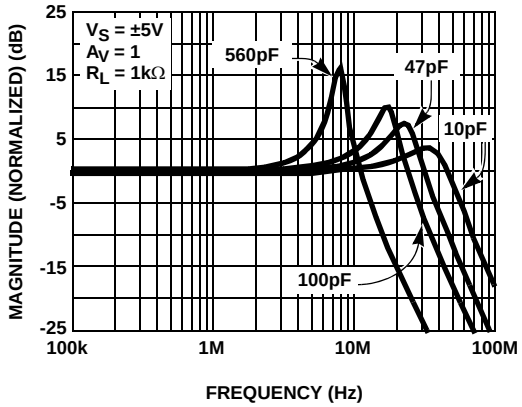


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS C_L

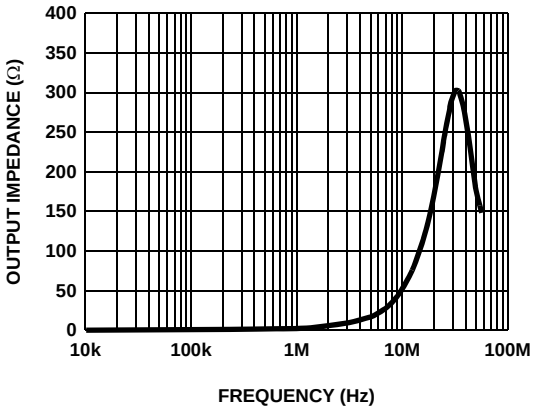


FIGURE 17. CLOSED LOOP OUTPUT IMPEDANCE

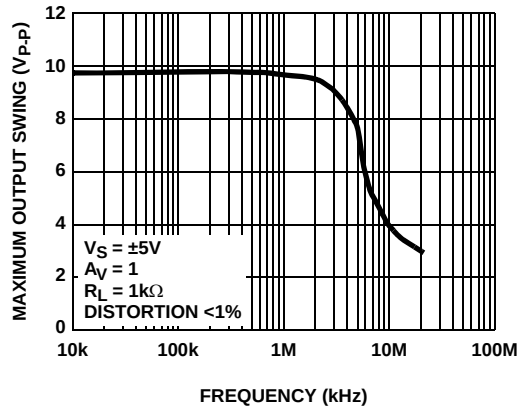


FIGURE 18. MAXIMUM OUTPUT SWING vs FREQUENCY

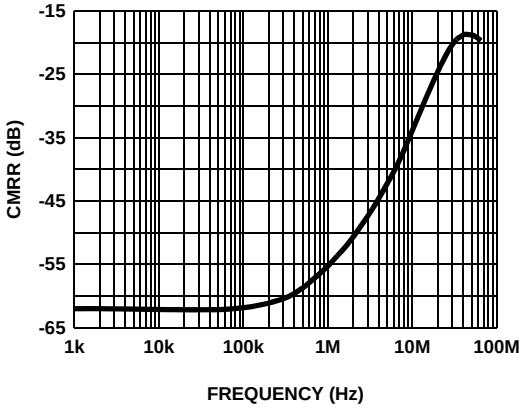


FIGURE 19. CMRR

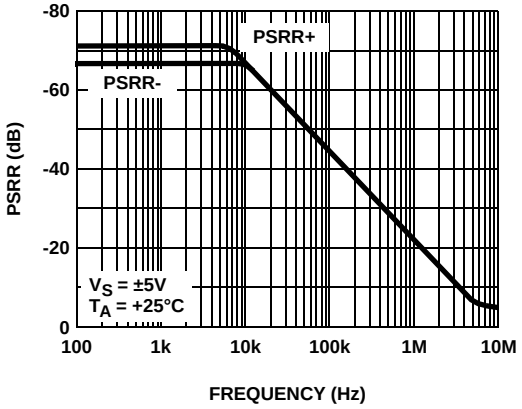


FIGURE 20. PSRR

Typical Performance Curves (Continued)

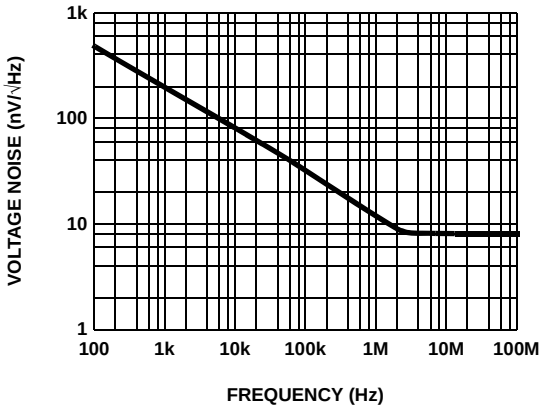


FIGURE 21. INPUT VOLTAGE NOISE SPECTRAL DENSITY

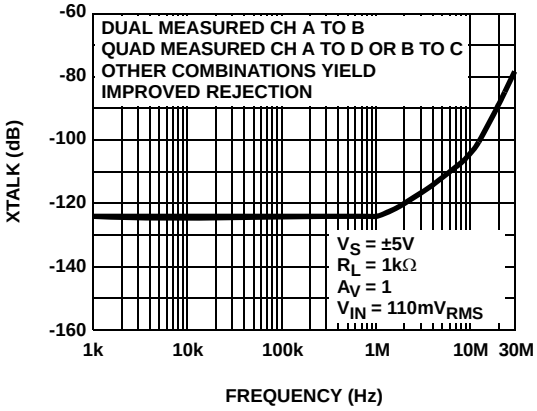


FIGURE 22. CHANNEL SEPARATION

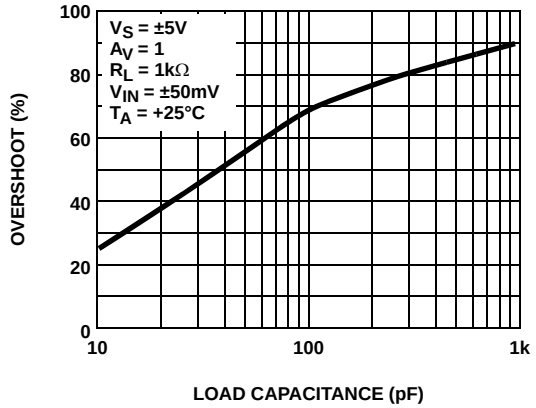


FIGURE 23. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

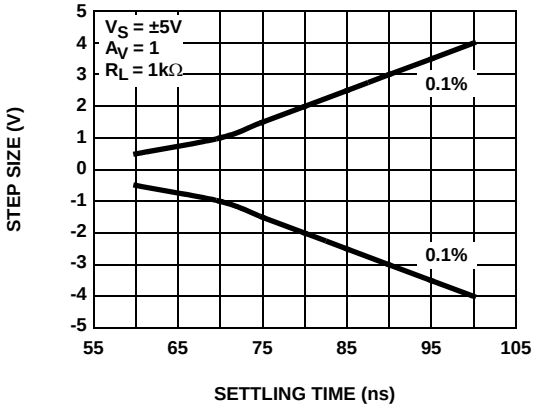


FIGURE 24. SETTLING TIME vs STEP SIZE

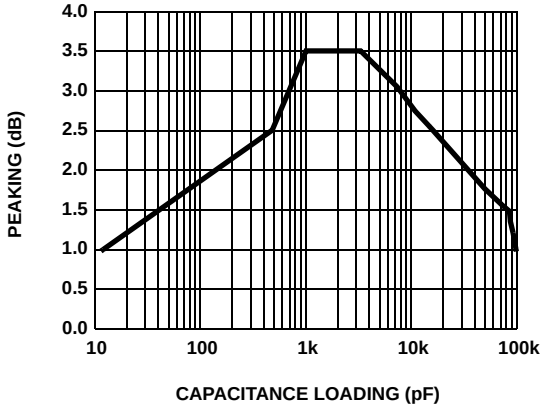


FIGURE 25. PEAKING vs C_L

Typical Performance Curves (Continued)

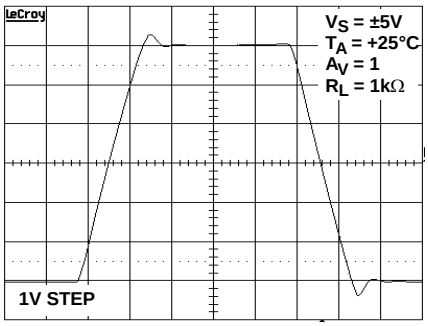


FIGURE 26. LARGE SIGNAL TRANSIENT RESPONSE

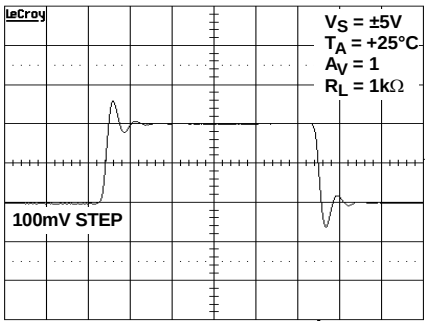
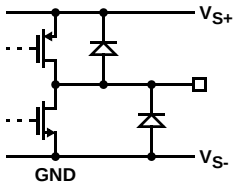
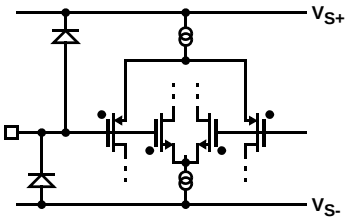


FIGURE 27. SMALL SIGNAL TRANSIENT RESPONSE

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUTA	Amplifier A output	 CIRCUIT 1
2	VINA-	Amplifier A inverting input	 CIRCUIT 2
3	VINA+	Amplifier A non-inverting input	(Reference Circuit 2)
4	VS-	Negative power supply	
5	VINB+	Amplifier B non-inverting input	(Reference Circuit 2)
6	VINB-	Amplifier B inverting input	(Reference Circuit 2)
7	VOUTB	Amplifier B output	(Reference Circuit 1)
8	VS+	Positive power supply	

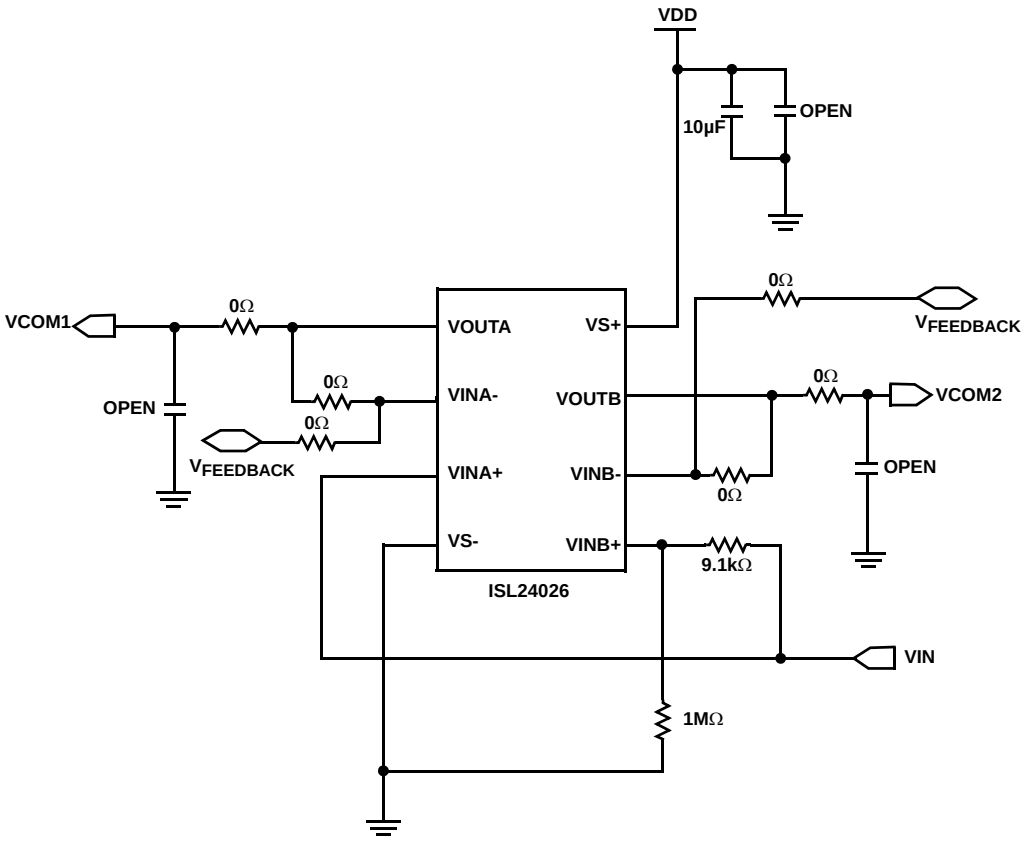


FIGURE 28. TYPICAL APPLICATION CIRCUIT

Applications Information

Product Description

The ISL24026 voltage feedback amplifier is fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability, is unity gain stable, and has low power consumption (3mA per amplifier). These features make the ISL24026 ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 1kΩ, the ISL24026 has a -3dB bandwidth of 60MHz while maintaining a 85V/µs slew rate. The ISL24026 is a dual amplifier.

Operating Voltage, Input and Output

The ISL24026 is specified with a single nominal supply voltage from 5V to 19V or a split supply with its total range from 5V to 19V. Correct operation is guaranteed for a supply range of 4.5V to 19V. Most ISL24026 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the "Typical Performance Curves" on page 4.

The input common-mode voltage range of the ISL24026 extends 500mV beyond the supply rails. The output swings of the ISL24026 typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 29 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ±5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.8V_{P-P}$.

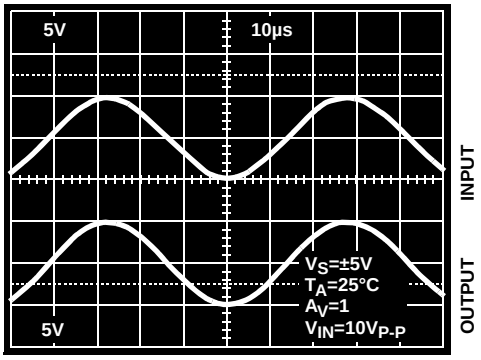


FIGURE 29. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The ISL24026 will limit the short circuit current to ±140mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power

dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±65mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The ISL24026 is immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 30 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

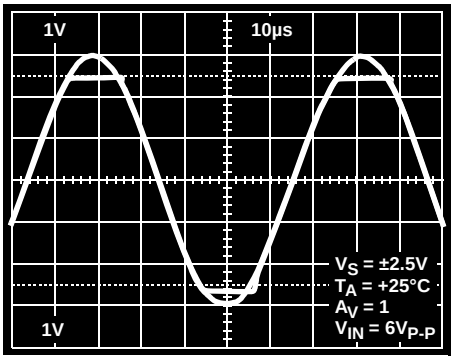


FIGURE 30. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the ISL24026 amplifier, it is possible to exceed the +125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or Equation 2:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S+ - V_{OUT}i) \times I_{LOAD}i] \quad \text{(EQ. 2)}$$

when sourcing, and Equation 3:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S-) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking,

where:

- i = 1 to 2 for dual and 1 to 4 for quad
- V_S = Total supply voltage
- I_{SMAX} = Maximum supply current per amplifier
- $V_{OUT}i$ = Maximum output voltage of the application
- $I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figures 31 and 32 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figures 31 and 32.

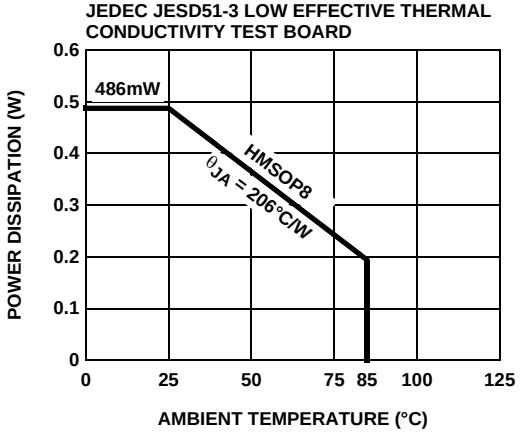


FIGURE 31. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

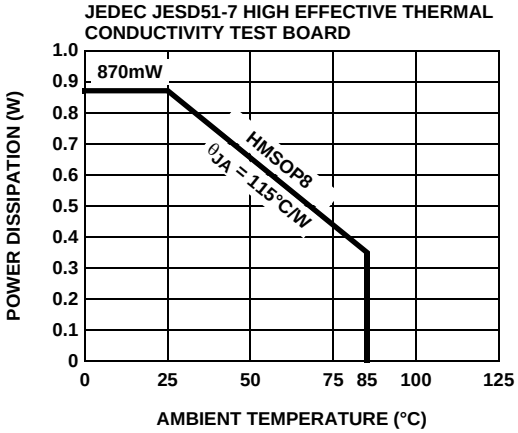


FIGURE 32. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

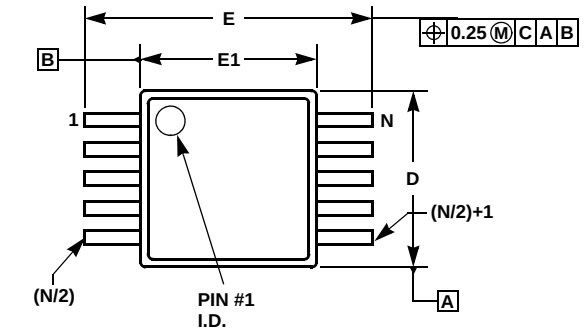
Unused Amplifiers

It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

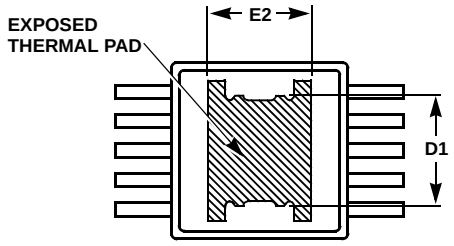
Power Supply Bypassing and Printed Circuit Board Layout

The ISL24026 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ pin to V_S- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

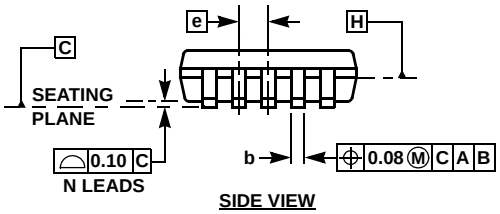
HMSOP (Heat-Sink MSOP) Package Family



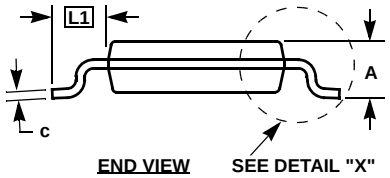
TOP VIEW



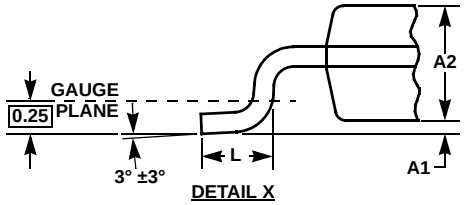
BOTTOM VIEW



SIDE VIEW



END VIEW SEE DETAIL "X"



DETAIL X

MDP0050

HMSOP (HEAT-SINK MSOP) PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	HMSOP8	HMSOP10		
A	1.00	1.00	Max.	-
A1	0.075	0.075	+0.025/-0.050	-
A2	0.86	0.86	±0.09	-
b	0.30	0.20	+0.07/-0.08	-
c	0.15	0.15	±0.05	-
D	3.00	3.00	±0.10	1, 3
D1	1.85	1.85	Reference	-
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
E2	1.73	1.73	Reference	-
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. 1 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.