



PRELIMINARY

# SOLID STATE DEVICES, INC.

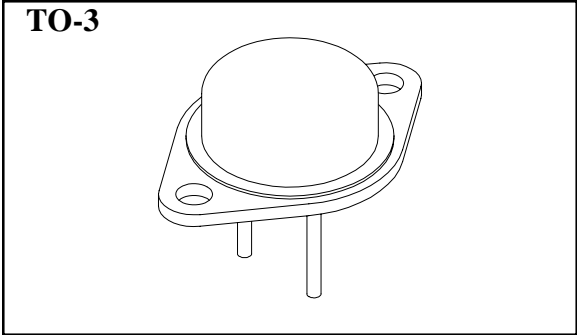
14830 Valley View Av. \* La Mirada, Ca 90670  
Phone: (562) 404-7855 \* Fax: (562) 404-1773

## DESIGNER'S DATA SHEET

- FEATURES:**
- Rugged construction with polysilicon gate
  - Low RDS (on) and high transconductance
  - Excellent high temperature stability
  - Very fast switching speed
  - Fast recovery and superior dv/dt performance
  - Increased reverse energy capability
  - Low input and transfer capacitance for easy paralleling
  - Hermetically sealed package
  - TX, TXV, and Space Level screening available
  - Replaces: SMM40N20 Type

# SFF1310M SFF1310Z

## 40 AMPS 200 VOLTS 0.050 Ω N-CHANNEL POWER MOSFET



## MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V <sub>DS</sub>	200	Volts
Gate to Source Voltage	V <sub>GS</sub>	±20	Volts
Continuous Drain Current	I <sub>D</sub>	40	Amps
Operating and Storage Temperature	T <sub>op</sub> & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	0.5	°C/W
Total Device Dissipation	P <sub>D</sub>	250 190	Watts

@ TC = 25°C  
@ TC = 55°C

**PACKAGE OUTLINE: TO-3**

**PINOUT:**  
 DRAIN: PIN 1  
 SOURCE: PIN 2  
 GATE: PIN 3

**NOTE:** All specifications are subject to change without notification. SCDs for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: FT0004A**

**SFF1310M**  
**SFF1310Z**

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**ELECTRICAL CHARACTERISTICS @ T<sub>J</sub>=25°C (Unless Otherwise Specified)**

RATING		SYMBOL	MIN	TYP	MAX	UNIT
<b>Drain to Source Breakdown Voltage</b> (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250μA)		<b>BV<sub>DSS</sub></b>	200	-	-	<b>V</b>
<b>Drain to Source ON State Resistance</b> (V <sub>GS</sub> = 10 V, 60% of Rated ID)	I <sub>D</sub> = 37.5A	<b>R<sub>DS(on)</sub></b>	- -	- -	0.050	<b>Ω</b>
<b>ON State Drain Current</b> (V <sub>DS</sub> > I <sub>D(on)</sub> x R <sub>DS(on)</sub> Max, V <sub>GS</sub> = 10 V)		<b>I<sub>D(on)</sub></b>	50	-	-	<b>A</b>
<b>Gate Threshold Voltage</b> (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 4mA)		<b>V<sub>GS(th)</sub></b>	2.0	-	4.0	<b>V</b>
<b>Forward Transconductance</b> (V <sub>DS</sub> > I <sub>D(on)</sub> x R <sub>DS(on)</sub> Max, I <sub>DS</sub> = 50% rated ID)		<b>g<sub>fs</sub></b>	20	25	-	<b>S(Ω)</b>
<b>Zero Gate Voltage Drain Current</b> (V <sub>GS</sub> = 0V) V <sub>DS</sub> = max rated Voltage, T <sub>A</sub> = 25°C V <sub>DS</sub> = 80% rated V <sub>DS</sub> , T <sub>A</sub> = 125°C		<b>I<sub>DSS</sub></b>	- -	- -	250 1000	<b>μA</b>
<b>Gate to Source Leakage Forward</b> <b>Gate to Source Leakage Reverse</b>	At rated V <sub>GS</sub>	<b>I<sub>GSS</sub></b>	- -	- -	+100 -100	<b>nA</b>
<b>Total Gate Charge</b>	V <sub>GS</sub> = 10 V	<b>Q<sub>g</sub></b>	-	190	220	<b>nC</b>
<b>Gate to Source Charge</b>	50% rated V <sub>DS</sub>	<b>Q<sub>gs</sub></b>	-	35	50	
<b>Gate to Drain Charge</b>	50% rated ID	<b>Q<sub>gd</sub></b>	-	95	120	
<b>Turn on Delay Time</b> <b>Rise Time</b> <b>Turn off DELAY Time</b> <b>Fall Time</b>	V <sub>DD</sub> = 50% rated V <sub>DS</sub> 50% rated ID R <sub>G</sub> = 6.2 Ω	<b>t<sub>d(on)</sub></b> <b>tr</b> <b>t<sub>d(off)</sub></b> <b>tf</b>	- - - -	28 38 110 30	35 40 130 35	<b>nsec</b>
<b>Diode Forward Voltage</b> (I <sub>S</sub> = rated I <sub>D</sub> , V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C)		<b>V<sub>SD</sub></b>	-	-	1.50	<b>V</b>
<b>Diode Reverse Recovery Time</b> <b>Reverse Recovery Charge</b>	T <sub>J</sub> = 25°C I <sub>F</sub> = 10A di/dt = 100A/μsec	<b>t<sub>rr</sub></b> <b>Q<sub>RR</sub></b>	- -	- 1.5	225 -	<b>nsec</b> <b>μC</b>
<b>Input Capacitance</b> <b>Output Capacitance</b> <b>Reverse Transfer Capacitance</b>	V <sub>GS</sub> = 0 Volts V <sub>DS</sub> = 25 Volts f = 1 MHz	<b>C<sub>iss</sub></b> <b>C<sub>oss</sub></b> <b>C<sub>rss</sub></b>	- - -	4400 800 285	- - -	<b>pF</b>

NOTES: