



## FQD18N20V2 / FQU18N20V2

### N-Channel QFET® MOSFET

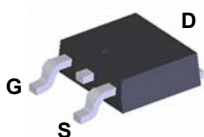
200 V, 15 A, 140 mΩ

#### Description

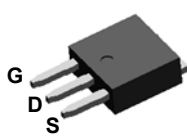
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

#### Features

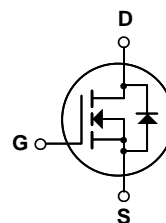
- 15 A, 200 V,  $R_{DS(on)} = 140 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$ ,  $I_D = 7.5 \text{ A}$
- Low Gate Charge (Typ. 20 nC)
- Low  $C_{rss}$  (Typ. 25 pF)
- 100% Avalanche Tested



D-PAK



I-PAK



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD18N20V2 / FQU18N20V2	Unit
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	15	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	9.75	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	60	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	340	mJ
$I_{AR}$	Avalanche Current (Note 1)	15	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	83	W
	- Derate above $25^\circ\text{C}$	0.67	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	FQD18N20V2 / FQU18N20V2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.25	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$	--	0.12	0.14	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 7.5\text{ A}$ (Note 4)	--	11	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	830	1080	pF
$C_{oss}$	Output Capacitance		--	200	260	pF
$C_{riss}$	Reverse Transfer Capacitance		--	25	33	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	70	--	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 160\text{ V}, V_{GS} = 0\text{ V}$	--	135	--	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 18\text{ A},$ $R_G = 25\ \Omega$	--	16	40	ns	
$t_r$	Turn-On Rise Time		--	133	275	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	38	85	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	62	135	ns
$Q_g$	Total Gate Charge		$V_{DS} = 160\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$	--	20	26	nC
$Q_{gs}$	Gate-Source Charge	(Note 4, 5)	--	5.6	--	nC	
$Q_{gd}$	Gate-Drain Charge	(Note 4, 5)	--	10	--	nC	

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	15	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	60	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 18\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	158	--	ns
$Q_{rr}$	Reverse Recovery Charge	(Note 4)	--	1.0	--	$\mu\text{C}$

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 1.58\text{ mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 18\text{ A}, dI/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

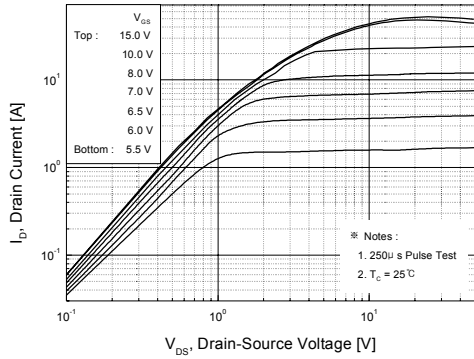


Figure 1. On-Region Characteristics

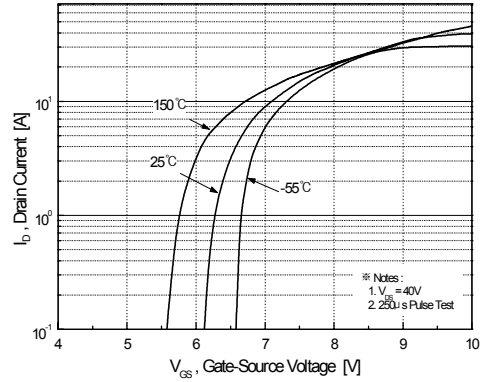


Figure 2. Transfer Characteristics

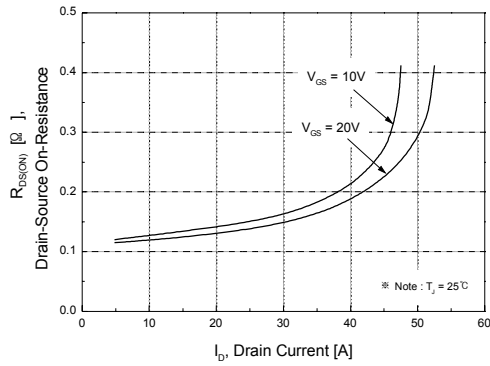


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

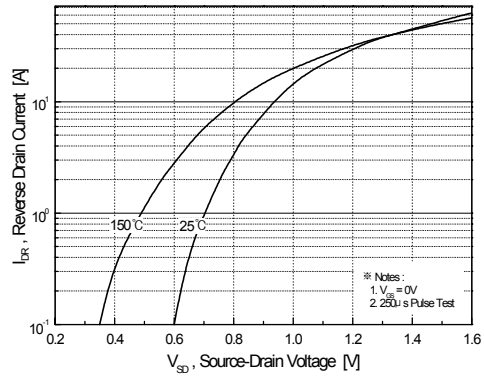


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

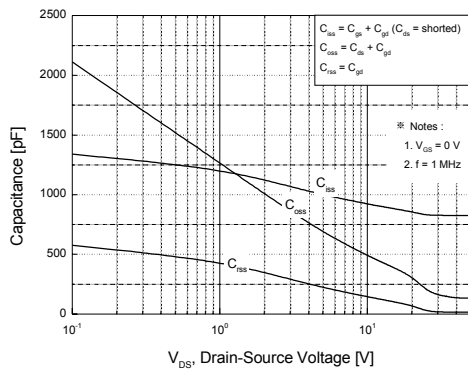


Figure 5. Capacitance Characteristics

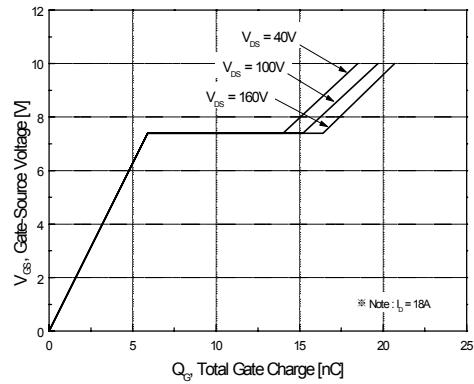
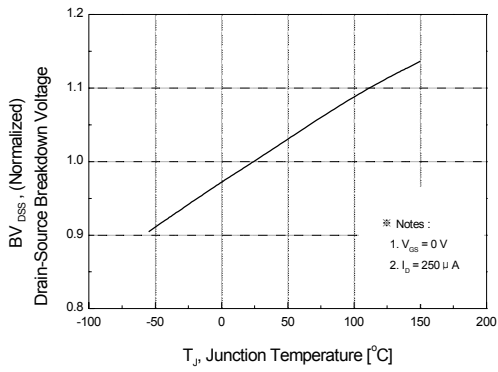
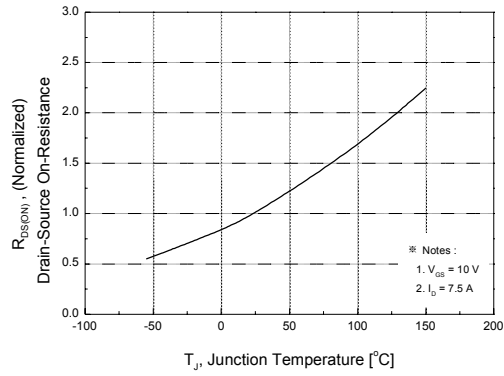


Figure 6. Gate Charge Characteristics

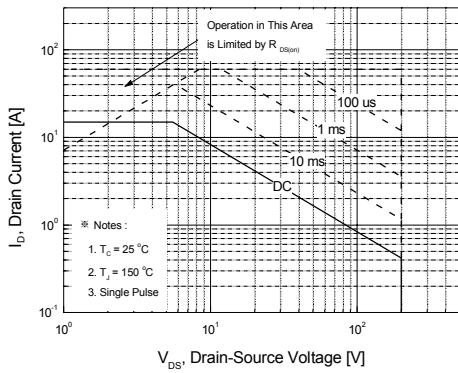
**Typical Characteristics** (Continued)



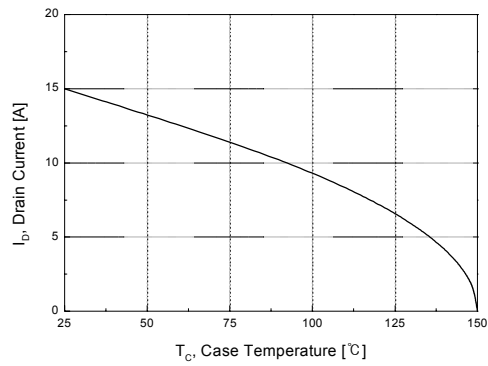
**Figure 7. Breakdown Voltage Variation vs. Temperature**



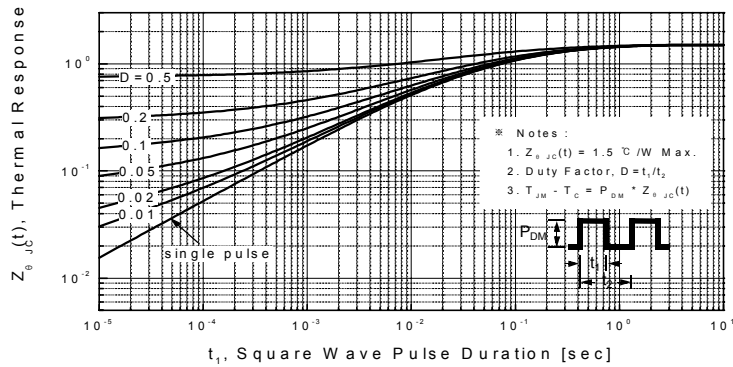
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

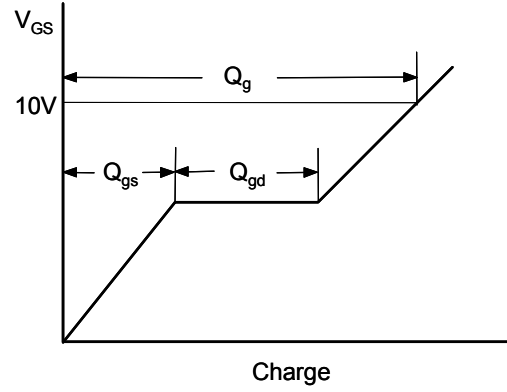
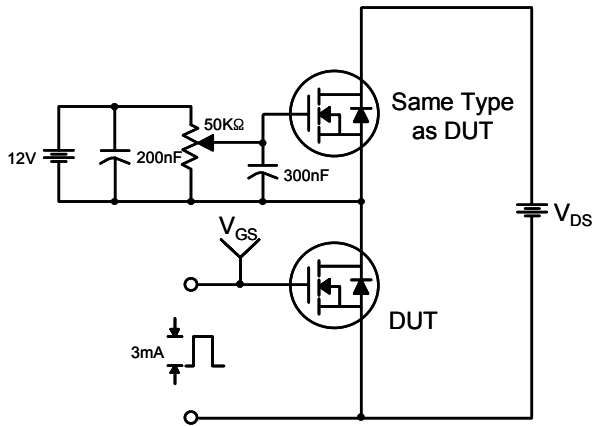


**Figure 10. Maximum Drain Current vs. Case Temperature**

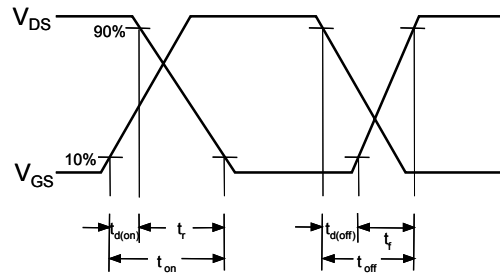
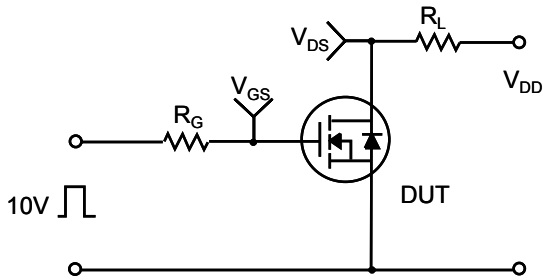


**Figure 11. Transient Thermal Response Curve**

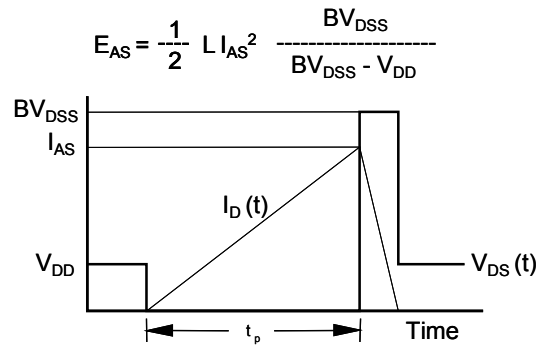
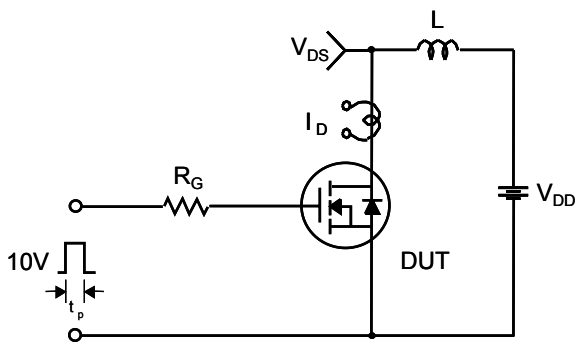
**Gate Charge Test Circuit & Waveform**



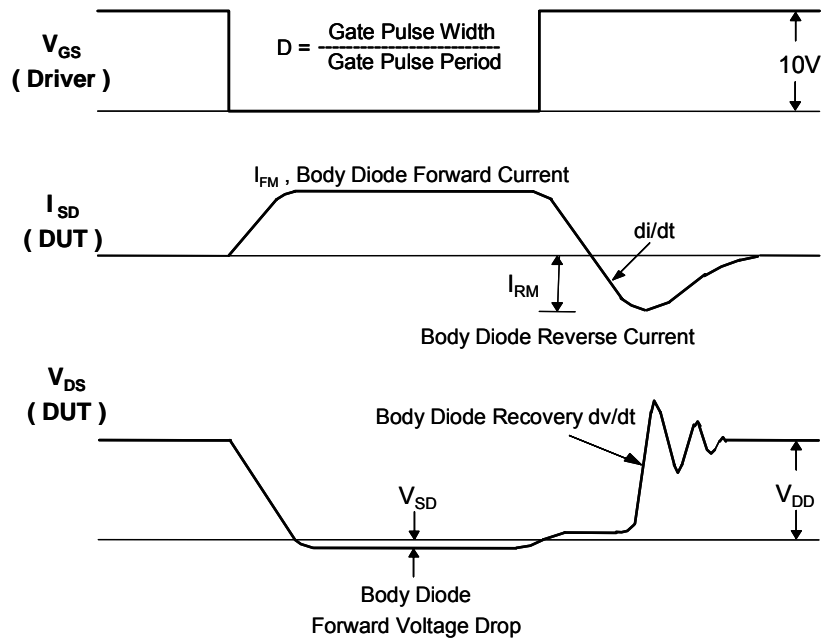
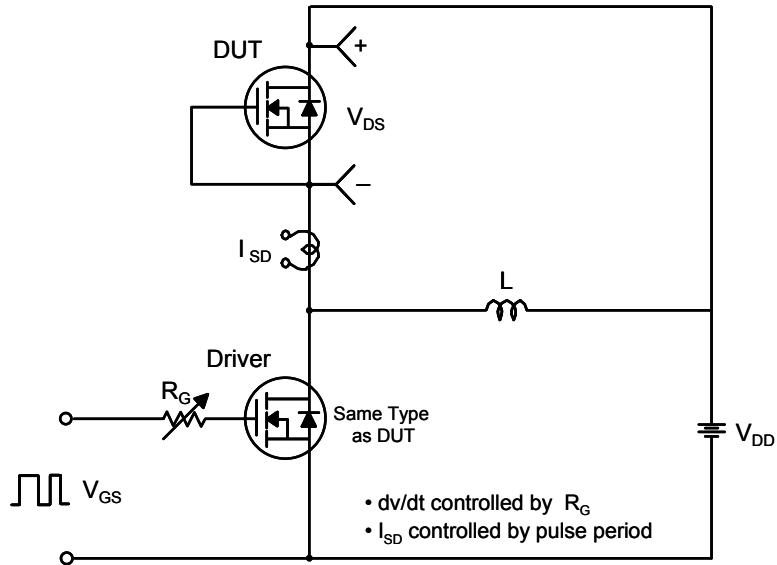
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

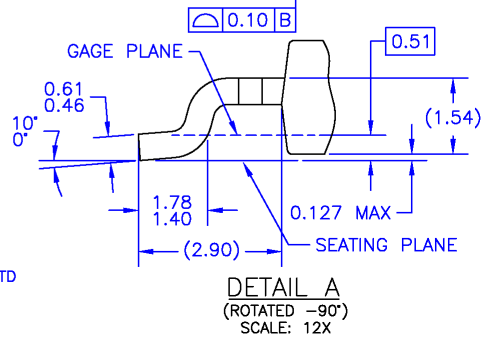
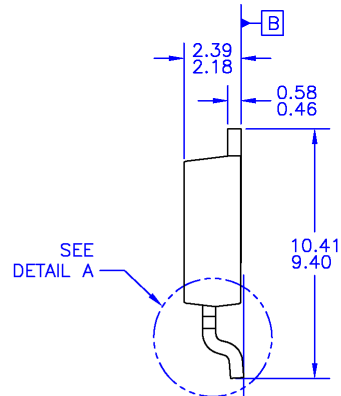
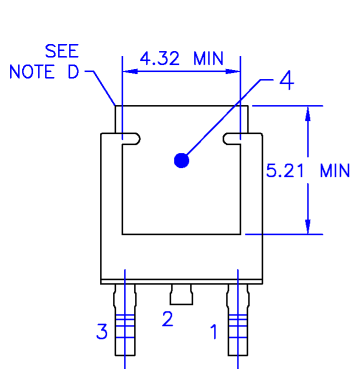
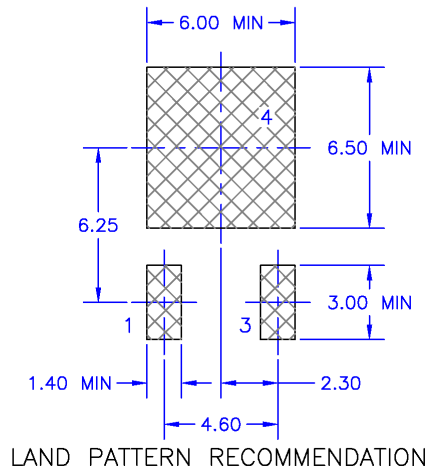
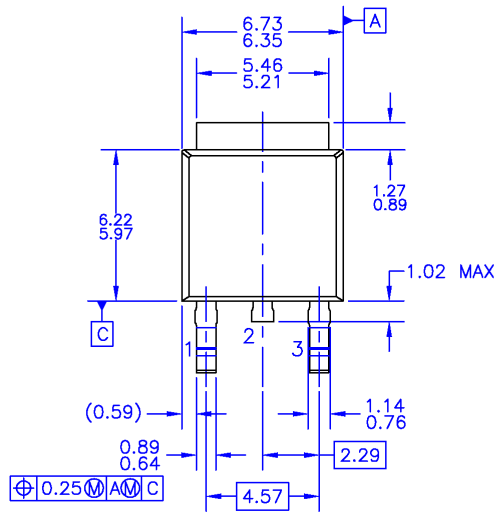


Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Mechanical Dimensions

### D-PAK

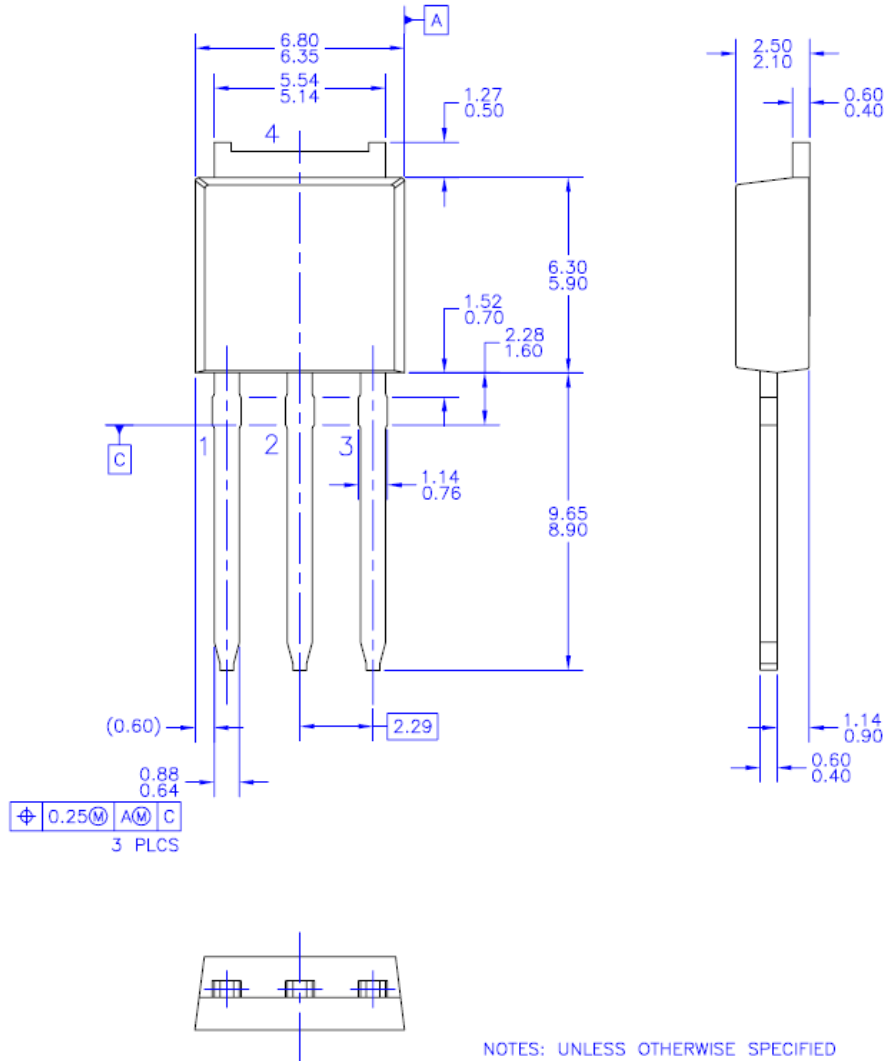


- NOTES: UNLESS OTHERWISE SPECIFIED
- THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters

## Mechanical Dimensions

### I-PAK



Dimensions in Millimeters





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| BitSiC™                  | Global Power Resource <sup>SM</sup>             | QFET®                      | TinyBuck™        |
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