July 1997

UltraSPARC™-IIi

DATA SHEET — Highly Integrated 64-Bit RISC Processor, PCI Interface

FUNCTIONAL DESCRIPTION

UltraSPARC-IIi (SME1040) is a highly-integrated 64-bit SPARC V9 superscalar processor. An optional APB™ (Advanced PCI Bridge -- SME2411) is available to increase connectivity and support demand for PCI I/O bandwidth. The UltraSPARC-IIi interfaces have been optimized to the "sweet spot" of typical uniprocessor system requirements. This means a balanced price-performance solution delivering the power and features that a majority of high-end applications need, optimizing power utilization and supporting manufacturability and ease-of-use.

UltraSPARC-IIi and the Advanced PCI Bridge allow designers to add UltraSPARC price-performance levels to a broad range of embedded and desktop designs. This CPU-Bridge combination not only optimizes embedded designs that require maximum processing power — such as telecommunications devices, set-top boxes, high-end printers and photocopiers — but the UltraSPARC-IIi also drives desktop applications, supporting connection to a wide array of PCI-compatible devices up to 66 MHz (directly) and 33 MHz (across the bridge).

Features

- SPARC V9 Architecture Compliant
- Binary Compatible with all SPARC Application Code
- VIS Instruction Set (Extended V9 Instructions)
- 4-way SuperScalar Design with 9 Execution Units
  - 4 Integer Execution Units
  - 3 Floating-Point Execution Units
  - 2 Graphics Execution Units
- Directly Addresses Little- or Big-Endian Data
- 64-Bit Address Pointers
- 16-Kilobyte Non-blocking Data Cache
- 16-Kilobyte Instruction Cache
  - In-Cache 2-bit Branch Prediction
  - Single Cycle Branch Following
- Integrated Second Level (E-Cache) Controller
- Supports 0.25- to 2- Megabyte Cache Sizes
- Integrated Control of 400 Megabyte/sec EDO Dram Memory Subsystem

Benefits

- 64-Byte Block Load and Block Store Instructions
- Supports Software Data Prefetch into E-Cache
- Supports up to 3 Outstanding E-Cache Misses
- Supports UPA64S Interface
  - 800 Megabyte/Sec
  - 64-Bit Slave Interface for Graphics or Similar Subsystems
- Integrated Rev 2.1 PCI
  - Higher Sustained PIO and DMA PCI I/O Bandwidth than Competing Solutions
  - Read Prefetch and Write Gathering and Posting
- PCI DMA is Cache Coherent
  - Dedicated TLB Provides Mapping and Protection
- JTAG Boundary Scan
- Technology/Packaging
  - 0.35 um 5-Layer Metal CMOS Process
  - 2.6 V & 3.3 V (IO Only) Power Supplies
- 266 Mhz and 300 Mhz processor clock hardware options

The UltraSPARC-II*i* (with a 0.5 Megabyte cache) achieves estimated SPECint95 and SPECfp95 benchmarks of 10 and 12, respectively. At the same time, it provides industry-leading bandwidth and latency. The UltraSPARC-II*i* has integrated a memory controller and the I/O interfaces onto the microchip.

Figure 1 shows a high-level illustration of an UltraSPARC-II*i*-based system. This system minimizes the memory-to-CPU bottleneck by using the following interface speeds:

Hardware Interface	266 MHz CPU	300 MHz CPU
CPU	266 MHz	300 MHz
SRAM external cache (E-Cache)	133 MHz	150 MHz
DRAM data throughput	67 MHz	75 MHz
PCI	up to 66 MHz	up to 66 MHz

As shown in "Product System and Subsystems" beginning on page 302, this solution supports a wide array of applications.

Each functional area on the UltraSPARC-II*i* maintains decentralized control, allowing many activities to overlap. Sustained performance of up to 4 instructions per cycle is supported (even in the presence of conditional branches and cache misses) by a decoupled Prefetch and Dispatch Unit. Load buffers on the input side of the Execution Unit, together with store buffers on the output side, decouple pipeline execution from data cache misses. Instructions predicted to be executed are issued in program order to multiple functional units. Such instructions are executed in parallel and may be completed out of order. The separate Memory Control and PCI I/O interface units also decouple their related key activities from the instruction pipeline.

UltraSPARC-II*i* supports the VIS extended instruction set for the V9 architecture. Use of VIS in conjunction with the four-way superscalar pipeline on the i-series processors enhances the performance for a wide range of networking applications, including TCP/IP. Use of VIS instructions also enables speed-up of I/O operations. In addition, VIS instructions support:

- H.261 real-time video compression/decompression
- one stream of MPEG-2 decompression at full broadcast quality without any additional hardware support

The UltraSPARC-II*i* processor supports Sun's popular Solaris operating system and is binary-compatible with the broad array of existing applications. In addition, Sun is planning robust third-party real-time operating system (RTOS) and development tool support for embedded applications.

The UltraSPARC-II*i* will be available as an individual component, on integrated cache-based modules and on industry-standard format board solutions. Please contact your Sun representative for current information on these products.

System Illustration

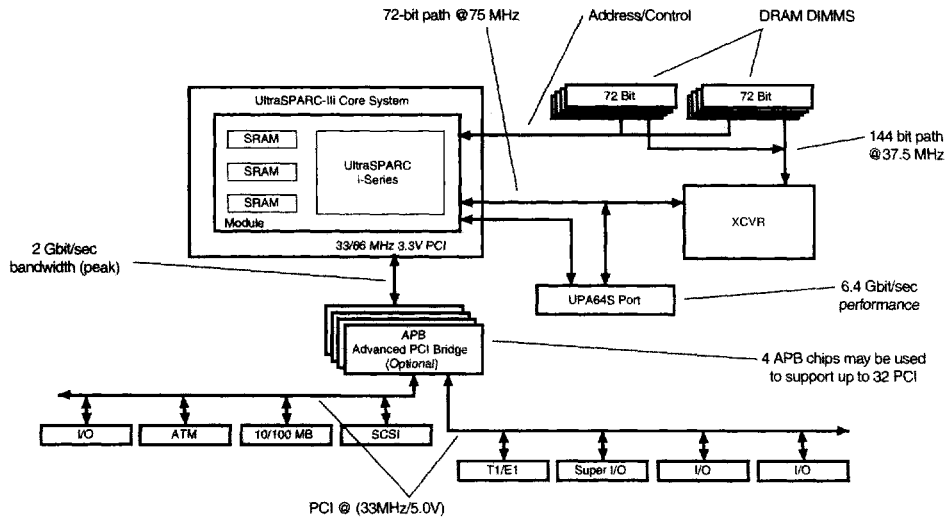


Figure 1. UltraSPARC-IIi System Implementation Example

For more detailed information, see "Product System and Subsystems" beginning on page 302.

Block Diagram

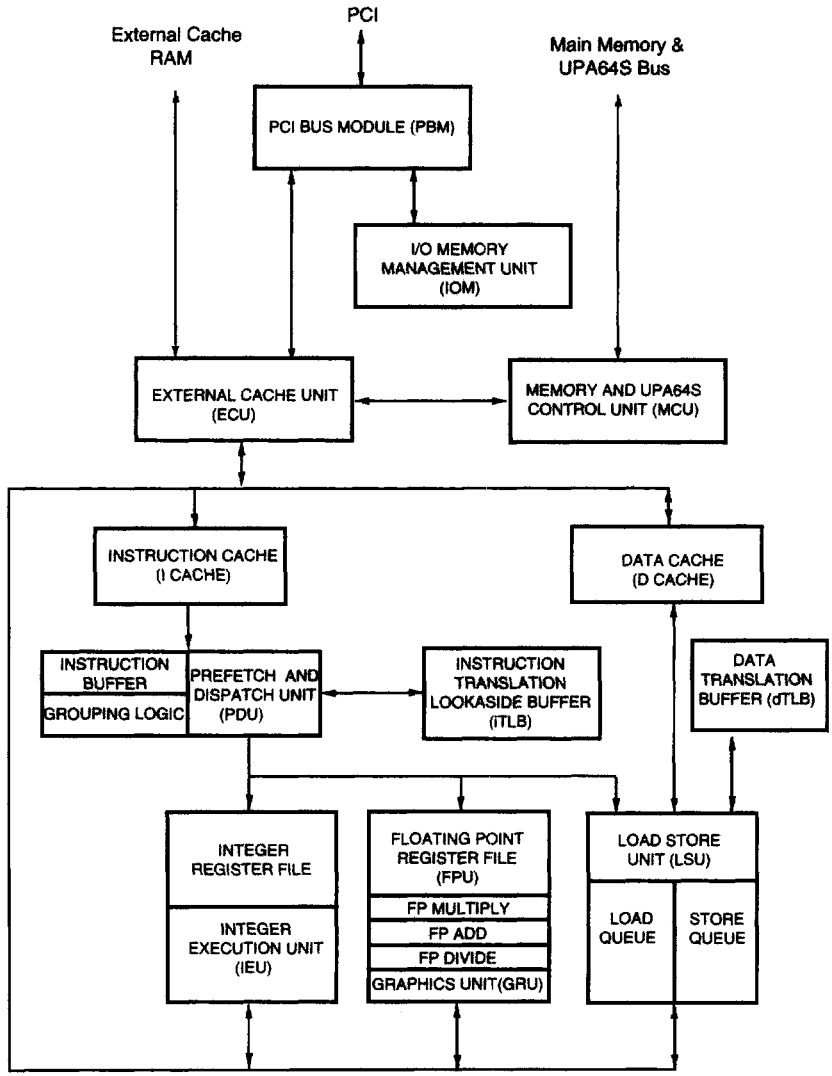


Figure 2. Functional Block Diagram of UltraSPARC-II*i*

Component Overview

In a single-chip implementation, UltraSPARC-IIi integrates the following components (see *Figure 2*):

- Independently clocked (132 MHz internal, 66 or 33 MHz external) PCI interfaces, fully decoupled from the main CPU
- PCI bus module (PBM)
- PCI I/O memory management unit (IOM) with 16 entries for incoming I/O to physical mapping/protection
- External (E-Cache) cache control unit (ECU)
- Memory controller unit (MCU), operates both the 144-bit-wide DRAM subsystem and the UPA64S interface
- 16-Kilobyte instruction cache (I-Cache)
- 16-Kilobyte data cache (D-Cache)
- Prefetch, branch prediction and dispatch unit (PDU) containing grouping logic and an instruction buffer
- A 64-entry instruction translation lookaside buffer (iTLB) and a 64-entry data translation lookaside buffer (dTLB)
- Integer execution unit (IEU) with two arithmetic logic units (ALUs)
- Floating-point unit (FPU) with independent add, multiply and divide/square root sub-units
- Graphics unit (GRU) composed of two independent execution pipelines
- Load buffer and store buffer unit (LSU), decoupling data accesses from the pipeline

PCI Bus Module (PBM)

The PBM interfaces UltraSPARC-IIi directly with a 32-bit PCI bus, compliant with the PCI specification, revision 2.1. The PCI bus runs at speeds up to 66MHz, typically 33 and 66 MHz. The PBM is optimized for 16-, 32- and 64-byte transfers, and can support up to four PCI bus masters. The module also queues pending interrupts received from the interrupt concentrator (or RIC-SME2210) chip. The entire PCI address space is noncacheable for CPU references but coherent DMA is supported. (This means that all writes to memory from PCI, and reads from memory, are cache coherent.) Interrupt handling is synchronized to the completion of all prior DMA writes.

IO Memory Management Unit (IOM)

The IOM performs address translations from 32-bit DVMA to 34-bit physical addresses when UltraSPARC-IIi is a PCI target (when DVMA read/write access is required). The IOM uses a fully-associative 16-entry TLB (translation lookaside buffer). In the case of a TLB miss, the IOM performs a single-level hardware tablewalk into the large translation storage buffer (TSB) in memory.

External Cache Control Unit (ECU)

The main role of the ECU is to handle I-Cache and D-Cache misses efficiently. The ECU can handle one access every other cycle to the external cache. Loads that miss in the D-Cache cause 16-byte D-Cache fills using two consecutive 8-byte accesses to the E-Cache. Stores are writethrough to the E-Cache and are fully pipelined. Instruction prefetches that miss the I-Cache cause 32-byte I-Cache fills using four consecutive 8-byte accesses to the E-Cache. The E-Cache is parity-protected.

In addition, the ECU supports DMA accesses which hit in the external cache and maintains data coherency between the external cache and the main memory. The size of the external cache can be 256 KB, 512 KB, 1 MB, or 2 MB (where the line size is always 64 bytes). Cache lines have only 3 states: modified, exclusive or invalid.

The combination of the load buffer and the ECU is fully pipelined. For programs with large data sets, instructions are scheduled with load latencies based on the E-Cache latency, so the E-Cache acts as a large primary cache. Floating-point applications use this feature to effectively "hide" D-Cache misses. Coherency is maintained between all caches and external PCI DMA references.

The ECU overlaps processing during load and store misses. Stores that hit the E-Cache can proceed while a load miss is being processed. The ECU is also capable of processing reads and writes without a costly turnaround penalty on the bidirectional E-Cache data bus.

Block loads and block stores (these load or store a 64-byte line of data from memory or E-Cache to the floating-point register file) provide high transfer bandwidth. By not installing into the E-Cache on miss, they avoid polluting the cache with data that is only touched once.

The ECU also provides support for multiple outstanding data transfer requests to the MCU and PBM.

Memory Controller Unit (MCU)

All transactions to the DRAM and UPA64S subsystems are handled by the MCU. The external pins controlled by the MCU operate at divisions of the processor clock:

- UPA64S runs at 1/3 the processor clock
- data transfers to the DRAM transceivers typically occur at 1/4 of the processor clock rate (programmable)

External data transceivers allow the DRAM data to be twice as wide as data from the processor's MEMDATA pins, so the EDO CAS cycle is only 26.5 ns at 300 MHz. The MCU supports a composite DRAM specification which is a superset of 60 ns EDO DRAM specifications from all major vendors.

Use of faster DRAMs allow higher-than-quoted performance, because the various components of memory delay are programmable.

Instruction Cache (I-Cache)

The I-Cache is a 16 Kilobyte two-way set-associative cache with 32-byte blocks. The cache is physically indexed and physically tagged. The set is predicted as part of the "next field" so that only the index bits of an address are necessary to address the cache. (This means only 13 bits, which matches the minimum page size.) The instruction cache returns up to 4 instructions from a line that is 8 instructions wide.

Data Cache (D-Cache)

The data cache is a write-through non-allocating 16 Kilobyte direct-mapped cache with two 16-byte subblocks per line. It is virtually indexed and physically tagged. The tag array is dual-ported so that tag updates due to line fills do not collide with tag reads for incoming loads. Snoops to the D-Cache use the second tag port so that an incoming load can proceed without being held up by a snoop.

Prefetch and Dispatch Unit (PDU)

The PDU fetches instructions before they are needed in the pipeline, so that the execution units do not starve for instructions. Instructions can be prefetched from all levels of the memory hierarchy, including the instruction cache, the external cache, and the main memory. To prefetch across conditional branches, a dynamic branch prediction scheme is implemented in hardware, based on a two-bit history of the branch. A "next field" associated with every four instructions in the I-Cache points to the next I-Cache line to be fetched. This makes it possible to follow taken branches and provides the same instruction bandwidth achieved during sequential code. Up to 12 prefetched instructions are stored in the instruction buffer sent to the rest of the pipeline.

Translation Lookaside Buffers (iTLB and dTLB)

The Translation Lookaside Buffers provide mapping between 44-bit virtual addresses and 34-bit physical addresses. A 64-entry iTLB is used for instructions and a 64-entry dTLB for data, and both are fully associative. UltraSPARC-II*i* provides hardware support for a software-based TLB miss strategy. For low-latency miss handling, a separate set of global registers is available whenever such a trap is encountered. Page sizes of 8 KB, 64 KB, and 512 KB and 4 MB are supported.

Integer Execution Unit (IEU)

Two Arithmetic Logic Units (ALUs) form the main computational part of the IEU. An early-finish-detect multi-cycle integer multiplier and a multi-cycle integer divider are also part of the IEU. Eight register windows and four sets of global registers are provided (normal, alternate, MMU and interrupt globals). The trap registers (UltraSPARC-II*i* supports five levels of traps) are part of the IEU.

Floating-Point Unit (FPU)

The separation of the execution units in the FPU allows UltraSPARC-II*i* to issue and execute two floating-point instructions per cycle. Source data and results data are stored in the 32-entry register file, where each entry can contain a 32- or 64-bit value. Most instructions are fully pipelined (throughput of one per cycle), have a latency of three, and are not affected by the precision of the operands (same latency for single or double precision).

The divide and square-root instructions are not pipelined. These take 12 cycles to execute in single precision (22 cycles in double precision) but they do not stall the processor. Instructions, following the divide/square root can be issued, executed, and retired to the register file before the divide/square root finishes. A precise exception model is maintained by synchronizing the floating-point pipe with the integer pipe and by predicting traps for long-latency operations.

Graphics Unit (GRU)

UltraSPARC-II*i* introduces a comprehensive set of graphics instructions (VIS) that provide industry-leading support for two-dimensional and three-dimensional image and video processing, image compression, audio processing, and similar functions. Sixteen-bit and 32-bit partitioned add, boolean, and compare are provided. Eight-bit and 16-bit partitioned multiplies are supported. Single cycle pixel distance, data alignment, packing and merge operations are all supported in the GRU.

Load/Store Unit (LSU)

The LSU is responsible for generating the virtual address of all loads and stores (including atomics and ASI loads), for accessing the data cache, for decoupling load misses from the pipeline through the load buffer, and for decoupling the stores through a store buffer. One load or one store can be issued per cycle. The store buffer can compress (or gather) multiple stores to the same 8 bytes into a single E-Cache access. The UPA64S and PCI control units can compress sequential 8-byte stores into burst transactions, to improve noncacheable store bandwidth.

Phase Locked Loops (PLL)

To minimize the clock skew at the system level UltraSPARC-IIi has PLLs for both the processor clock and the PCI clock. The internal PCI clock runs at twice the speed of the PCI interface clock. For details, see "Quick Pin Reference - Internal, SRAM, and UPA Clock Interface" beginning on page 294 and "Quick Pin Reference - PCI Clock Interface" beginning on page 296.

Signals

All external cache signals are of 2.6 V magnitude and exist only on the processor module. All other signals are 3.3 V LVTTL. The highest signal frequency from the module to the motherboard is 75 MHz. (unless the 100 MHz UPA64S interface is used), which allows economic motherboard design.

TECHNICAL CAPABILITIES

All performance specifications are for a 300 MHz processor, with 512 kB E-Cache.

SPEC Performance

SPECint95	10
SPECfp95	12

Newer compilers may improve SPECfp95 through use of software prefetch instructions.

One of the features of UltraSPARC-IIi is the superior performance of its integrated I/O, DRAM and UPA64S interfaces:

Memory Performance

Maximum E-Cache read bandwidth	1.2 GB/s
Maximum E-Cache write bandwidth	1.2 GB/s
Maximum DRAM random read bandwidth	350 MB/s
Maximum DRAM random write bandwidth	350 MB/s
Maximum same page read bandwidth	400 MB/s
Memcopy, from DRAM to DRAM	275 MB/s
Memcopy, from DRAM to UPA64S	550 MB/s

FP Vector

STREAM Copy (compiled)	200 MB/s
STREAM Scale (compiled)	210 MB/s
STREAM Add (compiled)	230 MB/s
STREAM Triad (compiled)	230 MB/s

Note that DRAM bandwidth is 1/3 to 1/4 greater than these numbers, since there is an initial DRAM read of the data locations that are used for store operations.

PCI Bandwidth

To DRAM from Processor PCI Bus (DMA)	66mhz, 32-bit	Random 64-byte Reads	132 MB/s
		Random 64-byte Writes	151 MB/s
To E-Cache from Processor PCI Bus (DMA)	66mhz, 32-bit	Random 64-byte Reads	163 MB/s
		Random 64-byte Writes	186 MB/s
From Processor to Processor PCI bus (PIO)	66mhz, 32-bit	64-byte writes	200 MB/s

All sustained DMA numbers are for a single device. Multiple devices on separate secondary buses can cause higher sustained bandwidths. In no case is the combined bandwidth from two secondary buses less than the peak bandwidth available from one bus. This is because of efficient internal arbitration between multiple events in the bus bridge.

UPA64S Bandwidth

From Processor, to UPA64S (PIO)	100mhz, 64-bit	Random 64-byte Writes	600 MB/s
		Compressed 8-byte Writes	800 MB/s

PCI Bandwidth with APB (33MHz Secondary Bus)

From Processor, to Secondary PCI Bus (PIO)	33mhz, 32-bit	64-byte Writes	124 MB/s
To DRAM from Secondary PCI Bus (DMA)	33mhz, 32-bit	Random 64-byte Reads	78 MB/s
		Random 64-byte Writes	124 MB/s

SIGNAL DESCRIPTIONS [1] [2]

Quick Pin Reference - External Cache (E-Cache) Interface

EDATA[63:0]	2.6 V	I/O	SRAM_CLK_A/B	E-Cache Data Bus; Connects UltraSPARC-IIi to the E-Cache data RAMs; clocked at 1/2 the processor clock rate
EDPAR[7:0]		I/O		E-Cache Data Parity; odd parity is driven or checked for all EDATA transfers; MSB corresponds to the MS byte of EDATA; clocked at 1/2 the processor clock rate
TDATA[15:0]		I/O		E-Cache Tag Data. Bits 15:14 carry the MEI I state; bits[13:0] carry the physical address bits [31:18]; allows a minimum cache size of 256k bytes; all TDATA bits are used, even when the E-Cache is more than 256 kilobytes; clocked at 1/2 the processor clock rate.
TPAR[1:0]		I/O		E-Cache Tag Parity; odd parity for TDATA[15:0]; TPAR[1] covers TDATA[15:8]; TPAR[0] covers TDATA[7:0]; clocked at 1/2 the processor clock rate
BYTEWE_L[7:0]		O		E-Cache Byte Write Enables; active low bit [0] controls EDATA[63:56]; bit 7 controls EDATA[7:0]; clocked at 1/2 the processor clock rate
ECAD[17:0]		O		E-Cache Data Address; corresponds to physical address [20:3]; allows a maximum 2 MB E-Cache; clocked at 1/2 the processor clock rate
ECAT[14:0]		O		E-Cache Tag Address; corresponds to physical address [20:6]; allows a maximum 2 MB E-Cache, with 64-byte lines; clocked at 1/2 the processor clock rate
DSYN_WR_L		O		E-Cache Data Write Enable; active low; clocked at 1/2 the processor clock rate
DOE_L		O		E-Cache Data Operation Enable; active low; asserted on all SRAM operations; clocked at 1/2 the processor clock rate
TSYN_WR_L		O		E-Cache Tag Write Enable; active low; clocked at 1/2 the processor clock rate
TOE_L		O		E-Cache Tag Operation Enable; active low; clocked at 1/2 the processor clock rate
ECACHE_22_MODE	3.3 V	I	Not Aligned Static (all modes)	Selects E-Cache 22 (1-tie high) or 222 mode (0-tie low). (2 cycle read pipeline, or 3 cycle read pipeline)

1. Unused inputs should be connected to the appropriate level.
2. Use approximately 10 kΩ resistors for pullups (unused) and 1 kΩ for pulldowns. Never tie a pin directly to a to a supply rail.

Quick Pin Reference - Internal, SRAM, and UPA Clock Interface

CLKA	PECL	I	See *Figure 3* and *Figure 4* for logical relation of clocks	Primary positive differential clock source to UltraSPARC-IIi; normally (in 2X mode) runs at 1/2 the internal clock rate; during test, when the PLL is bypassed, the full internal clock rate can be used
CLKB		I		Primary negative differential clock source to UltraSPARC-IIi; normally (in 2X mode) runs at 1/2 the internal clock rate; during test, when the PLL is bypassed, the full internal clock rate can be used
UPA_CLK_POS, UPA_CLK_NEG		I		Signals run at 1/3 frequency of the internal CPU clock; also used to drive the UPA64S; when the UPA64S interface is used these signals indicate to the processor which CLKA edge corresponds to a UPA_CLK_POS edge
SRAM_CLK_POS SRAM_CLK_NEG		I		Signals run at 1/2 the internal clock rate; also drive the SRAMs; they indicate to the processor which CLKA edges correspond to SRAM_CLK_POS clock edges
PLLBYPASS	3.3 V	I	Static Signal	Used during test to bypass PLL and PLL2; clock from differential receiver is directly passed to the clock tree; during PLLBYPASS, SRAM_CLK_POS and SRAM_CLK_NEG must be 1/2 the frequency of CLKA and CLKB; also during PLLBYPASS, UPA_CLK_POS and UPA_CLK_NEG must be 1/3 the frequency of CLKA and CLKB; during PLLBYPASS mode, PCI_REF_CLK must be 2X frequency of PCI_CLK
L5CLK	2.6 V	O	CLKA and CLKB	Internal level 5 clock that reflects the CPU clock; used to determine PLL lock or clock tree delay when in PLL bypass mode; may be disabled during normal operation

Clock Interface Timing Detail [1] [2] [3]

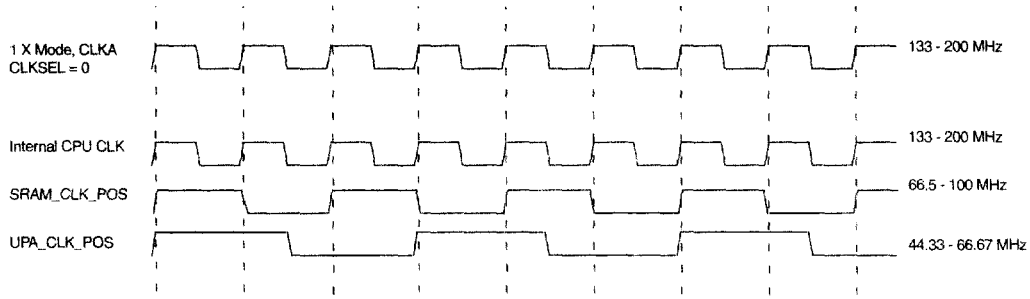


Figure 3. CLKA 1X Mode: Relation of CLKA to Internal, SRAM, and UPA Clocks

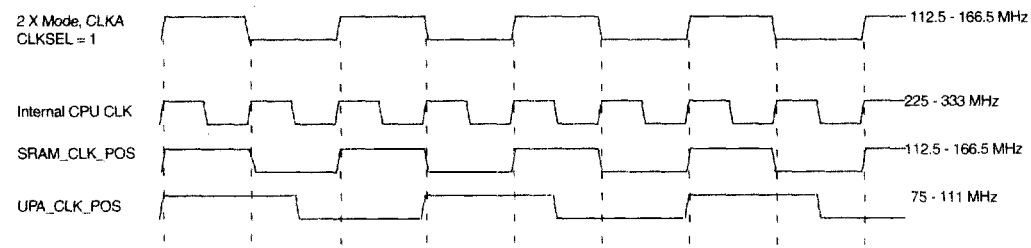


Figure 4. CLKA 2X Mode: Relation of CLKA to Internal, SRAM, and UPA Clock

1. See *Figure 28* and the table: Clock Skew on page 326 for skew requirements for CLKA.
2. Note that each CLK_POS has a complementary CLK_NEG not shown.
3. During PLLBYPASS, the Internal, SRAM, and UPA Clock relationships must be the same as in CLKA 1X Mode.

Quick Pin Reference - PCI Clock Interface

PCI_REF_CLK	3.3 V	I	See *Figure 5* and *Figure 6* for logical relations.	PCI reference clock; 40-66 MHz.
PCI_CLK	3.3 V	I		PCI clock, 66mhz; can be set to 33 MHz PCI interface if desired.
P2L5CLK	2.6 V	O	PCI_REF_CLK	Disabled during normal operation; internal level 5 clock that reflects the PCI clock and is used to determine PLL lock or clock tree delay when in PLLBYPASS mode; during PLLBYPASS mode, PCI_REF_CLK must be 2X frequency of PCI_CLK
PLLBYPASS				Refer to "Quick Pin Reference - Internal, SRAM, and UPA Clock Interface" on page 294

PCI Clock Timing [1] [2]

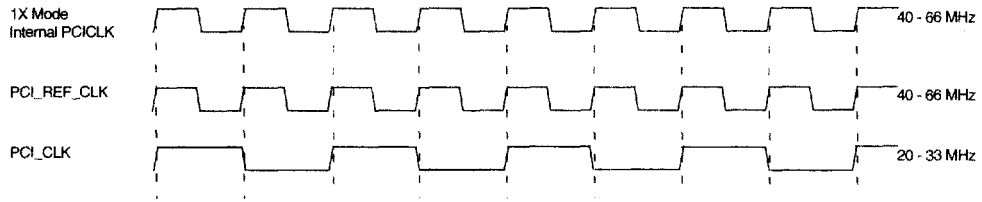


Figure 5. Relation Between PCI (1X Mode) Clocks [3]

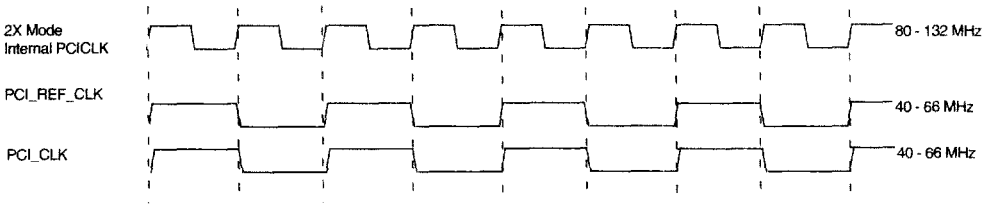


Figure 6. Relation Between PCI (2X Mode) Clocks [4] [5]

1. See *Figure 28* and table: Clock Skew on page 326 for skew requirements for PCI_REF_CLK.
2. During PLLBYPASS the PCI_CLK and PCI_REF_CLK relationships must be the same as for PCI 1X Mode.
3. *Figure 5* applies to the PCI bus clock between 20-33 MHz, which must be in 1X mode.
4. *Figure 6* (and 2X mode) applies when the bus is run from 40-66 MHz.
5. Refer to the table: Clock Skew on page 326 for permissible skew between PCI_REF_CLK and PCI_CLK. It is recommended that the system designer supplies PCI_REF_CLK directly from the PCI_CLK signal for 2X mode operation – see *Figure 6*. Skew between PCI_CLK and PCI_REF_CLK must be minimized; the required setup time is: $t_{SUeff} = (3ns + t_{SKEW\_POS})$

Quick Pin Reference - JTAG/Debug Interface

TDI	3.3 V	I	Not aligned	IEEE 1149 test data input; pin internally pulled to logic 1 when not driven
TCK		I		IEEE 1149 test clock input; pin must always be held at logic 1 or logic 0 if not connected to a clock source
TMS		I		IEEE 1149 test mode select input; pin internally pulled to logic 1 if not driven
TRST_L		I		IEEE 1149 test reset input (active low); pin internally pulled to logic 1 if not driven
RAM_TEST		I		When asserted this pin forces the processor into SRAM test mode allowing direct access to the cache SRAMs for memory testing
ITB_TEST_MODE		I		Enables a special SRAM mode for testing the ITB megacell; pull to ground using a 10.7 kΩ, 1% resistor
EXT_EVENT		I		Signal used to indicate that the clock should be stopped; debug signal set inactive to logic 0 on production systems
TDO	2.6 V	O	Not aligned	IEEE 1149 test data output; tri-state signal driven only when the TAP controller is in the shift-DR state
PMO		O		Used for on-chip process monitors; reserved for IC manufacturing only
TEMP_SEN[1:0]	N/A	O		Defines scale end points of the processor temperature sense element on the module; reserved for IC manufacturing only

Quick Pin Reference - Initialization Interface

P_RESET_L	3.3 V	I	Not Aligned	For non power-on resets (debug); asynchronous assertion and de-assertion; active low
X_RESET_L		I		Driven to signal XIR traps (debug); acts as non-maskable interrupt; asynchronous assertion and de-assertion; active low
SYS_RESET_L		I		Driven for power-on resets (POR); asynchronous assertion and de-assertion; active low[1]
RST_L		O		Resets PCI subsystem; Asynchronous assertion and monotonic deassertion; also used for UPA64S reset
RMTV_SEL		I		Red Mode Trap Vector Select; pull up if alternate PC-compatible boot vector is required
CLKSEL		I		Pullup to enable the 2x function of the CLKA/B PLL; E-Cache interface still works at 1/2 the internal processor clock rate
EPD	2.6 V	O		Asserted when UltraSPARC-IIi is in clock shutdown mode; use P_RESET_L to re-start

1. SYS_RESET_L must be a clean indication that 3.3 V, 5 V, etc. are stable and within specification. No anomalies may be present, beginning when the power supplies are turned on and extending until the signals are within specification. When signals are within specification, the power supply can transition monotonically to 3.3 V.

Quick Pin Reference - PCI interface

AD[31:0]	3.3 V (All)	I/O	PCI_CLK	Address/Data; multiplexed on same PCI pins.
CBE_L[3:0]		I/O		Bus Command and Byte Enables; multiplexed on same PCI pins
PAR		I/O		Parity; even parity across AD[31:0] and CBE_L[3:0]
DEVSEL_L		STS [1]		Device Select. Indicates the driving device has decoded the address of the target of the current access; as input, indicates whether any device has been selected
FRAME_L		STS		Cycle Frame; driven by current master to indicate beginning and end of an access
REQ_L[3:0]		I		Request; indicates to arbiter that an external device requires use of the bus
GNT_L[3:0]		T/S [2]		Grant; indicates to device that bus access has been granted.
IRDY_L		STS		Initiator Ready; indicates the bus master's ability to complete the current data phase
TRDY_L		STS		Target Ready; indicates the selected device's ability to complete the current data phase
PERR_L		STS		Parity error; reports data parity errors
SERR_L		O/D		System Error; reports address parity errors, data parity errors on special cycles, or any other catastrophic PCI errors
STOP_L		STS		Stop; indicates that the current target is requesting the master to stop the current transaction

1. Sustained Tri-State. STS is an active low tri -state signal owned and driven by one and only one agent at a time. The agent that drives an STS pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an STS signal any sooner than one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it, and must be provided by the motherboard or module.
2. Tri-State Output.

Quick Pin Reference - Interrupt Interface

SB_DRAIN	3.3 V	O	PCI_CLK	Store Buffer Drain. sampled at a 66 MHz PCI_CLK edge; asserted after Interrupts, or by software, to cause outstanding DMA writes to be flushed from buffers
SB_EMPTY[1:0]		I		Store Buffer Empty; sampled at 66 MHz PCI_CLK edge. asserted when external APB PCI bus bridge indicates that all DMA writes queued before the assertion of SB_DRAIN have left the bus bridge;
INT_NUM[5:0]		I		Interrupt Number; sampled at 66 MHz PCI_CLK edge; encoded interrupt request

Quick Pin Reference - Memory and Transceiver Interface

MEM_WE_L	3.3 V (All)	O	CLKA/B	Memory Write Enable; active low
MEM_CAS_L[1:0]		O		Memory Column Address Strobe; active low
MEM_RAST_L[3:0]		O		Memory Row Address Strobe Top; active low
MEM_RASB_L[3:0]		O		Memory Row Address Strobe Bottom, active low
MEM_DATA[71:0]		I/O		Memory Data; bits [71:64] are ECC bits
MEM_ADDR[12:0]		O		Memory Address, row and column (10 and 11 bit column support)
XCVR_OEA_L		O		Transceiver Output Enable A; active low
XCVR_OEB_L		O		Transceiver Output Enable B; active low
XCVR_SEL_L		O		Transceiver Select; active low; picks high or low half of read data
XCVR_WR_CNTL[1:0]		O		Transceiver Write Control; controls lock enables on internal registers
XCVR_RD_CNTL[1:0]		O		Transceiver Read Control; control clock enables on internal registers
XCVR_CLK[2:0]		O		Transceiver Clock; all data and control signals are registered by these clocks; multiple outputs to minimize loading effects of 6 transceivers

Quick Pin Reference - UPA64S Interface

S_REPLY[2:0]	3.3 V	O	UPA_CLK_POS/NEG	S Reply; encoded command indicates arrival of write data on MEM_DATA[63:0], or command to drive MEM_DATA[63:0] with read data
P_REPLY[1:0]		I		P Reply; encoded command that indicates ability consumption of prior write, or ability to provide read data
SYSADR[28:0]		I/O[1]		System Address; sends 2 cycle address packet to UPA64S slave, or provides internal state debug information
ADR_VLD		O		Address Valid; asserted during first cycle of two cycle address packet

1. *Not all of SYSADR[28:0] is bidirectional, since SYSADR[14:0] is I/O but SYSADR[28:15] is output only. SYSADR[14:0] is used as an input during* RAM_TEST.

PRODUCT SYSTEM AND SUBSYSTEMS

An UltraSPARC-IIi Reference Platform

A reference platform has been developed to illustrate UltraSPARC-IIi operation. This platform is illustrated in the schematic block diagram of *Figure 7* and detailed in the following description:.

Hardware

This model assumes CPU and SRAM for the E-Cache are provided on the same module, to keep the high-speed E-Cache interface in a controlled electrical environment and away from the motherboard.

This standard module uses five, 64 K x 18 register-latch SRAMs, to provide a 512-kilobyte E-Cache.

The module provides support for two standard, 33 MHz, 32-bit PCI buses, along with a 66 MHz, 32-bit PCI interface to a bus bridge ASIC, for example, the Advanced PCI Bridge (APB), SME2411.

Memory

- Four DIMM pairs for up to 256 Megabytes, using 168-pin JEDEC DIMMs, with 16-Megabit DRAM. Up to 1 Gigabyte, using 64-Megabit DRAM
- 144-bit DRAM data bus with 8-bit ECC on each 64 bits of data

Graphics

- PCI add-in card, or custom UPA64S solution

PCI Buses

- Three PCI buses, all compatible with the existing PCI 2.1 standard:
  - Primary: One 66 MHz, 32-bit bus from UltraSPARC-IIi to APB; Note that multiple APBs can be used for multiplying PCI connectivity
  - Secondary: Two 33 MHz, 32-bit busses from the APB.
- PCI clocks asynchronous with processor clock

Block Diagram of the Reference Platform

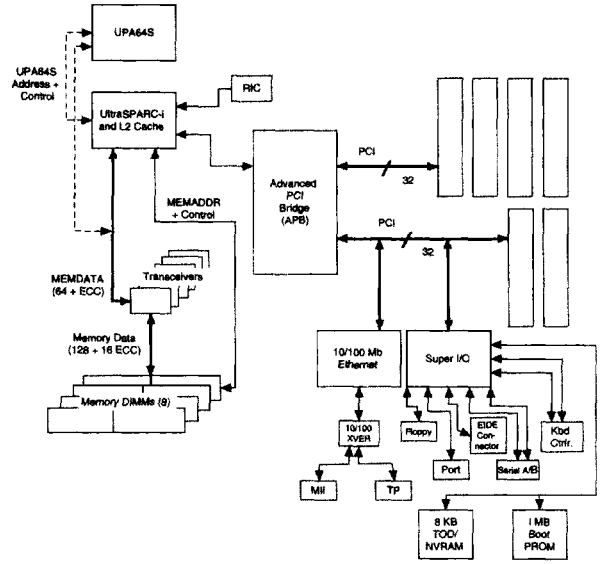


Figure 7. Overview of UltraSPARC-IIi Reference Platform

Transceivers

The Texas Instruments SN74ALVC16268 is a bidirectional registered 12-bit-to-24-bit bus exchanger, with 3-state outputs.

The transceiver transfers data bidirectionally between the 72-bit UltraSPARC-IIi memory data bus, and the 144-bit DIMM memory data bus. The DIMMs cycle data in EDO mode at 37.5 MHz maximum frequency – a period of 26.5 ns.

The transceiver has bus-hold on data inputs, eliminating the need for external pullup resistors. It is available in 56-pin Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) packages.

The ports connected to the DIMMs include the equivalent of 26Ω series resistors, to make external series termination resistors unneccessary.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate CLKEN inputs are low. All control inputs, including the CLK inputs, are driven by UltraSPARC-IIi.

RIC Chip

The RIC Chip (SME2210) supports the system resets, system interrupts, system scan, and system clock control functions. It's features include:

- Support for resets from power supply, reset buttons, and scan
- Concentration of all of the interrupts; it sends interrupt numbers to the UltraSPARC-IIi
- Direction of SCAN inputs and outputs through scan chains

UPA64S

UPA64S is a custom 64-bit slave interface for graphics or similar subsystems. Transfers to and from the UPA64S interface are fully synchronous, since UPA64S receives a PECL clock that is aligned with the processor's clock. The processor transfers data on clock edges that correspond to the UPA64S clock edges. This interface runs at 1/3 of the processor clock rate, that is up to 100 MHz.

Memory

The following are the major features of the DRAM modules utilized in UltraSPARC-IIi memory:

- JEDEC and industry standard ECC pinout in a 168-pin, dual-in-line memory module (DIMM)
- High performance CMOS silicon gate process
- Single +3.3V ± 0.3 V power supply
- All device pins are 3.3 V compatible
- Low power, 9 mW standby; 1,800 mW active, typical
- Refresh modes: $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR)
- All inputs are buffered except $\overline{\text{RAS}}$
- 2,048-cycle refresh distributed across 32 ms
- Extended Data Out (EDO) access cycles

The UltraSPARC-IIi memory design is built with JEDEC standard 168-pin DIMMs. The memory bus is 144 bits wide. RAS and CAS signals are provided that support a maximum of eight 8 - 128 megabyte DIMMs. A mode that supports 11-bit column addresses for 16M X 4, 64 megabit DRAMs allows a maximum of four 8 - 256 megabyte DIMMs. The memory bus width requires that the DIMMs be populated in pairs at a time. Consequently the minimum memory configuration contains 16 megabytes and the maximum memory configuration contains 1 gigabyte.

These DIMMs are available from many vendors. A composite specification was made considering typical vendor specifications. When the UltraSPARC-IIi is programmed according to the *Programmer's Reference Manual* for a particular frequency and DIMM loading combination, it generates signals that meet this composite specification, if the electrical and topological motherboard layout requirements are met.

Memory Model for Reference Platform

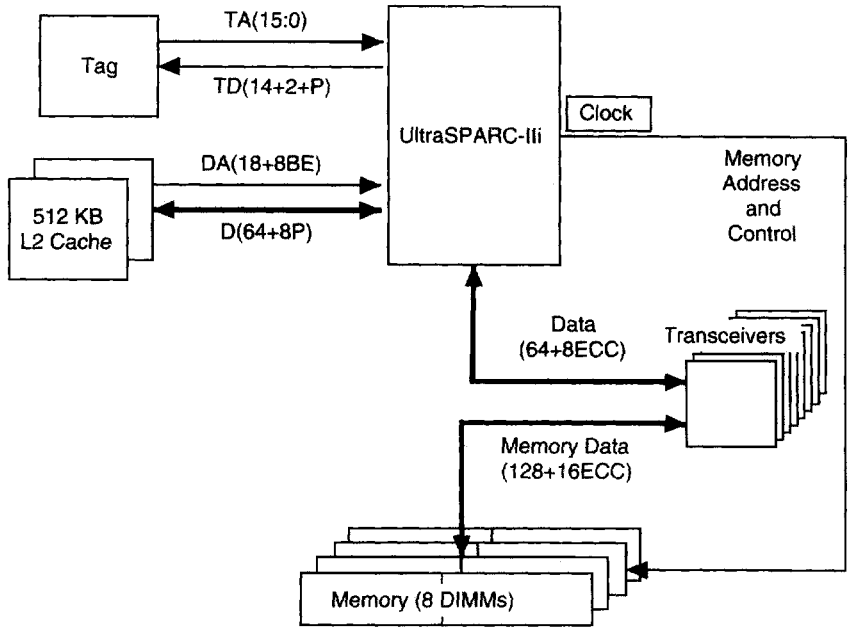


Figure 8. UltraSPARC-IIi Memory: Simplified Block Diagram

Figure 8 shows how memory is connected to, and controlled by, the UltraSPARC-IIi. The memory DIMMs are arranged on a 144-bit bus to allow an entire cache line to be fetched in four CAS accesses.

UltraSPARC-IIi implements ECC, with single-bit correction and multi-bit detection of errors, for all memory data transfers.

PCI Buses for UltraSPARC-IIi and Advanced PCI Bridge

Figure 9 shows an example of the connection of an external PCI subsystem.

The interface from UltraSPARC-IIi with its I/O subsystems is a 32-bit PCI bus, which can run at either 33 or 66 MHz. UltraSPARC-IIi internal PLLs allow slower PCI bus clock rates, down to 20 MHz or 40 MHz for each range respectively. This allows use of more PCI targets than the 2.1 specification permits for full-speed operation. However, the PCI arbiters on UltraSPARC-IIi and APB only support four master requests. The Advanced PCI Bridge (APB) allows external arbiters on the secondary buses.

The UltraSPARC-IIi PCI interface runs at 3.3 V only. To support 5 V PCI cards, the Advanced PCI Bridge (APB) must be used, which also provides expansion from one 66 MHz 32-bit PCI bus, to two 32-bit 33 MHz PCI buses. APB provides up to 64-byte write posting and data prefetching, so that the delivered throughput can be higher than a single 33 MHz bus could provide.

The secondary PCI buses have:

- 3.3 Volt operation and signalling, but are compatible with the PCI 5 V signalling environment definition.
- 32-bit data bus
- Compatibility with the PCI Rev. 2.1 Specification
- Support for up to four master devices

Interrupts are not routed through the APB. A separate Drain/Empty protocol is used to guarantee that all DMA writes temporally complete to memory, prior to receipt of an interrupt, and thus before a potential processor trap as a result of that interrupt.

The Primary bus, which can be used with or without the Advanced PCI Bridge, has the same characteristics discussed above, except it can run in the 20-33 MHz or the 40-66 MHz range. UltraSPARC-IIi operates internally at twice the external PCI clock frequency, that is, up to 132 MHz. This helps reduce the latency involved in crossing clock domains and manipulating state machines.

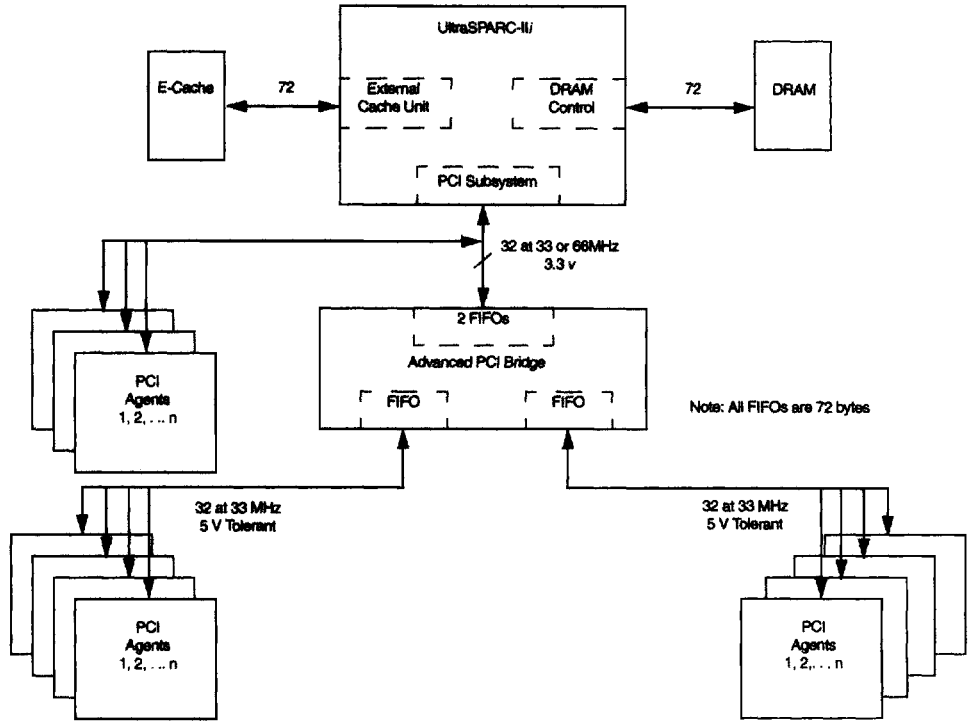


Figure 9. Example of Externally-Connected PCI Subsystem

UPA64S interface (FFB)

UPA64S is a slave-only interface protocol used, for instance, by proprietary graphics boards. It can be used for any high bandwidth control or data transfers between the processor and a dedicated subsystem.

UltraSPARC-IIi drives the SYSADR (system address), ADR_VLD (address valid) signals, the P_REPLY and S_REPLY handshakes, and reset (RST_L) to the UPA64S. The data bus (64 bits out of 72) is shared with the transceiver connection to the UltraSPARC-IIi. The internal memory controller of the UltraSPARC-IIi transfers data aligned to processor clocks, but guarantees that UPA64S transfers appear aligned to the UPA64S clock. In other words, these are valid for 3 processor clock cycles, and only sampled on the UPA clock edge when UPA64S is driving.

Note that, although the transceivers only cycle the 72-bit MEMDATA at 75 MHz maximum, the FFB/UPA64S cycle this bus at up to 100 MHz.

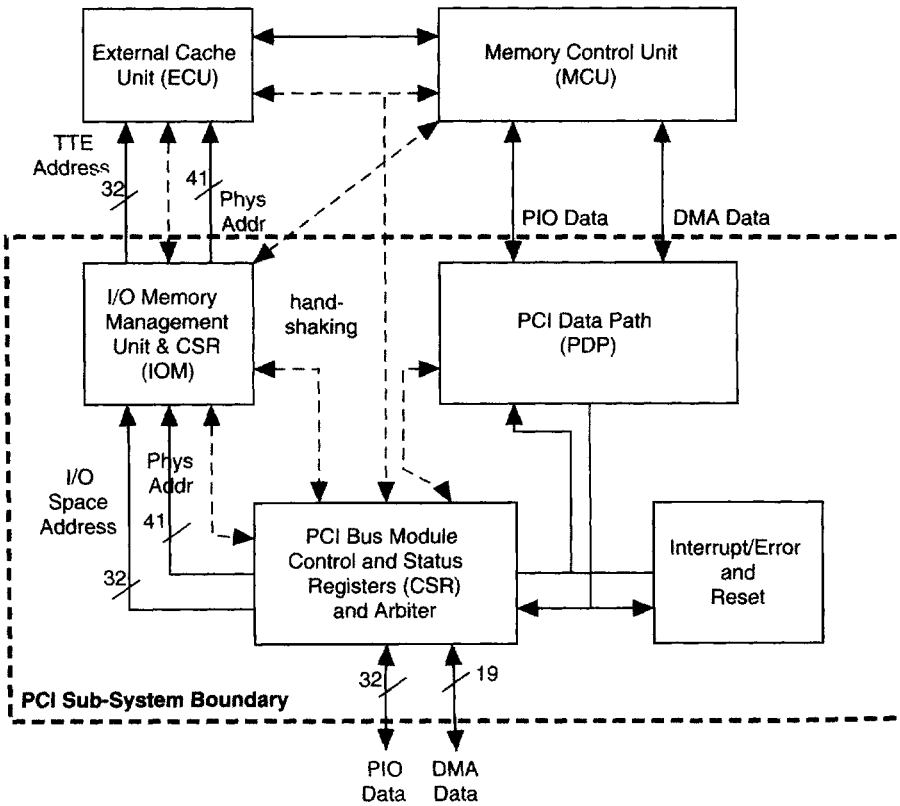


Figure 10. UltraSPARC-II*i* PCI Sub-System

TIMING DIAGRAMS

E-Cache Read Hit in 2-2 Mode

Three consecutive reads are shown hitting the E-Cache in *Figure 11*. The control signal (TOE_L) and the address for the tag read (ECAT) are shown in transition shortly after the rising edge of the clock -- along with the control signal DOE_L and address for the data (ECAD). One cycle later, the data for both the tag read and the data read is back at the pins of the CPU. The data arrives shortly before the next rising edge, meeting the set-up time and clock skew requirements. The data bus is eight bytes wide so the data RAM is accessed twice for each data read request. The most critical eight bytes (D0_data1) of data are returned first followed by the next eight bytes (D0_data2) in the subsequent clock cycle. For each read request, both the tag address and the tag data are stable for 2 clock cycles, but the data address and data read changes every cycle. The reads are fully pipelined to allow full throughput.

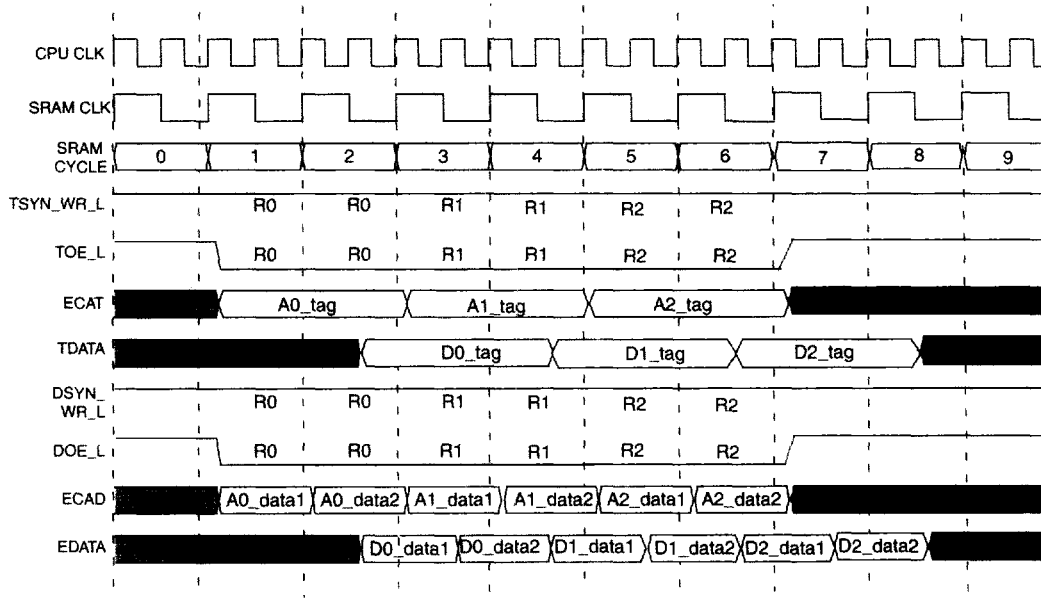


Figure 11. Timing for E-Cache Read Hit (2-2 mode)

E-Cache Write Hit to M State Line in 2-2 Mode

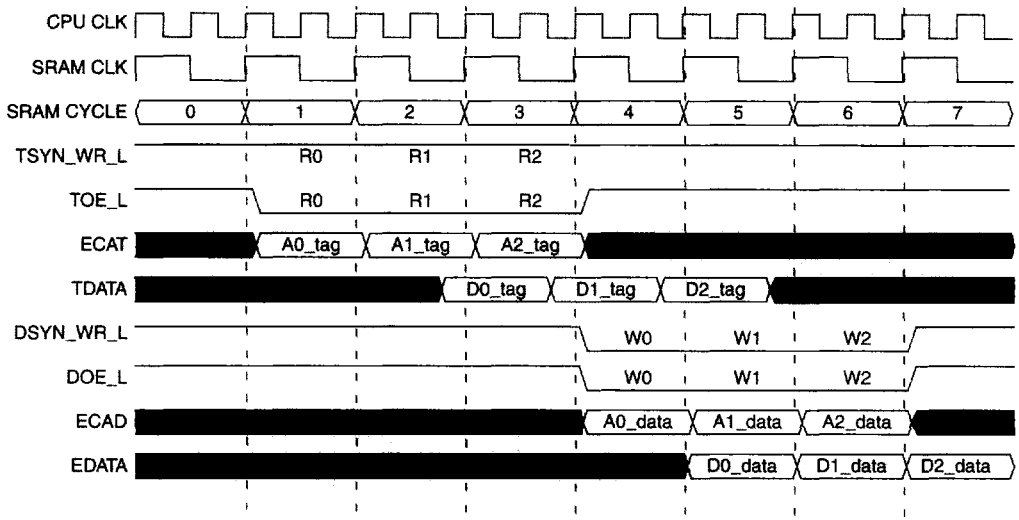


Figure 12. Timing for E-Cache Write Hit to M State Line (2-2 mode)

Figure 12 shows the 2-2 timing mode for three consecutive write hits to the M state lines. Access to the first tag (D0_tag) is started by asserting TOE_L and by sending the tag address (A0_tag). In the cycle after the tag data (D0_tag) comes back, UltraSPARC-II*i* determines that the access is a hit and that the line is in Modified (M) state. In the next clock, a request is made to write the data. The data address is presented on the ECAD pins in the cycle after the request (cycle 4 for W0) and the data is sent in the following cycle (cycle 5). Systems running in 2-2 mode incur no read-to-write bus turnaround penalty.

Read-to-Write Transition in 2-2 Mode

Figure 13 shows the read-to-write transition for 2-2 mode. Three reads are followed by two writes and two tag updates. Since the tag and data appear in the same cycle as the write, there is no turnaround penalty for reads followed by writes in 2-2 mode.

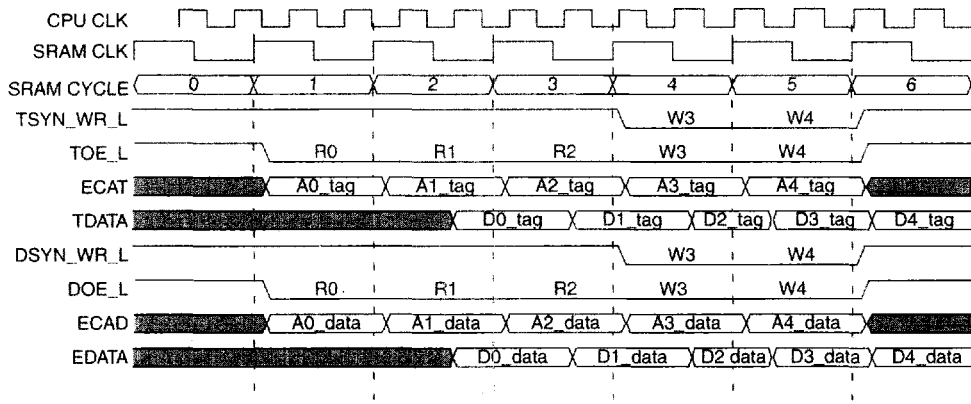


Figure 13. No Turn-Around Penalty: Read-to-Write Transition (2-2 mode)

E-Cache Read Hit In 2-2-2 Mode

Figure 14 shows the 2-2-2 mode timing for three consecutive reads that hit the E-cache. The control signal (TOE_L) and the address for the tag read (ECAT) as well as the control signal (DOE_L) and the address for the data (ECAD) are shown to change state shortly after the rising edge of clock cycle 1. Two cycles later the data from the tag RAM and the critical eight bytes (D0_data1) from the data RAM are back at the pins of the CPU, just before the rising edge of cycle 4. One cycle later the next eight bytes of data (D0_data2) returns from the data RAM. Note that, for each read request, the tag address and tag data are stable for two clock cycles, but the data address and data read changes every cycle. This is because the data RAM is accessed twice for each read request. Two requests are made before the data of the first read request returns.

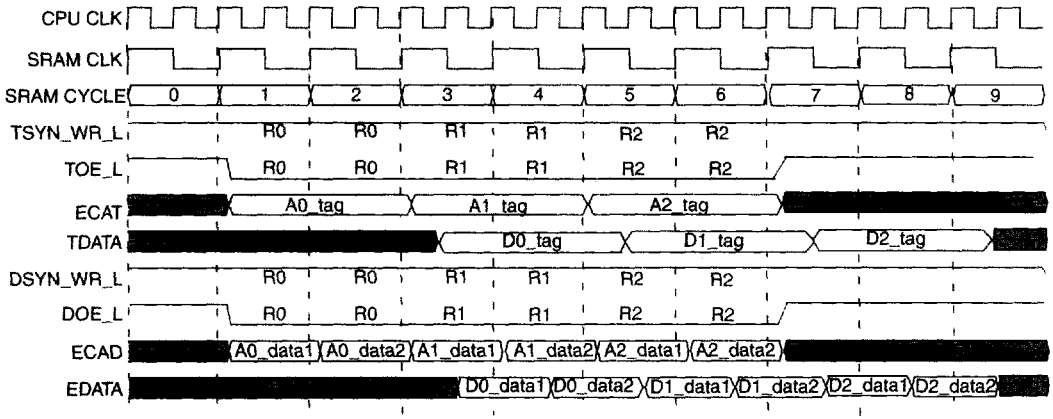


Figure 14. Timing for E-Cache Read Hit (2-2-2 mode)

E-Cache Write Hits In 2-2-2 Mode

Figure 15 shows the 2-2-2 mode timing for six consecutive write hits to M state lines. Access to the first tag (D0_tag) is started by asserting the tag address (A0_tag) in clock cycle 1. The tag data comes back two cycles later in cycle 3. In clock cycle 4, UltraSPARC-IIi determines that the access is a hit and that the line is in Modified (M) state. In the next cycle, a request is made to write the data by asserting the data address (A0_data). The write data (D0_data) is sent in the next cycle. Separating the address and data by one cycle reduces the turn-around penalty when reads are immediately followed by writes (*Figure 17*).

If the line is in M state, then the tag port is available for the tag check of a more recent store during the data write cycle. In *Figure 15* the store buffer is empty when the first request is made, which is why there is no overlap between the tag accesses and the write accesses. In normal operation, if the line is in M state, the tag access for one write can be done in parallel with the data write step of a previous write phase. In *Figure 15*, clock cycles 5 and 6 show overlap of two previous data writes (W0, W1) and tag accesses for two more recent stores (R4 and R5).

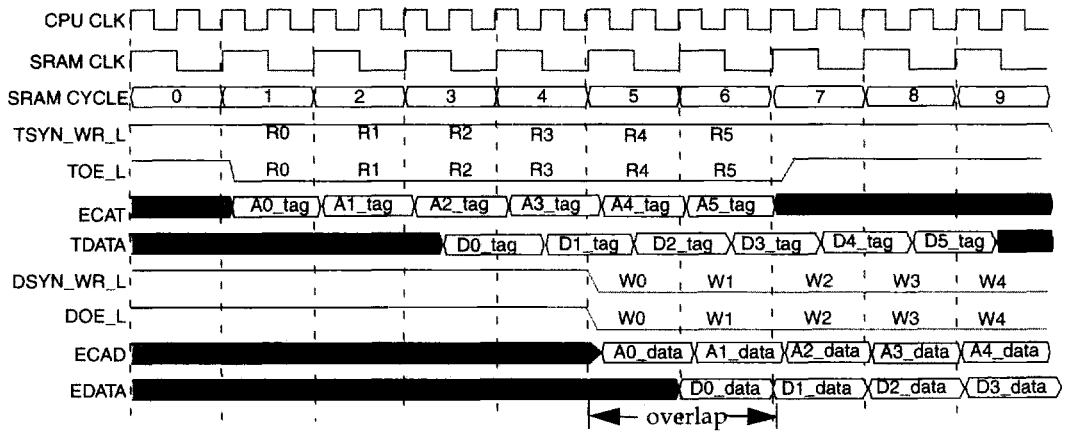


Figure 15. Timing for E-Cache Write Hit to M State Line (2-2-2 mode)

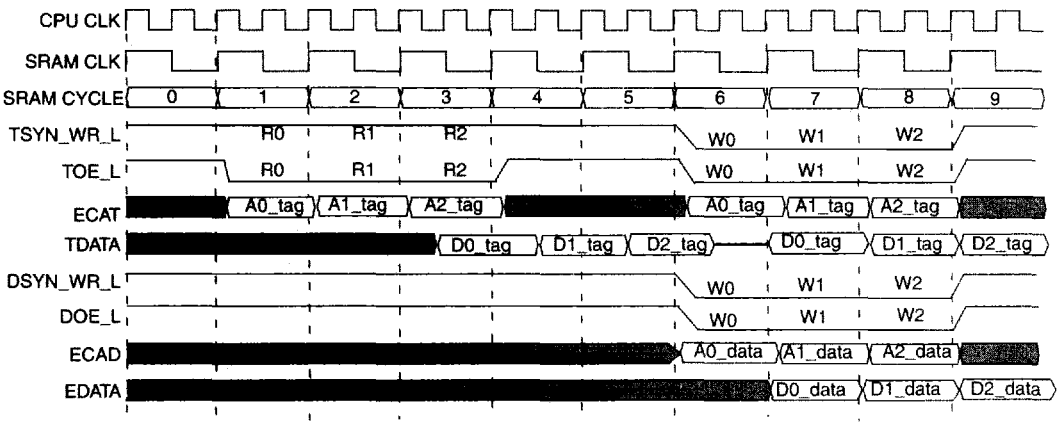


Figure 16. Timing for E-Cache Writes with E-to-M State Transition (2-2-2 mode)

Figure 16 shows the timing of E-Cache writes with E-to-M state transition. The tag checks in clock cycles 3, 4 and 5 found the line in Exclusive (E) state. The tag is updated to Modified (M) state at the same time data is written in clocks 6, 7 and 8, respectively.

E-Cache Read Followed by E-Cache Write In 2-2-2 Mode

Figure 17 shows the two-cycle read-to-write turnaround penalty for 2-2-2 mode. The figure shows two reads followed by two writes and two tag updates. The data for the second read (R1) is available in clock cycles 5 and 6. UltraSPARC-II*i* cannot assert the write address in clock cycle 6 because electrical considerations force an extra dead cycle while the E-cache data bus driver is switched from the SRAMs to UltraSPARC-II*i*. The address for the first write is asserted in clock cycle 7. This causes a two-cycle turnaround penalty. The two-cycle penalty applies to both tag accesses and data accesses because there are two stalled cycles between A1_tag and A2_tag, as well as between A1_data and A2_data.

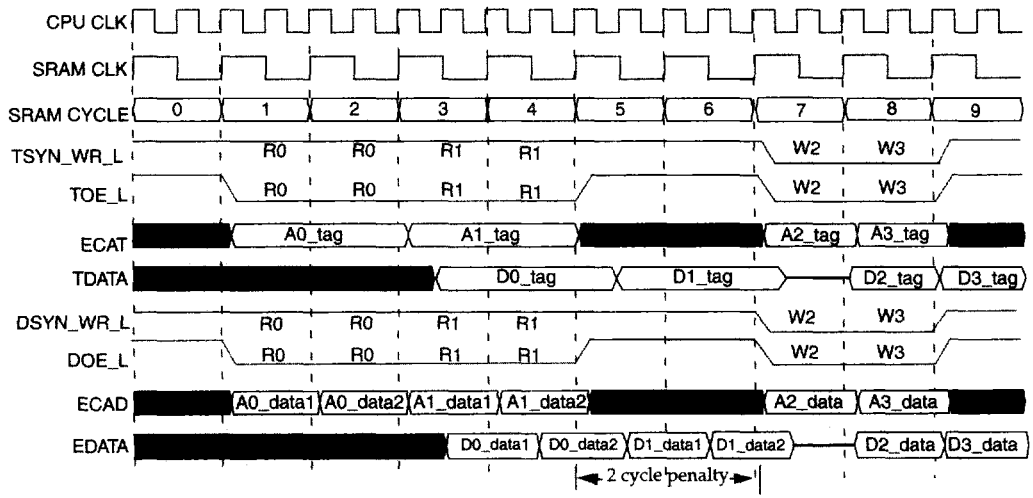


Figure 17. Read -to-Write Turnaround Penalty (2-2-2 Mode Only) for E-Cache Read Hit (2-2-2 mode)

DRAM Timing

Dram Write

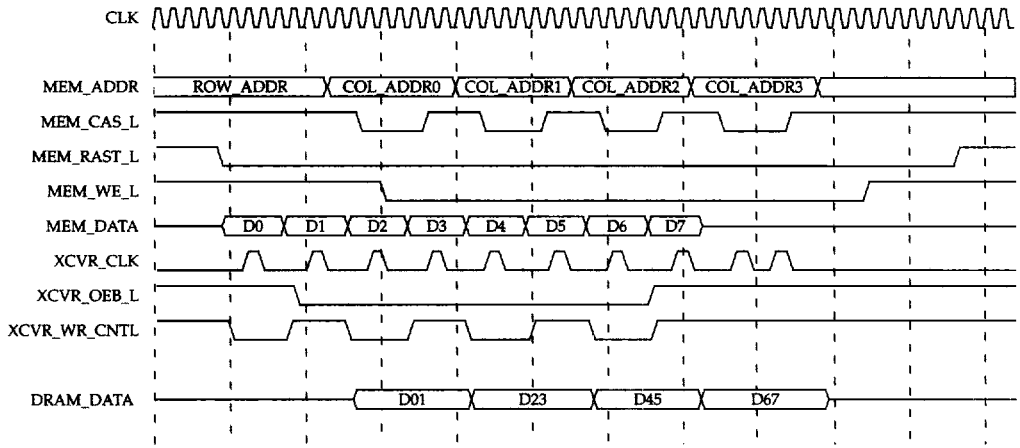


Figure 18. DRAM Write Timing Diagram

Figure 18 shows the timing of a DRAM write.

DRAM Read

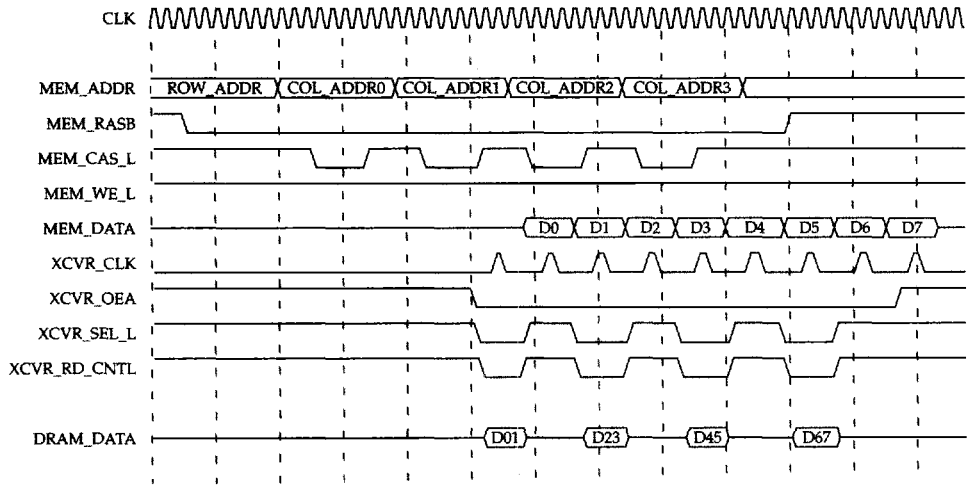


Figure 19. DRAM Read Timing Diagram

Figure 19 shows the timing diagram for a DRAM read operation.

PCI Timing Information

PCI Read

Figure 20 below illustrates a PCI read transaction. For more information, see the relevant section of the PCI Specification.

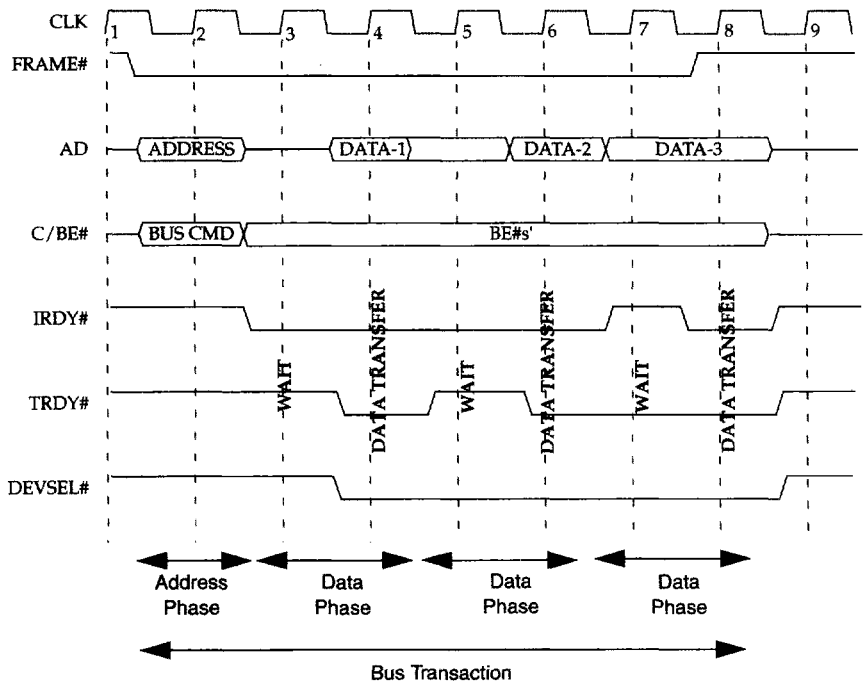


Figure 20. Basic PCI Read Operation

PCI Write

Figure 21 below illustrates a PCI write transaction. For more information, see the relevant section of the PCI Specification.

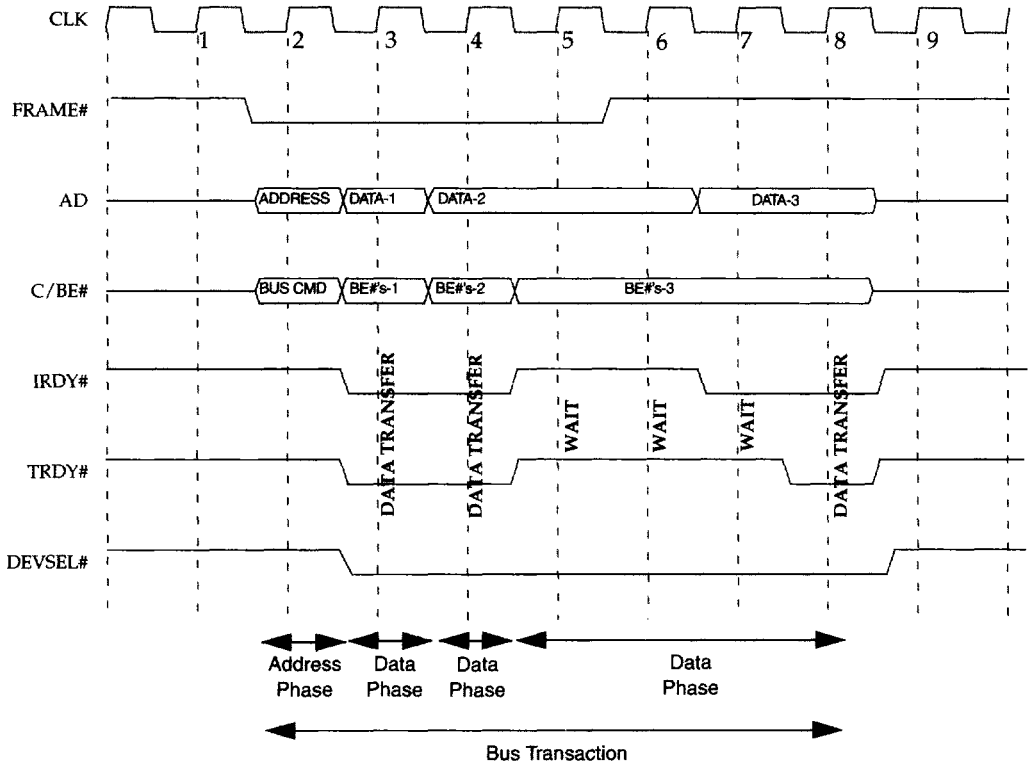


Figure 21. Basic PCI Write Operation

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings[1]

VDD_C	Supply voltage range (2.6v)	0 to 3.2	V
VDDPLL	Supply voltage range (2.6v)	0 to 3.2	V
VDDPECL	Supply voltage range (2.6v)	0 to 3.2	V
VDDPLL2	Supply voltage range (2.6v)	0 to 3.2	V
VDD_O	Supply voltage range (2.6v)	0 to 3.2	V
VDD_H	Supply voltage range (3.3v)	0 to 4.0	V
VDD_{DIFF}	Supply voltage difference: VDD_C or VDD_O -VDD_H	-1.4 to 2.9	V
V_I	Input voltage range	-0.5 to VDD + 0.5	V
V_O	Output voltage range	-0.5 to VDD + 0.5	V
I_{IK}	Input clamp current (V_I < 0 or V_I > VDD)[2]	20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > VDD)	50	mA
	Current into any output in the low state	50	mA
T_{STG}	Storage temperature	-40 to 150	C

1. Operation of the device at values in excess of those listed above may result in degradation or destruction of the device. All voltages are defined with respect to Vss. Functional operation of the device is not implied at these or any other conditions beyond those indicated under "Recommended Operating Conditions." Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Do not clock while subject to these conditions. High static voltages or electric fields should be avoided.
2. Thermal stress should be minimized by turning power off if the regulated 2.6 V power fails.

Recommended Operating Conditions

VDD_C	Supply voltage (2.6 v)[1] (±3%)		2.52	2.6	2.68	V
VDDPLL	Supply voltage (2.6 v) (±3%)		2.52	2.6	2.68	V
VDDPECL	Supply voltage (2.6 v) (±3%)		2.52	2.6	2.68	V
VDDPLL2	Supply voltage (2.6 v) (±3%)		2.52	2.6	2.68	V
VDD_O	Supply voltage (2.6v) (±3%)		2.52	2.6	2.68	V
VDD_H	Supply voltage (3.3v) (-3%+5%)		3.2	3.3	3.465	V
VSS_C	Core ground		–	0	–	V
VSS_O	IO ground		–	0	–	V
V_{IH}	High-level input voltage	2.6 V signals	2.0	–	VDD_C + 0.3	V
		3.3 V non-PCI signals	2.4	–	VDD_H + 0.3	V
		3.3 V PCI signals	0.5(VDD_H)		VDD_H+0.5	V

Recommended Operating Conditions (Continued)

V_{IL}	Low-level input voltage	2.6 v signals	-0.3	–	0.8	V
		3.3 V non-PCI signals	-0.3	–	0.8	V
		3.3 V PCI signals	-0.5	-	$0.3VDD_H$	V
V_{CM}	DC Common Mode Input Range	PECL clocks see *Figure 27*	VDD_{PECL} - 0.85	VDD_{PECL} - 0.5	VDD_{PECL} - 0.15	V
V_{DIFF}	Minimum Input Signal Amplitude	PECL clocks see *Figure 27*	± 0.155	±0.35		V
I_{OH}	High-level output current			-4.0		mA
I_{OL}	Low-level output current			8.0		mA
T_J	Operating junction temperature		–	–	105	C
T_C	Operating case temperature		0	–	85	C

1. Even with the recommended bypass capacitance, there will be some dv/dt due to dynamic load variation. This 0-20Mhz dv/dt may be up to 100mV and is not included in the VDD requirements.

DC Characteristics

V_{OH}	High-level output voltage	2.6 V signals	VDD_O = Min, I_{OH} = Max	1.65	–	–	V
		3.3 V non-PCI signals	VDD_H = Min, I_{OH} = Max	2.0	–	–	V
		3.3 V PCI signals	Iout = -500 µA	$0.9VDD_H$	-	-	V
V_{OL}	Low-level output voltage	2.6 V signals	VDD_O = Min, I_{OL} = Max	–	–	1.15	V
		3.3 V non-PCI signals	VDD_H = Min, I_{OL} = Max	–	–	0.8	V
		3.3v PCI signals	Iout = 1500 µA	-	-	$0.1VDD_H$	V
V_{IH}	High-level input voltage	2.6 V signals	VDD_C = Max	1.65	–	–	V
		PECL signals	VDD_C = Max	VDDPLL-0.345	–	–	V
		3.3 V non-PCI signals	VDD_H = Max	2.0	–	–	V
		3.3v PCI signals	VDD_H = Max	$0.5VDD_H$	-	$0.5 + VDD_H$	V
V_{IL}	Low-level input voltage	2.6 V signals	VDD_C = Min	–	–	1.15	V
		PECL signals	VDD_C = Min	–	–	VDDPLL - 0.655	V
		3.3 V non-PCI signals	VDD_H = Min	–	–	0.8	V
		3.3v PCI signals	VDD_H = Min	-0.5	-	$0.3VDD_H$	V
$I_{DD(2.6V)}$	2.6 V Supply current		VDD_C, VDD_O & VDD_H = Max, freq = 300MHz	–	8	11	A
$I_{DD(3.3V)}$	3.3V Supply current		VDD_C, VDD_O & VDD_H = Max, freq = 300MHz	–	2	3	A

DC Characteristics (Continued)

I_{DDQ}	Quiescent supply current	VDD_C, VDD_O & VDD_H = Max, Freq = 0 MHz, $V_I = V_{SS}$ or VDD	–	–	TBD	mA
I_{OZ}	High-impedance output current [1] (Outputs without pull-ups)	V_{DD} = Max, V_O = 2.4 V	–	–	20	µA
		V_{DD} = Max, V_O = 0.4 V	–	–	-20	µA
	High-impedance output current (Outputs with pull-ups)	V_{DD} = Max, $V_O = V_{SS}$ to V_{DD}	–	–	250	µA
I_I	Input current (inputs without pull-ups)	V_{DD} = Max, $V_I = V_{SS}$ to V_{DD}	-20	–	20	µA
	Input current (inputs with pull-ups)	V_{DD} = Max, $V_I = V_{SS}$ to V_{DD}	–	–	-250	µA
C_I	Input capacitance [2]		–	5	–	pF
C_O	Output capacitance		–	10	–	pF

1. Only bidirectional lines can be tri-stated; output-only lines cannot be tri-stated. All bidirectional lines are tri-stated when SYS_RESET_L or P_RESET_L is held LOW and RAM_TEST is held high.
2. This specification is provided as an aid to board design but is not assured during manufacturing testing.

AC Characteristics - Signal Timing (Except JTAG) [1] [2]

t_{SU}	Input setup time [3] to CLK	2.6 v signals		1.38	–	ns
		3.3 V non-PCI interface		1.38	–	ns
		3.3v PCI interface		4.3	–	ns
t_H	Input hold time to CLK	2.6 v signals		1.07	–	ns
		3.3 V non-PCI interface		1.07	–	ns
		3.3v PCI interface		0.0	–	ns
t_{PD}	Output delay from CLK	2.6 v signals	I_{OL} = 8 mA I_{OH} = -4 mA C_L = 35 pF V_{LOAD} = 1.5V	–	1.40	ns
		3.3 V non-PCI interface		–	1.66	ns
		3.3v PCI interface		–	4.0	ns
		EPD		-	4.0	ns
t_{OH}	Output hold time from CLK	2.6 v signals		-0.37	–	ns
		3.3v signals except PCI		-0.37	–	ns
		PCI interface		-2.0	–	ns
		EPD		0.2	–	ns
t_{LOCK}	PLL acquisition time			20		us
				2500		cycles

1. All timing requirements are specified with PLL enabled.
2. All estimates are derived from simulation.
3. Some signals are asserted and deasserted asynchronously.

AC Characteristics - Clock Timing[1]

t_{CYC} (CLK)	Processor clock cycle time	3.3	–	–	ns
t_W(CLK)	Processor clock duty cycle	40	50	60	%
t_{SLEW}(CLK)	Clock input slew rate	3.3	–	–	V/ns
t_{CYC} (PCICLK)	PCI clock cycle time	7.5	–	–	ns
t_W(PCICLK)	Processor clock duty cycle	40	50	60	%
t_{SLEW}(PCICLK)	Clock input slew rate	1.5	–	4	V/ns
t_{CYC} (TCK)	TCK clock cycle time	20	–	100	ns
t_W(TCK)	TCK clock duty cycle	40	50	60	%
t_{CYC} (SRAM_CLK)	SRAM_CLK clock cycle time	–	t_{CYC} (CLK) x2	–	ns
t_{CYC} (UPA_CLK)	UPA_CLK clock cycle time	–	t_{CYC} (CLK) x3	–	ns
t_W (P_RESET_L, X_RESET_L)	RESET pulse width LOCK MODE (See figure tbd)	TBD	–	–	ns
t_W (P_RESET_L, X_RESET_L)	RESET pulse width BYPASS MODE (See figure tbd)	TBD	–	–	ns

1. This specification is for PLLs enabled

AC Characteristics - JTAG Timing

t_{SU} ($\overline{TRST}$)	Input setup time to TCK	$\overline{TRST}$		5	–	–	ns
t_{SU} (TDI)	Input setup time to TCK	TDI		–	3	–	ns
t_{SU} (TMS)	Input setup time to TCK	TMS		–	4	–	ns
t_H($\overline{TRST}$)	Input hold time to TCK	$\overline{TRST}$		–	TBD	–	ns
t_H(TDI)	Input hold time to TCK	TDI		–	1.5	–	ns
t_H(TMS)	Input hold time to TCK	TMS		–	1.5	–	ns
t_{PD}(TDO)	Output delay from TCK[1]	TDO	I_{OL} = 8 mA; I_{OH} = -4 mA	–	6	–	ns
t_{OH}(TDO)	Output hold time from TCK[1]	TDO	C_L = 35 pF; V_{LOAD} = 1.5V	–	–	3	ns

1. TDO is referenced from falling edge of TCK.

PARAMETER MEASUREMENT INFORMATION

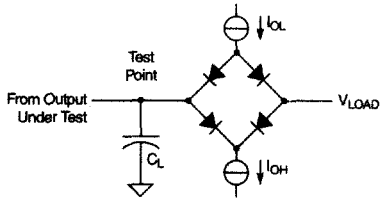


Figure 22. Load Circuit

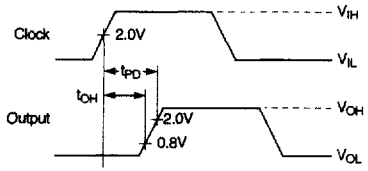


Figure 23. Voltage Waveforms for 3.3V Signals- Propagation Delay Times

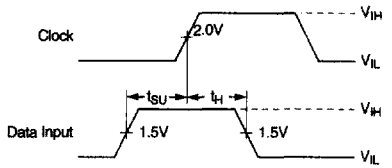


Figure 24. Voltage Waveforms for 3.3V Signals - Setup and Hold Times

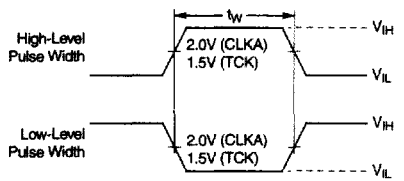


Figure 25. Voltage Waveforms - Clock Pulse Duration

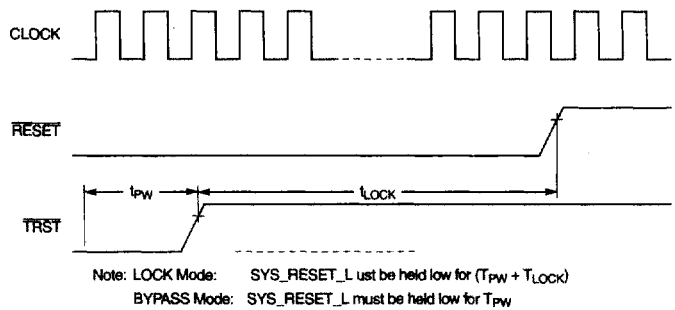


Figure 26. Reset Timing

Figure 27. Typical PECL Input Waveform for CLK

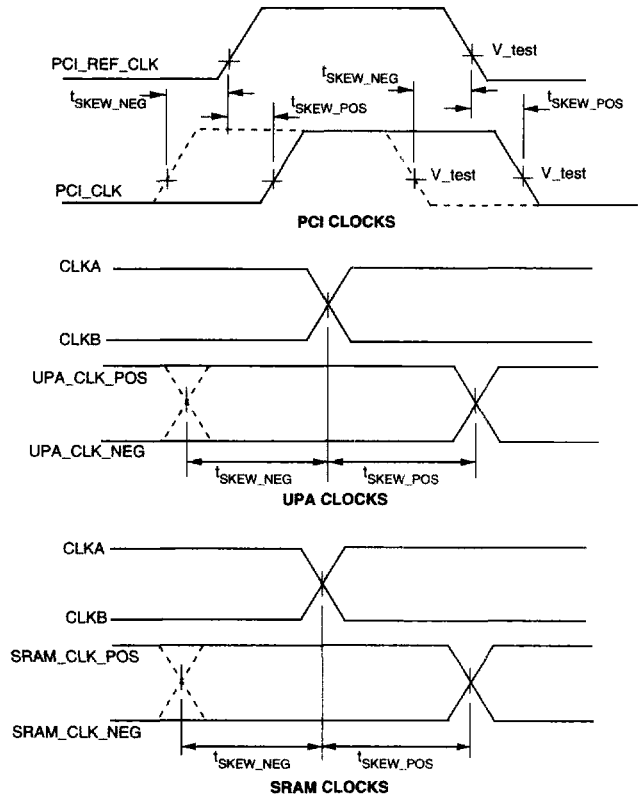


Figure 28. Voltage Waveforms - Clock Skew

Clock Skew [1] [2]

UPA_CLK_POS	0.45	0.6	ns	CLKA
SRAM_CLK_POS	0.45	0.6	ns	CLKA
PCI_CLK	1.2	2.15	ns	PCI_REF_CLK

1. For definitions, see *Figure 25*;
2. For PCI clock skews: v_test = 0.4(VDD_H); for full detail see PCI specification version 2.1

THERMAL SPECIFICATIONS

This covers the processor only. Other components, including the SRAMs, should be analyzed also to determine the possible need for heat sinks.

Maximum Ambient Temperature vs. Air Flow[1]

T_A	42	49	54	61	°C

1. Assuming use of approved heatsink, with approved attach method. All at sea level, assuming maximum power dissipation and maximum junction temperature of 105 deg C. Derate 1 deg C / 1000 ft.

T_A, ambient temperature, is the temperature of the air upstream of the package.

The maximum junction temperature (T_J) specification is 105 C, which is equivalent to the maximum case temperature (T_C) of 90 C for the UltraSPARC-IIi CPU. T_C can be obtained from the following relationship:

$$T_C = T_A + P_d \times \theta_{ca}$$

where T_A is the ambient air temperature, P_d is the power dissipation, and θ_{ca} is the case-to-air thermal resistance for the CPU with a heat sink. The table below lists thermal resistance θ_{ca} for several values of air flow rate when power dissipation and device junction temperature are at their maximum permissible values.

Thermal Resistances[1]

θ_{ca} (°C/W)[2]	1.41	1.09	0.95	0.88
θ_{ca} (°C/W)[3]	1.15	0.98	0.88	0.81

1. Assuming use of approved heatsink with approved attachment method. All specifications are for sea level altitude, assuming maximum power dissipation and maximum junction temperature.
2. Free-stream airflow
3. Ducted airflow

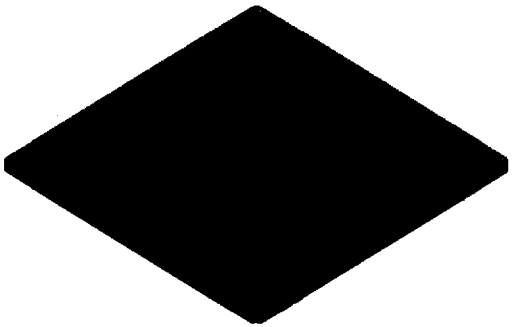
Case temperature must lie within the specified range and should be checked using a thermocouple in a fully configured system.

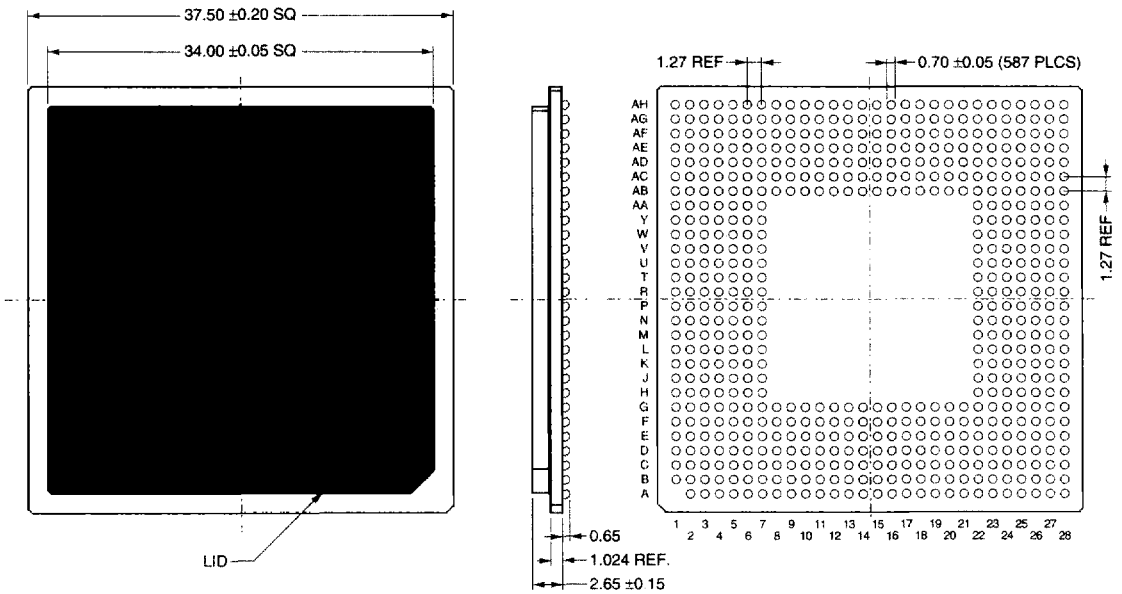
Errors are introduced by poor thermal contacts, by radiation heat loss, and by conduction through thermocouple leads. To minimize errors:

- Use a 35 gauge K-type thermocouple or equivalent.
- Attach the thermocouple to the center of the package top surface.
- Attach at a 90% angle with a temperature-tolerant adhesive bond, for example a thermal grease.
- Drill a hole through the heat sink (if attached) of diameter no greater than 0.150".

PACKAGING INFORMATION

587 BGA Package Dimensions





Notes: 1. Dimensions in mm.
2. LID Material is Mitsubishi MF224 1/4H Cu or equiv.
3. LID to be connected to VSSC.

587 BGA Pin Assignment

A02	VSSO	B19	SYSADR-0	D08	VDDO	E25	S_REPLY-1
A03	VDDO	B20	SYSADR-16	D09	ECAT-0	E26	MEM_CAS_L-0
A04	TDATA-10	B21	SYSADR-3	D10	VSSO	E27	MEM_RASB_L-0
A05	TDATA-11	B22	SYSADR-6	D11	ECAT-8	E28	MEM_RAST_L-3
A06	TPAR-0	B23	VSSO	D12	ECAT-14	F01	AD-23
A07	DOE_L	B24	SYSADR-10	D13	ECAD-2	F02	VSSO
A08	VDDO	B25	SYSADR-11	D14	VDDO	F03	VDDH
A09	VSSO	B26	SYSADR-14	D15	VDDO	F04	AD-31
A10	ECAT-9	B27	VDDH	D16	ECAD-16	F05	PCICLK
A11	ECAT-13	B28	VSSO	D17	BYTEWE_L-3	F06	VSSC
A12	VDDO	C01	VDDO	D18	BYTEWE_L-6	F07	TDATA-5
A13	VSSO	C02	P2L5CLK	D19	VSSO	F08	TDATA-9
A14	ECAD-9	C03	VDDO	D20	SYSADR-18	F09	VDDC
A15	ECAD-10	C04	TDATA-3	D21	VDDH	F10	TSYN_WR_L
A16	VSSO	C05	TDATA-7	D22	SYSADR-9	F11	ECAT-5
A17	VDDO	C06	VDDO	D23	SYSADR-12	F12	VSSC
A18	BYTEWE_L-4	C07	TPAR-1	D24	SYSADR-28	F13	VSSC
A19	ADR_VLD	C08	TOE_L	D25	VSSO	F14	ECAD-5
A20	VSSO	C09	ECAT-3	D26	S_REPLY-2	F15	ECAD-12
A21	VDDH	C10	ECAT-6	D27	MEM_CAS_L-1	F16	VSSC
A22	SYSADR-4	C11	ECAT-10	D28	MEM_RAST_L-2	F17	VSSC
A23	SYSADR-7	C12	ECAD-0	E01	AD-26	F18	SYSADR-15
A24	SYSADR-8	C13	ECAD-3	E02	AD-28	F19	SYSADR-19
A25	SYSADR-24	C14	ECAD-7	E03	PCI_REF_CLK	F20	VDDC
A26	VDDH	C15	ECAD-13	E04	VSSPLL2	F21	SYSADR-23
A27	VSSO	C16	ECAD-17	E05	ITB_TEST_MODE	F22	SYSADR-25
A28	VSSO	C17	BYTEWE_L-1	E06	TDATA-1	F23	VSSC
B01	VSSO	C18	BYTEWE_L-7	E07	VSSO	F24	S_REPLY-0
B02	TDATA0	C19	SYSADR-1	E08	TDATA-14	F25	MEM_RAST_L-0
B03	TDATA-4	C20	SYSADR-2	E09	DSYN_WR_L	F26	VDDH
B04	TDATA-8	C21	SYSADR-5	E10	ECAT-2	F27	VSSO
B05	TDATA-13	C22	SYSADR-22	E11	VDDO	F28	MEM_DATA-35
B06	VSSO	C23	VDDH	E12	ECAT-12	G01	AD-20
B07	TDATA-15	C24	SYSADR-26	E13	VSSO	G02	AD-22
B08	ECAT-1	C25	SYSADR-13	E14	ECAD-6	G03	AD-24
B09	ECAT-4	C26	VDDH	E15	ECAD-14'	G04	AD-27
B10	ECAT-7	C27	MEM_WE_L	E16	VSSO	G05	VSSO
B11	ECAT-11	C28	VDDH	E17	BYTEWE_L-2	G06	VDDPLL2
B12	ECAD-1	D01	AD-30	E18	VDDO	G07	VSSC
B13	ECAD-4	D02	RST_L	E19	SYSADR-17	G08	VDDC
B14	ECAD-8	D03	ECACHE_22_MODE	E20	SYSADR-20	G09	VDDC
B15	ECAD-11	D04	VSSO	E21	SYSADR-21	G10	VSSC
B16	ECAD-15	D05	TDATA-2	E22	VSSO	G11	VSSC
B17	BYTEWE_L-0	D06	TDATA-6	E23	SYSADR-27	G12	VDDC
B18	BYTEWE_L-5	D07	TDATA-12	E24	P_REPLY-0	G13	VDDC

587 BGA Pin Assignment (Continued)

G14	VSSC	K04	VSSO	N22	VDDC	T26	MEM_DATA-71
G15	VSSC	K05	TRDY_L	N23	VSSC	T27	MEM_DATA-36
G16	VDDC	K06	DEVSEL_L	N24	VSSO	T28	VSSO
G17	VDDC	K07	VSSC	N25	MEM_DATA-46	U01	VDDH
G18	VSSC	K22	VSSC	N26	MEM_DATA-48	U02	AD-15
G19	VSSC	K23	MEM_DATA-30	N27	MEM_DATA-47	U03	AD-14
G20	VDDC	K24	MEM_DATA-62	N28	VSSO	U04	AD-13
G21	VDDC	K25	VSSO	P01	REQ_L-3	U05	AD-12
G22	VSSC	K26	MEM_DATA-60	P02	CLKSEL	U06	VSSC
G23	P_REPLY-1	K27	MEM_DATA-59	P03	VSSPLL	U07	VDDC
G24	VSSO	K28	MEM_DATA-56	P04	VDDH	U22	VDDC
G25	MEM_RASB_L-2	L01	CBE_L-0	P05	CLKA	U23	VSSC
G26	MEM_RASB_L-3	L02	CBE_L-1	P06	CLKB	U24	MEM_DATA-66
G27	MEM_DATA-34	L03	PAR	P07	VSSC	U25	MEM_DATA-65
G28	MEM_DATA-31	L04	CBE_L-2	P22	VSSC	U26	MEM_DATA-67
H01	VDDH	L05	VDDH	P23	MEM_DATA-42	U27	MEM_DATA-68
H02	AD-18	L06	CBE_L-3	P24	MEM_DATA-45	U28	VDDH
H03	AD-19	L07	VSSC	P25	VDDH	V01	AD-11
H04	VDDH	L22	VSSC	P26	MEM_DATA-44	V02	AD-10
H05	AD-25	L23	MEM_DATA-58	P27	MEM_DATA-43	V03	AD-9
H06	AD-29	L24	VDDH	P28	MEM_DATA-41	V04	AD-8
H07	VDDC	L25	MEM_DATA-54	R01	REQ_L-1	V05	VDDH
H22	VDDC	L26	MEM_DATA-57	R02	REQ_L-0	V06	AD-4
H23	MEM_RAST_L-1	L27	MEM_DATA-55	R03	GNT_L-3	V07	VSSC
H24	MEM_RASB_L-1	L28	MEM_DATA-53	R04	VDDH	V22	VSSC
H25	VDDH	M01	VDDH	R05	REQ_L-2	V23	MEM_DATA-21
H26	MEM_DATA-32	M02	SRAM_CLK_NEG	R06	GNT_L-2	V24	VDDH
H27	MEM_DATA-28	M03	PLLBYPASS	R07	VSSC	V25	MEM_DATA-25
H28	VDDH	M04	UPA_CLK_POS	R22	VSSC	V26	MEM_DATA-26
J01	VSSO	M05	UPA_CLK_NEG	R23	MEM_DATA-38	V27	MEM_DATA-27
J02	IRDY_L	M06	VSSC	R24	MEM_DATA-70	V28	MEM_DATA-64
J03	FRAME_L	M07	VDDC	R25	VDDH	W01	AD-7
J04	AD-17	M22	VDDC	R26	MEM_DATA-37	W02	AD-6
J05	AD-21	M23	VSSC	R27	MEM_DATA-39	W03	AD-5
J06	VDDC	M24	MEM_DATA-50	R28	MEM_DATA-40	W04	VSSO
J07	VDDC	M25	MEM_DATA-52	T01	VSSO	W05.	AD-1
J22	VDDC	M26	MEM_DATA-51	T02	GNT_L-1	W06	AD-0
J23	VDDC	M27	MEM_DATA-49	T03	GNT_L-0	W07	VSSC
J24	MEM_DATA-33	M28	VDDH	T04	AD-16	W22	VSSC
J25	MEM_DATA-29	N01	VSSO	T05	VSSO	W23	MEM_DATA-17
J26	MEM_DATA-63	N02	SRAM_CLK_POS	T06	VSSC	W24	MEM_DATA-18
J27	MEM_DATA-61	N03	VDDPECL	T07	VDDC	W25	VSSO
J28	VSSO	N04	VDDPLL	T22	VDDC	W26	MEM_DATA-22
K01	SERR_L	N05	VSSO	T23	VSSC	W27	MEM_DATA-23
K02	PERR_L	N06	VSSC	T24	VSSO	W28	MEM_DATA-24
K03	STOP_L	N07	VDDC	T25	MEM_DATA-69	Y01	VSSO
Y02	AD-3	AB20	VDDC	AD10	EDATA-29	AE28	MEM_DATA-3

587 BGA Pin Assignment (Continued)

Y03	AD-2	AB21	VDDC	AD11	VDDO	AF01	VDDH
Y04	P_RESET_L	AB22	VSSC	AD12	EDATA-40	AF02	TDO
Y05	INT_NUM-3	AB23	SPARE3V	AD13	VSSO	AF03	VDDO
Y06	VDDC	AB24	VSSO	AD14	EDATA-3	AF04	EDATA-9
Y07	VDDC	AB25	MEM_DATA-4	AD15	EDATA-5	AF05	EDATA-12
Y22	VDDC	AB26	MEM_DATA-8	AD16	VSSO	AF06	VDDO
Y23	VDDC	AB27	MEM_DATA-12	AD17	EDATA-50	AF07	EDPAR-2
Y24	MEM_DATA-13	AB28	MEM_DATA-14	AD18	VDDO	AF08	EDATA-23
Y25	MEM_DATA-16	AC01	SB_EMPTY-0	AD19	EDATA-60	AF09	EDPAR-3
Y26	MEM_DATA-19	AC02	VSSO	AD20	XCVR_OEA_L	AF10	EDATA-30
Y27	MEM_DATA-20	AC03	VDDH	AD21	XCVR_CLK-2	AF11	EDATA-34
Y28	VSSO	AC04	TRST_L	AD22	VSSO	AF12	EDATA-38
AA01	VDDH	AC05	PMO	AD23	MEM_ADDR-5	AF13	EDATA-41
AA02	'NT_NUM-0	AC06	VSSC	AD24	MEM_ADDR-9	AF14	EDATA-43
AA03	INT_NUM-2	AC07	EDATA-8	AD25	RMTV_SEL	AF15	EDATA-4
AA04	VDDH	AC08	EDATA-15	AD26	MEM_DATA-2	AF16	EDATA-6
AA05	SB_DRAIN	AC09	VDDC	AD27	MEM_DATA-5	AF17	EDATA-48
AA06	SYS_RESET_L	AC10	EDATA-26	AD28	MEM_DATA-7	AF18	EDATA-52
AA07	VDDC	AC11	EDATA-33	AE01	TDI	AF19	EDATA-56
AA22	VDDC	AC12	VSSC	AE02	RAM_TEST	AF20	EDATA-59
AA23	MEM_DATA-6	AC13	VSSC	AE03	TEMP_SEN-0	AF21	EDATA-62
AA24	MEM_DATA-9	AC14	EDPAR-5	AE04	VSSO	AF22	XCVR_CLK-1
AA25	VDDH	AC15	EDATA-45	AE05	EDATA-10	AF23	VDDH
AA26	MEM_DATA-11	AC16	VSSC	AE06	EDATA-13	AF24	MEM_ADDR-3
AA27	MEM_DATA-15	AC17	VSSC	AE07	EDATA-17	AF25	MEM_ADDR-8
AA28	VDDH	AC18	EDATA-57	AE08	VDDO	AF26	VDDH
AB01	INT_NUM-1	AC19	XCVR_CLK-0	AE09	EDATA-24	AF27	MEM_ADDR-11
AB02	INT_NUM-4	AC20	VDDC	AE10	VSSO	AF28	VDDH
AB03	INT_NUM-5	AC21	XCVR_WR_CNTL-0	AE11	EDATA-36	AG01	VSSO
AB04	TCK	AC22	MEM_ADDR-2	AE12	EDATA-37	AG02	VDDO
AB05	VSSO	AC23	VSSC	AE13	EDATA-42	AG03	L5CLK
AB06	EXT_EVENT	AC24	MEM_ADDR-10	AE14	VDDO	AG04	EDATA-11
AB07	VSSC	AC25	MEM_DATA-1	AE15	VDDO	AG05	EDATA-16
AB08	VDDC	AC26	VDDH	AE16	EDATA-47	AG06	VSSO
AB09	VDDC	AC27	VSSO	AE17	EDATA-49	AG07	EDATA-21
AB10	VSSC	AC28	MEM_DATA-10	AE18	EDATA-53	AG08	EDATA-27
AB11	VSSC	AD01	SB_EMPTY-1	AE19	VSSO	AG09	EDATA-28
AB12	VDDC	AD02	TMS	AE20	EDATA-63	AG10	EDATA-31
AB13	VDDC	AD03	X_RESET_L	AE21	VDDH	AG11	EDATA-35
AB14	VSSC	AD04	TEMP_SEN-1	AE22	XCVR_RD_CNTL-1	AG12	EDATA-39
AB15	VSSC	AD05	EPD	AE23	MEM_ADDR-1	AG13	EDATA-0
AB16	VDDC	AD06	EDPAR-1	AE24	MEM_ADDR-6	AG14	EDATA-2
AB17	VDDC	AD07	VSSO	AE25	VSSO	AG15	EDATA-44
AB18	VSSC	AD08	EDATA-19	AE26	MEM_ADDR-12	AG16	EDATA-46
AB19	VSSC	AD09	EDAT-22	AE27	MEM_DATA-0	AG17	EDATA-7
AG18	EDPAR-6	AG28	VSSO	AH10	EDATA-32	AH20	VSSO
AG19	EDATA-55	AH01	VSSO	AH11	EDPAR-4	AH21	VDDO

587 BGA Pin Assignment (Continued)

AG20	EDATA-58	AH02	VSSO	AH12	VDDO	AH22	EDPAR-7
AG21	EDATA-61	AH03	VDDO	AH13	VSSO	AH23	XCVR_OEB_L
AG22	XCVR_SEL_L	AH04	EDATA-14	AH14	EDATA-1	AH24	XCVR_RD_CNTL-0
AG23	VSSO	AH05	EDATA-18	AH15	EDPAR-0	AH25	XCVR_WR_CNTL-1
AG24	MEM_ADDR-0	AH06	EDATA-20	AH16	VSSO	AH26	VDDH
AG25	MEM_ADDR-4	AH07	EDATA-25	AH17	VDDO	AH27	VSSO
AG26	MEM_ADDR-7	AH08	VDDO	AH18	EDATA-51	AH28	VSSO
AG27	VDDH	AH09	VSSO	AH19	EDATA-54		

ORDERING INFORMATION

SME1040BGA-266 SME1040BGA-300	266 MHz 300MHz	UltraSPARC IIi, The UltraSPARC *i* -Series High-Performance, 64-bit RISC Processor, PCI Interface

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