ESDA6V8UW

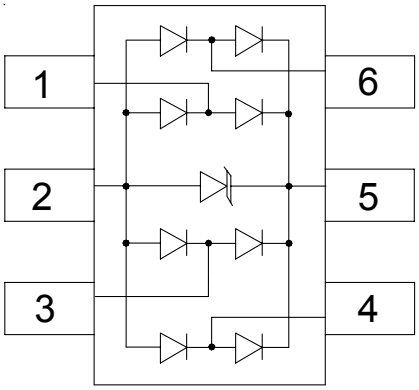
Transil array for data protection

Description:

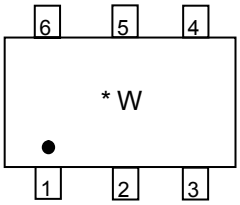
The ESDA6V8UW is 4-channel very low capacitance ESD transient voltage suppressor which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge. It is particularly well-suited to protect systems with high speed communication lines from ESD, EFT, and lighting.

The ESDA6V8UW is consists of eight low capacitance steering diodes and a TVS diode in a SC-70-6L package. Each channel of ESDA6V8UW could safely dissipate ESD strikes of ±15kV air discharge as well as ±8kV contact discharge, meeting the requirement of the IEC 61000-4-2 international standard. Using the MIL-STD-883 (Method 3015) specification for Human Body Model (HBM) ESD, the device provides protection for contact discharges to greater than ±15kV.

(SC-70-6L)



SC-70-6L (Top View)



* = Month

W = Specific Device Code

Specification Features:

- Stand−off Voltage: 5 V
- Peak Power up to 300 Watts @ 8 x 20 us Pulse
- Low Leakage current IEC61000−4−2
- Level 4 ESD Protection IEC61000−4−4
- Level 4 EFT Protection
- Low capacitance: 0.7 pF typical

Mechanical Characteristics

- SC-70-6L Package
- Pb−Free Packages are Available
- Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel per EIA 481

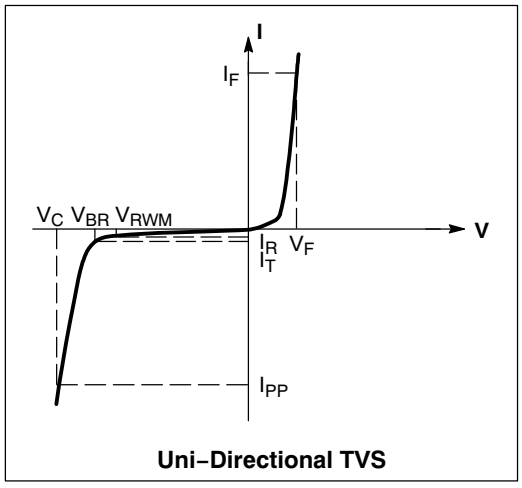
Applications

- High Speed Communication Line Protection
- USB 2.0 Power and Data Line Protection
- Monitors and Flat Panel Displays Notebook Computers
- Video Line Protection & Base Stations
- HDSL, IDSL Secondary IC Side Protection
- Microcontroller Input Protection
- LCD and camera modules
- 10/100/1000 Ethernet

Absolute Max Ratings (Tamb=25 C)

Rating	Symbol	Value	Units
Peak Pulse Power(tp = 8/20μs)	P_{PP}	300	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	Vpp	+/-15 +/-8	KV
Maximum lead temperature for soldering during 10s	T_L	260	˚C
Storage Temperature Range	Tstg	-55 to +125	˚C
Operating Temperature Range	Top	-55 to +125	˚C

Electrical Parameter



Uni−Directional TVS

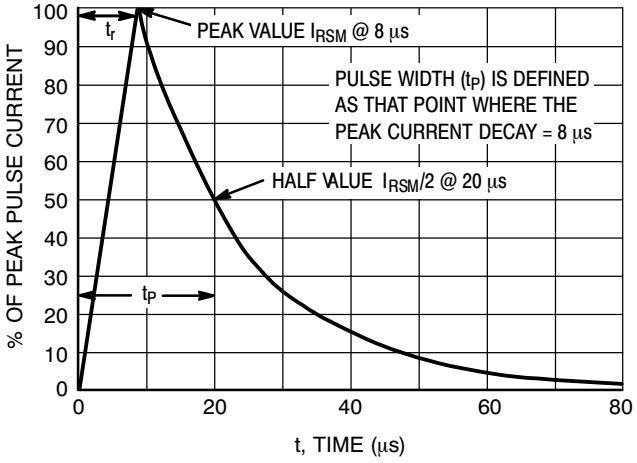


Figure 1. 8 X 20 μs Pulse Waveform

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ IPP
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ VRWM
I_T	Test Current
V_{BR}	Breakdown Voltage @ IT
I_F	Forward Current
V_F	Forward Voltage @ IF

Electrical Characteristics

(T=25°C, Device for 5.0V Reverse Stand-off Voltage)

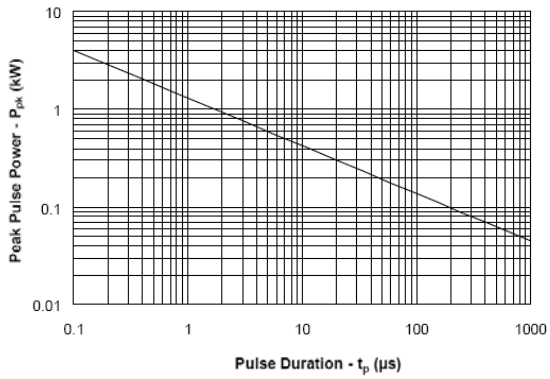
	Conditions	Minimum	Typical	Maximum	Unit
I_R	V_{RWM}=5V, Pin5 to 2			5	uA
V_F	I_F= 10mA	0.4	0.8	1.5	V
V_{BR},	I_T=1mA, Pin5 to 2	6.0	7.0		V
V_C	I_{PP}=1A, tp = 8/20us, note 1&2 Any I/O pin to Ground			12.0	V
C_j	V_R = 0V, f = 1MHz Any I/O pin to Ground		1.2	1.5	pF
	V_R = 0V, f = 1MHz Between I/O pins		0.7		pF

Note 1: These parameters guaranteed by design and characterization.

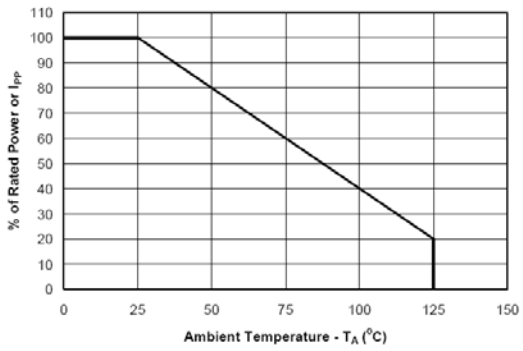
Note 2: These measurements performed with no external capacitor on Pin5.

Typical Characteristics

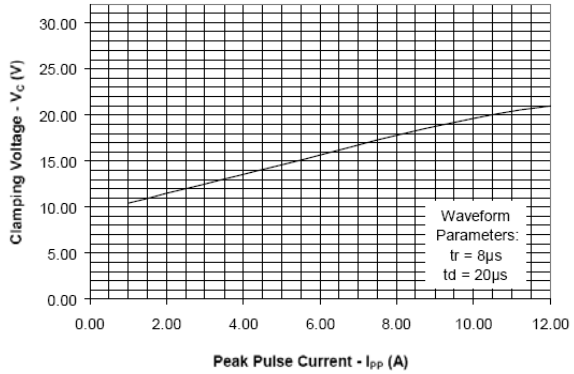
Non-Repetitive Peak Pulse Power vs. Pulse Time



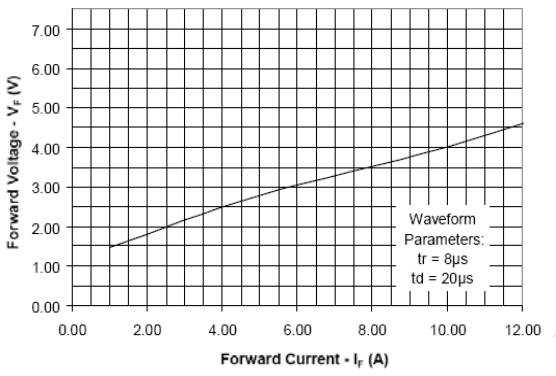
Power Derating Curve



Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Applications Information

Device Connection Options for Protection of Four □igh-Speed Data Lines

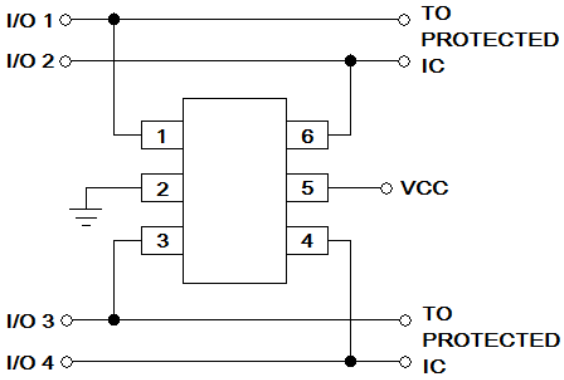
This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. Pin 2 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.

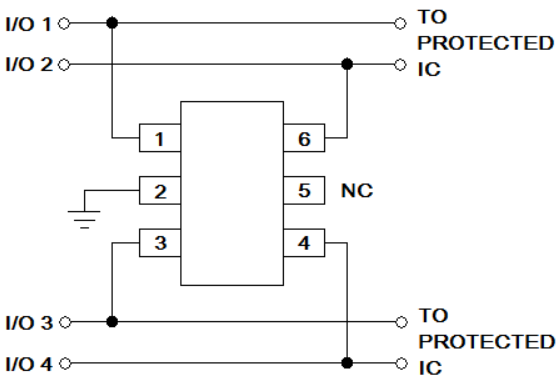
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and VCC is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at pins 1, 3, 4, and 6. Pin 2 is connected to ground and pin 5 is not connected.

Data Line and Power Supply Protection Using Vcc as reference



Data Line Protection Using Internal TVS Diode as reference

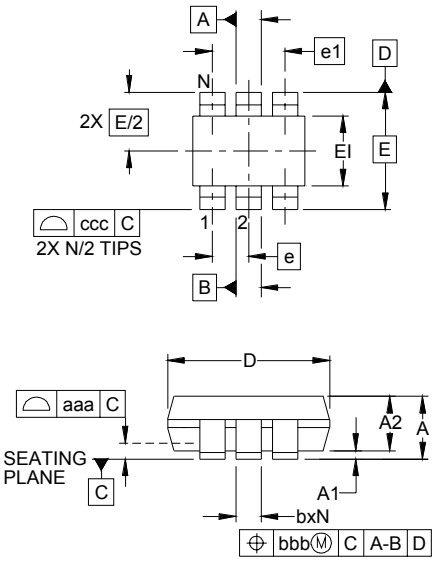


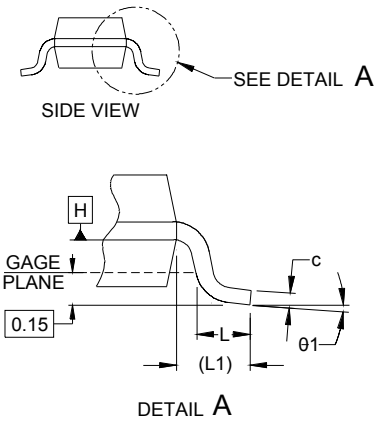
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100□ tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Package mechanical data

Outline drawing:



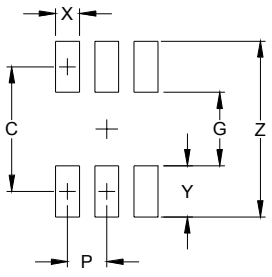


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.004	0.00	-	0.10
A2	.028	.035	.039	0.70	0.90	1.00
b	.006	-	.012	0.15	-	0.30
c	.003	-	.009	0.08	-	0.22
D	.075	.079	.083	1.90	2.00	2.10
E1	.045	.049	.053	1.15	1.25	1.35
E	.083 BSC			2.10 BSC		
e	.026 BSC			0.65 BSC		
e1	.051			1.30 BSC		
L	.010	.014	.018	0.26	0.36	0.46
L1	(.017)			(0.42)		
N	6			6		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.012			0.30		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-203, VARIATION AB.

Land Pattern:



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.073)	(1.85)
G	.039	1.00
P	.026	0.65
X	.016	0.40
Y	.033	0.85
Z	.106	2.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.