128K X 36 Dual I/O Dual Address Synchronous SRAM

Features

- Fast clock speed: 133, 100, and 83 MHz
- Fast Access Times: 4.0/5.0/6.0 ns Max.
- Single Clock Operation
- Single 3.3V –5% and +5% power supply V_{CC}
- Separate V_{CCQ} for output buffer
- Two chip enables for simple depth expansion
- Address, Data Input, $\overline{CE1X}$, CE2X, $\overline{CE1Y}$, CE2Y, $\overline{PTX}$, $\overline{PTY}$, $\overline{WEX}$, $\overline{WEY}$, and Data Output Registers On-Chip
- Concurrent Reads and Writes
- Two Bidirectional Data Buses
- Can be configured as separate I/O
- Pass-Through feature
- Asynchronous Output Enables (OEX#, OEY#)
- LVTTL Compatible I/O
- Self-Timed Write
- Automatic power-down
- 176-Pin TQFP Package

Functional Description

The CY7C1300A SRAM integrates 131,072 x 36 SRAM cells with advanced synchronous peripheral circuitry. It employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1300A allows the user to concurrently perform reads, writes, or pass-through cycles in combination on the two data ports. The two address ports (AX, AY) determine the read or write locations for their respective data ports (DQX, DQY).

All input pins except output enable pins ($\overline{OEX}$, $\overline{OEY}$) are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion chip enables ($\overline{CE1X}$, CE2X, $\overline{CE1Y}$ and CE2Y), pass-through controls ($\overline{PTX}$ and $\overline{PTY}$), and read-write control ($\overline{WEX}$ and $\overline{WEY}$).

The pass-through feature allows data to be passed from one port to the other, in either direction. The PTX# input must be asserted to pass data from port X to port Y. The PTY# will likewise pass data from port Y to port X. A pass-through operation takes precedence over a read operation.

For the case when AX and AY are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

The CY7C1300A operates from a +3.3V power supply. All inputs and outputs are LVTTL compatible. These dual I/O, dual address synchronous SRAMs are well suited for ATM, Ethernet switches, routers, cell/frame buffers, SNA switches and shared memory applications.

The CY7C1300A needs one extra cycle after power for proper power-on reset. The extra cycle is needed after Vcc is stable on the device.

This device is available in a 176-pin TQFP package.

Logic Block Diagram
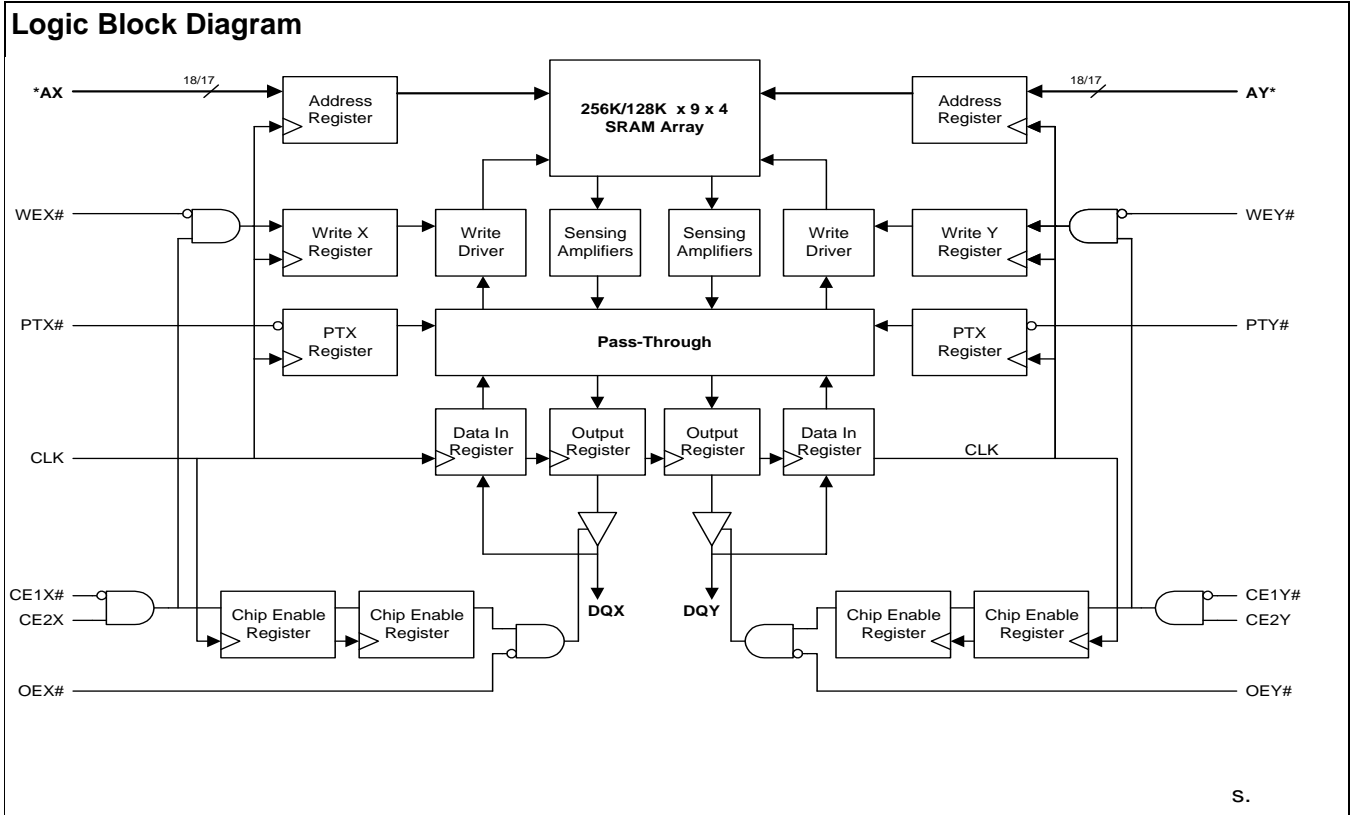
Selection Guide

	-133	-100	-83
Maximum Access Time (ns)	4.0	5.0	6.0
Maximum Operating Current (mA)	400	350	300
Maximum CMOS Standby Current (mA)	100	100	100

Shaded areas contain advance information.

Note:
1. For 128K x 36 devices, AX and AY are 17-bit wide buses.

Pin Configuration

176-Pin TQFP

Left side (pins 1–44):

Pin	Signal
1	VSS
2	DQX20
3	DQY20
4	VCCQ
5	VSS
6	DQX21
7	DQY21
8	DQX22
9	DQY22
10	VCCQ
11	VSS
12	DQX23
13	DQY23
14	DQX24
15	DQY24
16	VCCQ
17	VSS
18	DQX25
19	DQY25
20	DQX26
21	DQY26
22	VCC
23	VSS
24	DQY27
25	DQX27
26	DQY28
27	DQX28
28	VCCQ
29	VSS
30	DQY29
31	DQX29
32	DQY30
33	DQX30
34	VCCQ
35	VSS
36	DQY31
37	DQX31
38	DQY32
39	DQX32
40	VCCQ
41	VSS
42	DQY33
43	DQX33
44	VSS

Bottom side (pins 45–88):

Pin	Signal
45	VSS
46	DQY34
47	DQX34
48	VSS
49	VCCQ
50	DQY35
51	DQX35
52	VSS
53	VSS
54	AY5
55	AX5
56	AY4
57	AX4
58	AY3
59	AX3
60	AY2
61	AX2
62	AY1
63	AX1
64	AY0
65	AX0
66	VSS
67	VCC
68	AX10
69	AY10
70	AX11
71	AY11
72	AX12
73	AY12
74	AX13
75	AY13
76	AX14
77	AY14
78	AX15
79	AY15
80	AX16
81	AY16
82	DQX0
83	DQY0
84	VCCQ
85	VSS
86	DQX1
87	DQY1
88	VSS

Right side (pins 89–132):

Pin	Signal
89	VSS
90	DQX2
91	DQY2
92	VCCQ
93	VSS
94	DQX3
95	DQY3
96	DQX4
97	DQY4
98	VCCQ
99	VSS
100	DQX5
101	DQY5
102	DQX6
103	DQY6
104	VCCQ
105	VSS
106	DQX7
107	DQY7
108	DQX8
109	DQY8
110	VCC
111	VSS
112	DQY9
113	DQX9
114	DQY10
115	DQX10
116	VCCQ
117	VSS
118	DQY11
119	DQX11
120	DQY12
121	DQX12
122	VCCQ
123	VSS
124	DQY13
125	DQX13
126	DQY14
127	DQX14
128	VCCQ
129	VSS
130	DQY15
131	DQX15
132	VSS

Top side (pins 133–176):

Pin	Signal
133	VSS
134	DQY16
135	DQX16
136	VSS
137	VCC
138	DQY17
139	DQX17
140	VSS
141	VSS
142	AY9
143	AX9
144	AY8
145	AX8
146	PTX#
147	PTY#
148	WEX#
149	WEY#
150	CE1X#
151	CE2X
152	OEX#
153	OEY#
154	VSS
155	VCC
156	CLK
157	CE1Y#
158	CE2Y
159	NC
160	NC
161	VSS
162	NC
163	NC
164	NC
165	VSS
166	AY7
167	AX7
168	AY6
169	AX6
170	DQX18
171	DQY18
172	VCCQ
173	VSS
174	DQX19
175	DQY19
176	VSS

Pin Definitions (176-pin TQFP)

Name	I/O	Description
AX0–AX16	Input-Synchronous	Synchronous Address Inputs of Port X: Do not allow address pins to float.
AY0–AY16	Input-Synchronous	Synchronous Address Inputs of Port Y: Do not allow address pins to float.
$\overline{WEX}$	Input-Synchronous	Read Write of Port X: $\overline{WEX}$ signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
$\overline{WEY}$	Input-Synchronous	Read Write of Port Y: $\overline{WEY}$ signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
$\overline{PTX}$	Input-Synchronous	Pass-Through of Port X: $\overline{PTX}$ signal is a synchronous input that enables passing Port X input to Port Y output.
$\overline{PTY}$	Input-Synchronous	Pass-Through of Port Y: $\overline{PTY}$ signal is a synchronous input that enables passing Port Y input to Port X output.
$\overline{OEX}$	Input	Asynchronous Output Enable of Port X: $\overline{OEX}$ must be LOW to read data. When $\overline{OEX}$ is HIGH, the DQXx pins are in high-impedance state.
$\overline{OEY}$	Input	Asynchronous Output Enable of Port Y: $\overline{OEY}$ must be LOW to read data. When $\overline{OEY}$ is HIGH, the DQYx pins are in high-impedance state.
DQX0–DQX35	Input/Output	Data Inputs/Outputs of Port X: Both the data input path and data output path are registered and triggered by the rising edge of CLK.
DQY0–DQY35	Input/Output	Data Inputs/Outputs of Port Y: Both the data input path and data output path are registered and triggered by the rising edge of CLK.
CLK	Input-Synchronous	Clock: This is the clock input to this device. Except for $\overline{OEX}$ and $\overline{OEY}$, all timing references of the address, data in, and all control signals for the device are made with respect to the rising edge of CLK.
$\overline{CE1X}$	Input-Synchronous	Synchronous Active LOW Chip Enable Port X: $\overline{CE1X}$ is used with CE2X to enable Port X of this device. $\overline{CE1X}$ sampled HIGH at the rising edge of clock initiates a deselect cycle for Port X.
CE2X	input-Synchronous	Synchronous Active HIGH Chip Enable Port X: CE2X is used with $\overline{CE1X}$ to enable Port X of this device. CE2X sampled LOW at the rising edge of clock initiates a deselect cycle for Port X.
$\overline{CE1Y}$	Input-Synchronous	Synchronous Active LOW Chip Enable Port Y: $\overline{CE1Y}$ is used with CE2Y to enable Port Y of this device. $\overline{CE1Y}$ sampled HIGH at the rising edge of clock initiates a deselect cycle for Port Y.
CE2Y	input-Synchronous	Synchronous Active HIGH Chip Enable Port Y: CE2Y is used with $\overline{CE1Y}$ to enable Port Y of this device. CE2Y sampled LOW at the rising edge of clock initiates a deselect cycle for Port Y.
VCC	Supply	Power Supply: +3.3V –5% and +5%.
VSS	Ground	Ground: GND.
VSS	Ground	Ground: GND. No chip current flows through these pins. However, user needs to connect GND to these pins.
VCCQ	I/O Supply	Output Buffer Supply: +3.3V -5% and +5%.
NC	-	No Connect: These signals are not internally connected. User can connect them to V_{CC}, V_{SS}, or any signal lines or simply leave them floating.

Cycle Description Truth Table[2, 3, 4, 5, 6, 7, 8, 9]

Operation	CE1X#	CE2X	CE1Y#	CE2Y	WEX#	WEY#	PTX#	PTY#
DESELECT CYCLE	H	X	H	X	X	X	X	X
DESELECT CYCLE	X	L	X	L	X	X	X	X
WRITE PORT X	L	H	X	X	0	X	X	X
WRITE PORT Y	X	X	L	H	X	0	X	X
PASS-THROUGH from X to Y	L	H	L	H	X	X	0	X
PASS-THROUGH from Y to X	L	H	L	H	X	X	X	0
READ PORT X	L	H	X	X	1	X	1	1
READ PORT Y	X	X	L	H	X	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....−55°C to +125°C

Ambient Temperature with
Power Applied.. −10°C to +85°C

Supply Voltage on V_{DD} Relative to GND.........−0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State[10]...................................−0.5V to V_{CCQ} + 0.5V

DC Input Voltage[10]...............................−0.5V to V_{CCQ} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA.

Operating Range

Range	Ambient Temperature[11]	V_{DD}/V_{DDQ}
Com'l	0°C to +70°C	3.3V ± 5%

Notes:
2. X means "Don't Care." H means logic HIGH. L means logic LOW.
3. All inputs except OEX and OEY must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. OEX and OEY must be asserted to avoid bus contention during Write and Pass-Through cycles. For a Write and Pass-Through operation following a Read operation, OEX/OEY must be HIGH before the input data required setup time plus High-Z time for OEX/OEY and staying HIGH throughout the input data hold time.
5. Operation number 3 – 6 can be used in any combination.
6. Operation number 4 and 7, 3 and 8, 7 and 8 can be combined.
7. Operation number 5 can not be combined with operation number 7 or 8 because Pass-Through operation has higher priority over a READ operation.
8. Operation number 6 can not be combined with operation number 7 or 8 because Pass-Through operation has higher priority over a READ operation.
9. This device contains circuitry that will ensure the outputs will be in High-Z during power-up
10. Minimum voltage equals −2.0V for pulse duration less than 20 ns.
11. T_A is the case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			3.135	3.465	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[12]			2.0	V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage[13]			–0.5	0.8	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{IN} ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{CC}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.0-ns cycle, 133 MHz		400	mA
			7.5-ns cycle, 100 MHz		350	mA
			10.0-ns cycle, 83MHz		300	mA
I_{SB}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected[14], V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speed grades		100	mA

Shaded areas contain advance information

Note:
12. Overshoot: V_{IH} ≤ +6.0V for t ≤ $t_{KC/2}$
13. Undershoot: V_{IL} ≤ -2.0V for t ≤ $t_{KC/2}$.
14. "Device Deselected" means the device is in Power -Down mode as defined in the truth table.

Capacitance[15]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, V_{CC} = 3.3V, V_{CCQ} = 3.3V	6	pF
C_{CLK}	Clock Input Capacitance		6	pF
$C_{I/O}$	Input/Output Capacitance		8	pF

AC Test Loads and Waveforms[16]

(a)   (b)   1350B-2
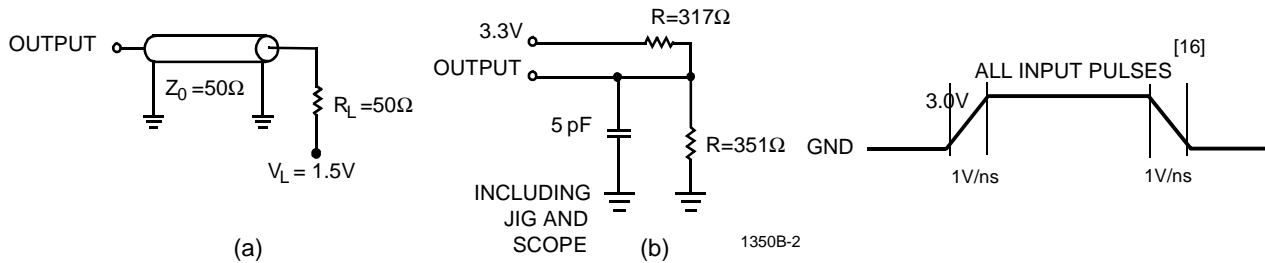
Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Units	Notes
Thermal Resistance (Junction to Ambient)	(@200lfm) Single-layer printed circuit board	Θ_{JA}	40	°C/W	15
Thermal Resistance (Junction to Ambient)	(@200lfm) Four-layer printed circuit board	Θ_{JC}	35	°C/W	15
Thermal Resistance (Junction to Board)	Bottom	Θ_{JA}	23	°C/W	15
Thermal Resistance (Junction to Case)	Top	Θ_{JC}	9	°C/W	15

Notes:
15. Tested initially and after any design or process change that may affect these parameters.
16. AC test conditions assume signal transition time of 1 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading shown in part (a) of AC Test Loads.

## Switching Characteristics Over the Operating Range[16, 17, 18]

| Parameter	Description	-133 Min.	-133 Max.	-100 Min.	-100 Max.	-80 Min.	-80 Max.	Unit
Clock								
t_{KC}	Clock cycle time	7.5		10		12		ns
t_{KH}	Clock HIGH time	3.0		3.5		4.0		ns
t_{KL}	Clock LOW time	3.0		3.5		4.0		ns
Output times								
t_{KQ}	Clock to output valid		4.0		5.0		6.0	ns
t_{KQX}	Clock to output invalid	1.5		1.5		1.5		ns
t_{KQLZ}	Clock to output in Low-Z[19]	0		0		0		ns
t_{KQHZ}	Clock to output in High-Z[19]		3.0		3.0		3.0	ns
t_{OEQ}	$\overline{OEX}/\overline{OEY}$ to output valid		4.0		5.0		6.0	ns
t_{OELZ}	$\overline{OEX}/\overline{OEY}$ to output in Low-Z[19]	0		0		0		ns
t_{OEHZ}	$\overline{OEX}/\overline{OEY}$ to output in High-Z[19]		3.0		3.0		3.0	ns
Setup times								
t_S	Addresses, Controls and Data In	1.5		1.5		2.0		ns
Hold times								
t_H	Addresses, Controls and Data In	0.5		0.5		0.5		ns

Shaded areas contain advance information.

Notes:

17. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
19. This parameter is sampled and not 100% tested.
20. $\overline{CE}$ LOW means (CE1X and CE1Y) equals LOW and ($\overline{CE2X}$ and $\overline{CE2Y}$) equals HIGH. $\overline{CE}$ HIGH means ($\overline{CE1X}$ and $\overline{CE1Y}$) equals HIGH or ($\overline{CE2X}$ and $\overline{CE2Y}$) equals LOW.

Switching Waveforms [20]

READ CYCLE TIMING FROM BOTH PORTS (WEX, WEY, PTX, PTY HIGH)[19]
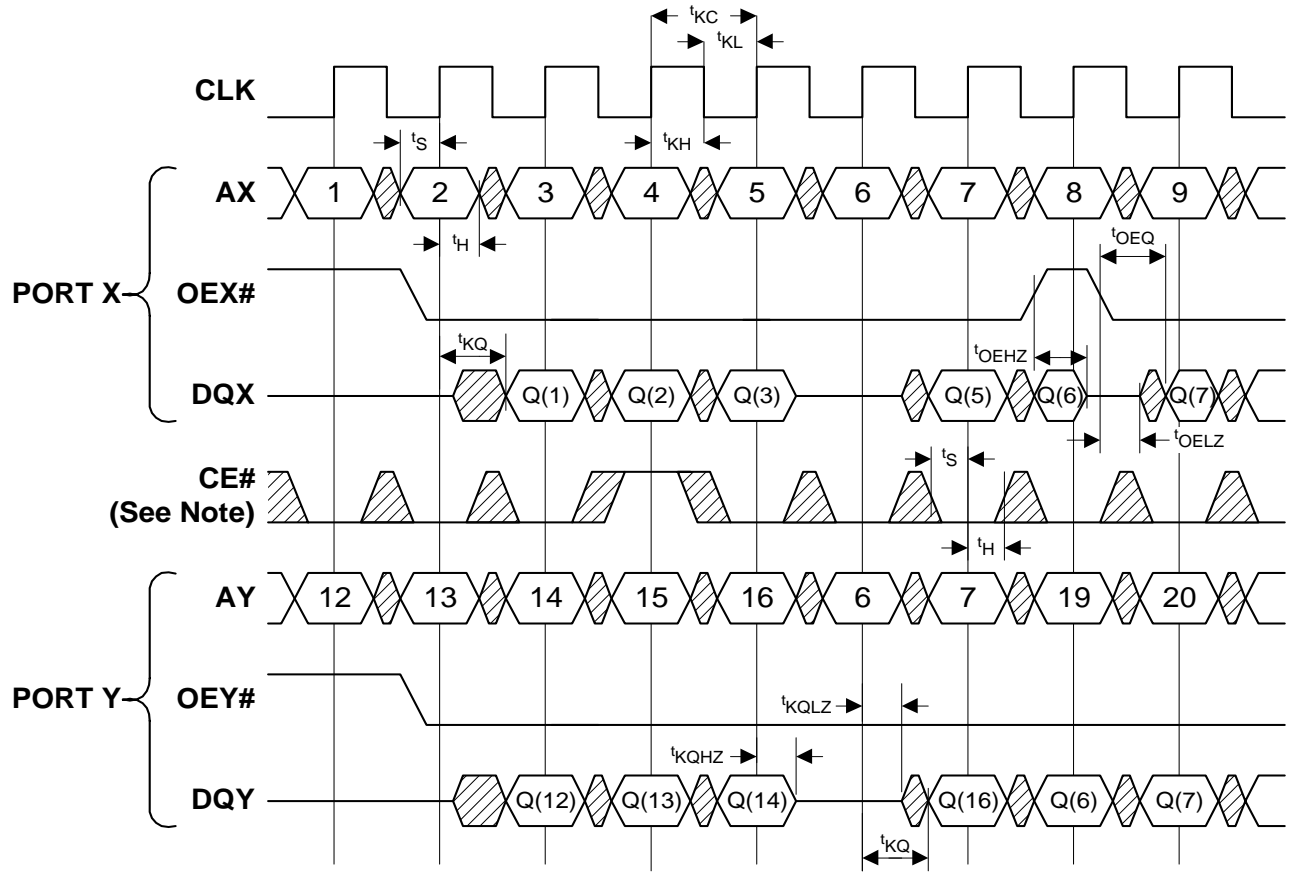
Switching Waveforms (continued)[20]

WRITE CYCLE TIMING TO BOTH PORTS ($\overline{\text{PTX}}$, $\overline{\text{PTY}}$ HIGH)[19]

PORT Y TAKES
PRIORITY OVER PORT X
WHEN AX=AY AND
WRITING TO BOTH
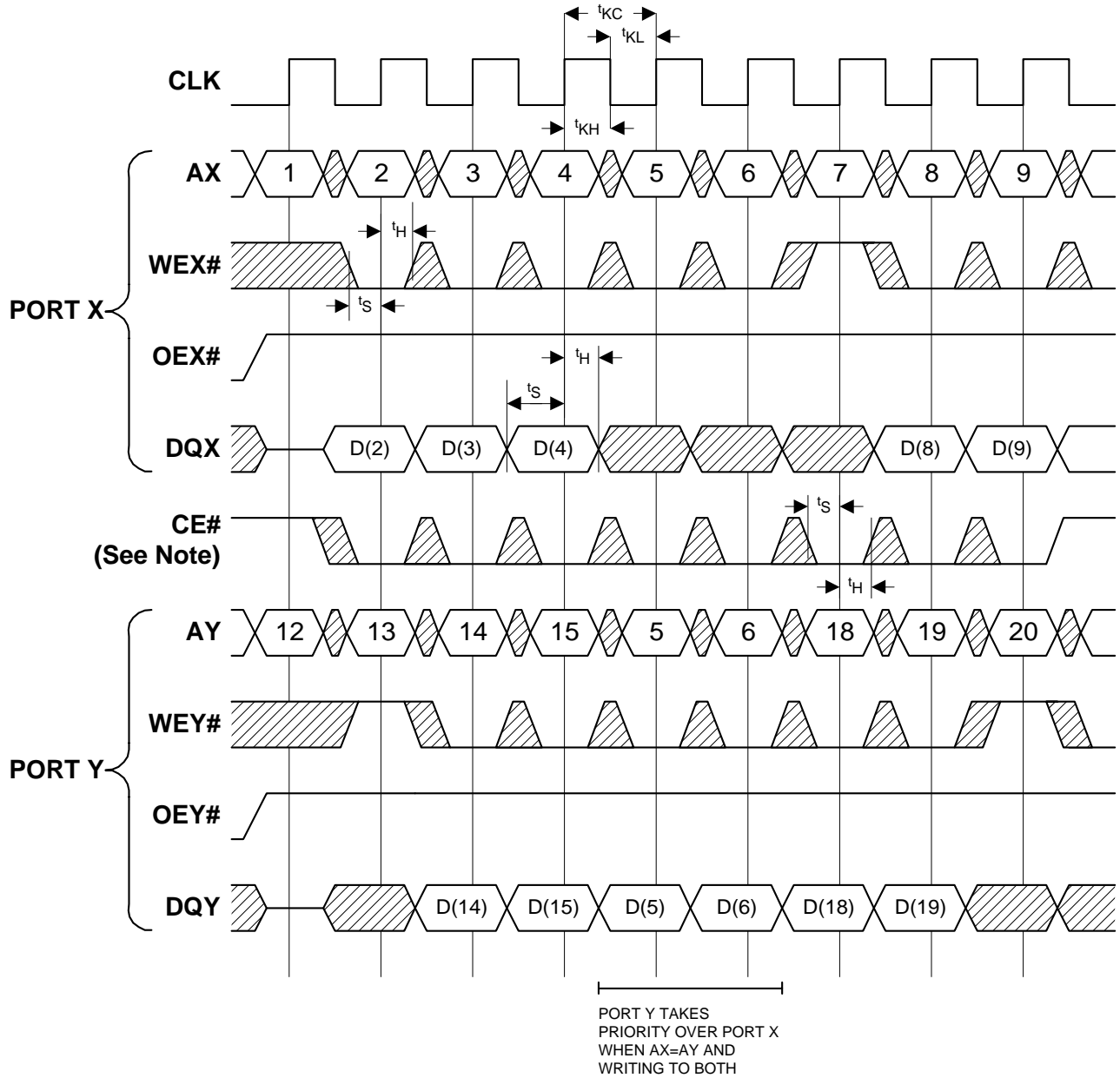
Switching Waveforms (continued)[20]

WRITE TO PORT X AND PASS-THROUGH TO PORT Y[19]
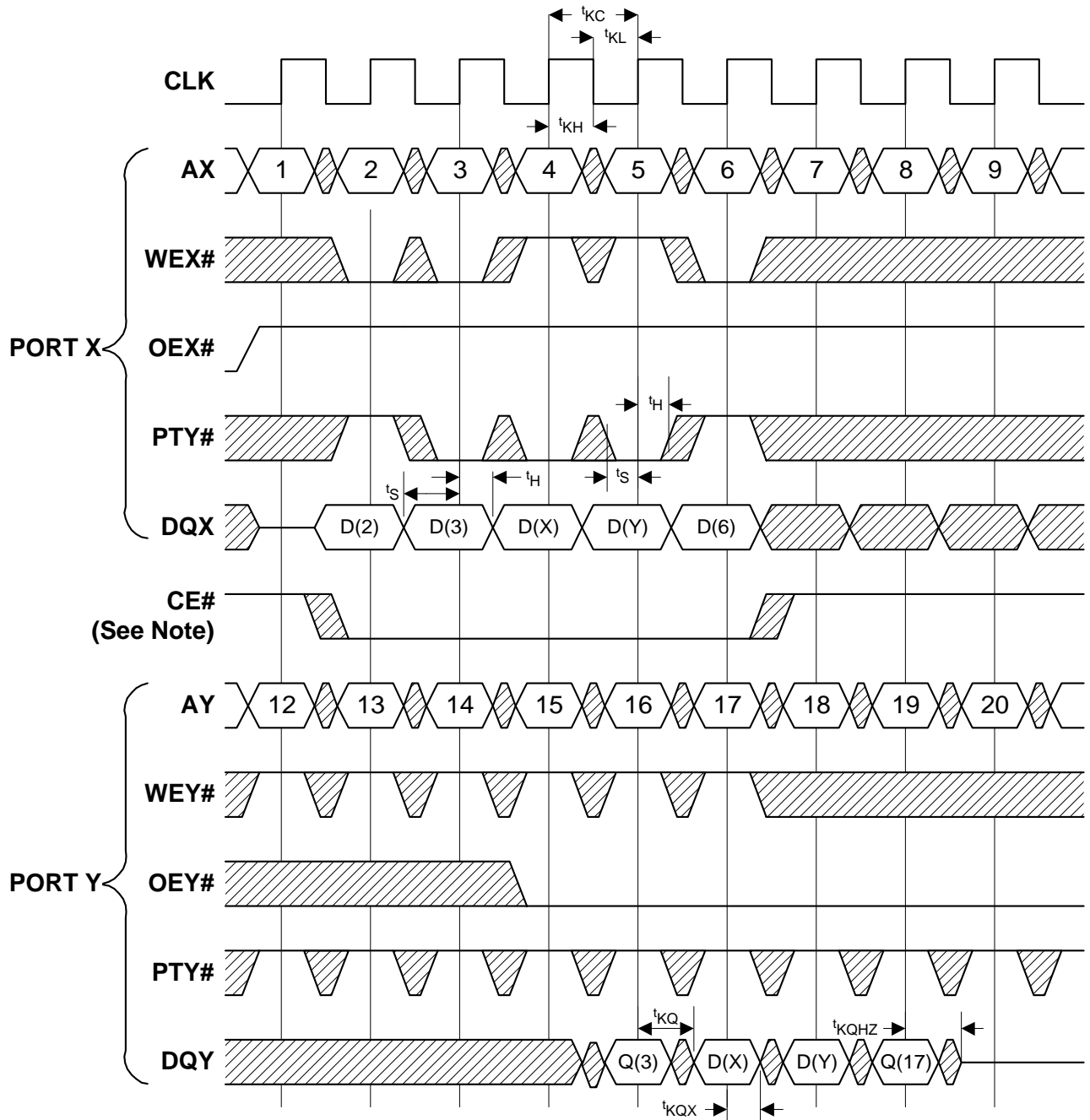
Switching Waveforms (continued)[20]

## COMBINATION READ/WRITE WITH SAME ADDRESS ON EACH PORT
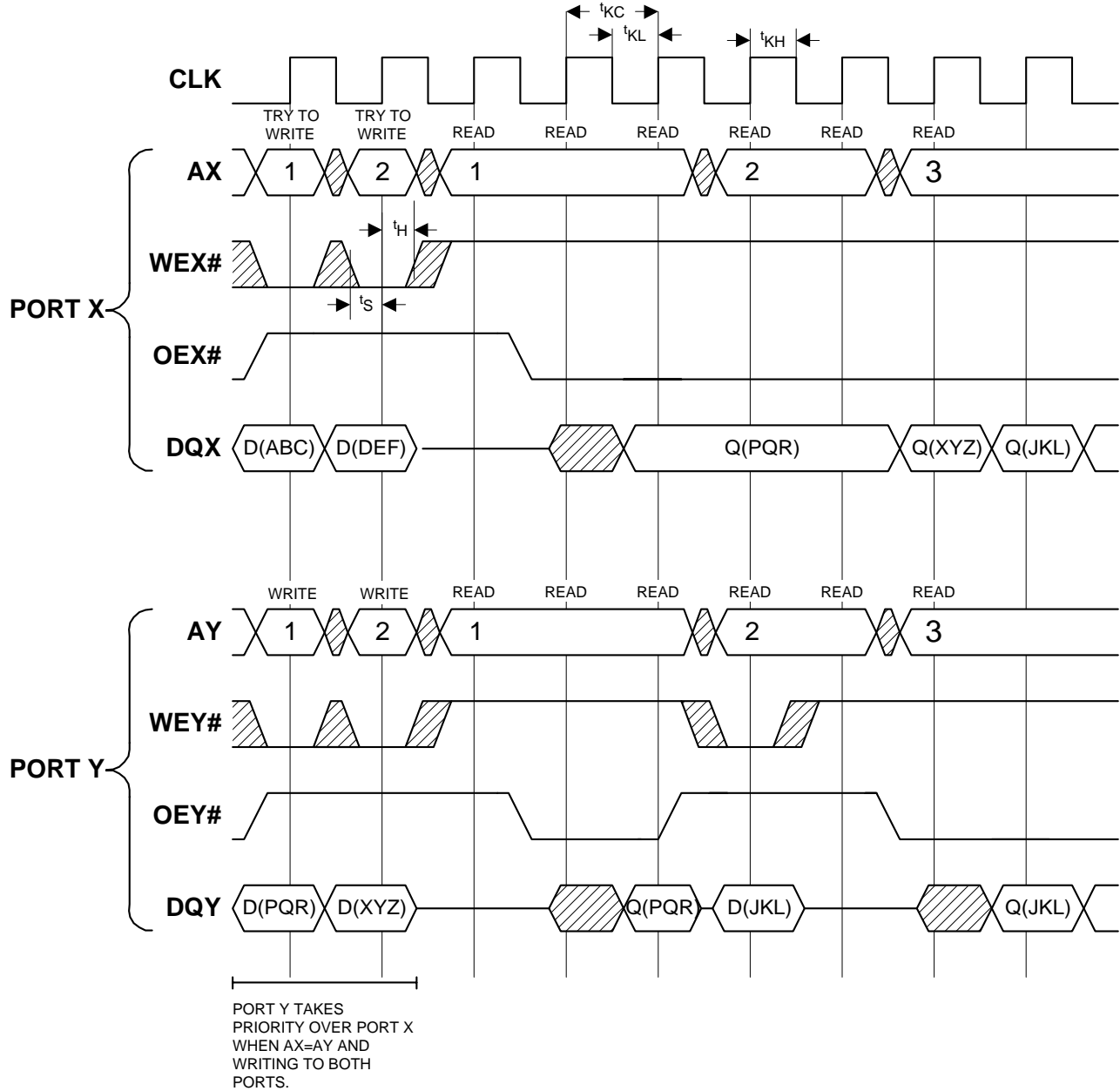
PTX# = PTY# = HIGH
D(Value) = Value is the input of the data port.
Q(Value) = Value is the output of the data port.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1300A-133AC	ACx	176 Pin TQFP	Commercial
100	CY7C1300A-100AC			
83	CY7C1300A-83BGC			
Shaded areas contain advance information				

Package Diagram

176-Lead Thin Quad Flat Pack (24x24x1.4 mm) A176
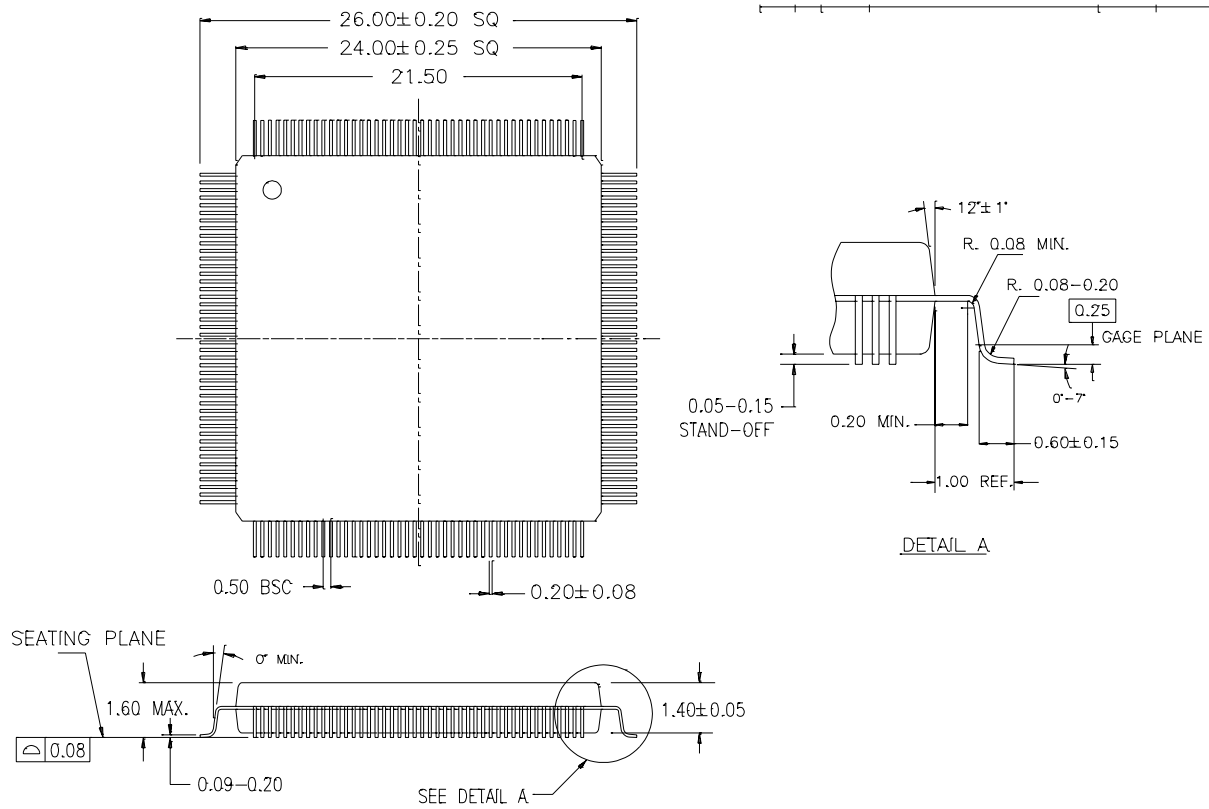
Document Title: CY7C1300A - 128K x 36 Dual I/O Dual Address Synchronous SRAM
Document Number: 38-05075

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107304	06/08/01	NSL	New Data Sheet