1.6X LINEAR FAN DRIVER WITH VOUT FULLY ON CONTROL

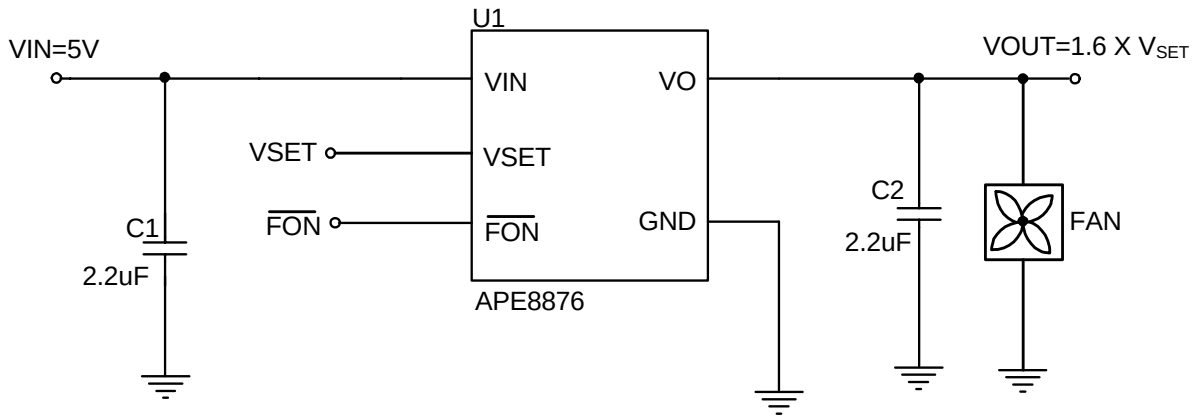
FEATURES

- **Low Dropout Voltage: 200mV@0.6A**
- **VO Follows 1.6 Times of VSET**
- **$\overline{FON}$ Pin to Turn VO Fully On**
- **Stable with Low ESR Ceramic Capacitors**
- **Current-Limit and Thermal Shutdown Protection**
- **TSOT-26 & SO-8 Pb-Free Package**

DESCRIPTIOON

The APE8876 is a low dropout linear regulator which is designed to power a DC fan and delivers up to 600mA output current. The output voltage follows the 1.6 times of VSET voltage and typical dropout voltage is only 200mV (typical) at 600mA output current. The VSET voltage can form 0.1V to 3.3V to guarantee VOUT 1.6 times of VSET. A $\overline{FON}$ pin turns VOUT output fully on when given low. The features of current limit (with fold back current) and over temperature protection protect the device against current over-loads and over temperature. The APE8876 is available in a TSOT-26 & SO-8 package.

TYPICAL APPLICATION



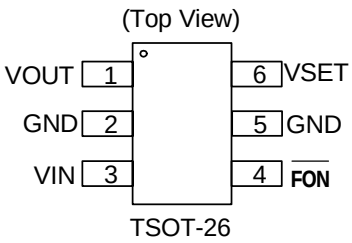
ORDERING / PACKAGE INFORMATION

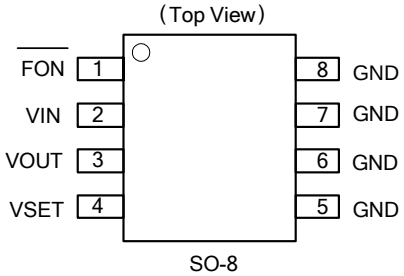
APE8876X

Package Type

TY : TSOT-26

M : SO-8





ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN Supply Voltage (V_{IN}) ---------- -0.3 to 6.5V

$\overline{FON}$ Voltage ($V_{\overline{FON}}$) ---------- -0.3 to VIN

VSET Voltage (V_{SET}) ---------- -0.3 to VIN

Power Dissipation (P_D) ---------- Internally limited

Storage Temperature Range (T_{ST}) ---------- -65 to +150°C

Junction Temperature Range (T_J) ---------- -40 to +125°C

Operating Temperature Range (T_{OP}) ---------- -40 to +85°C

Thermal Resistance from Junction to Case(Rth_{JC})

TSOT-26 50°C/W

SO-8 25°C/W

Thermal Resistance from Junction to Ambient(Rth_{JA})

TSOT-26 100°C/W

SO-8 70°C/W

Note: Rth_{JA} is measured with the PCB copper area approximately 1.5 in^2 (Multi-layer) that connect to GND Pins.

ELECTRICAL SPECIFICATIONS

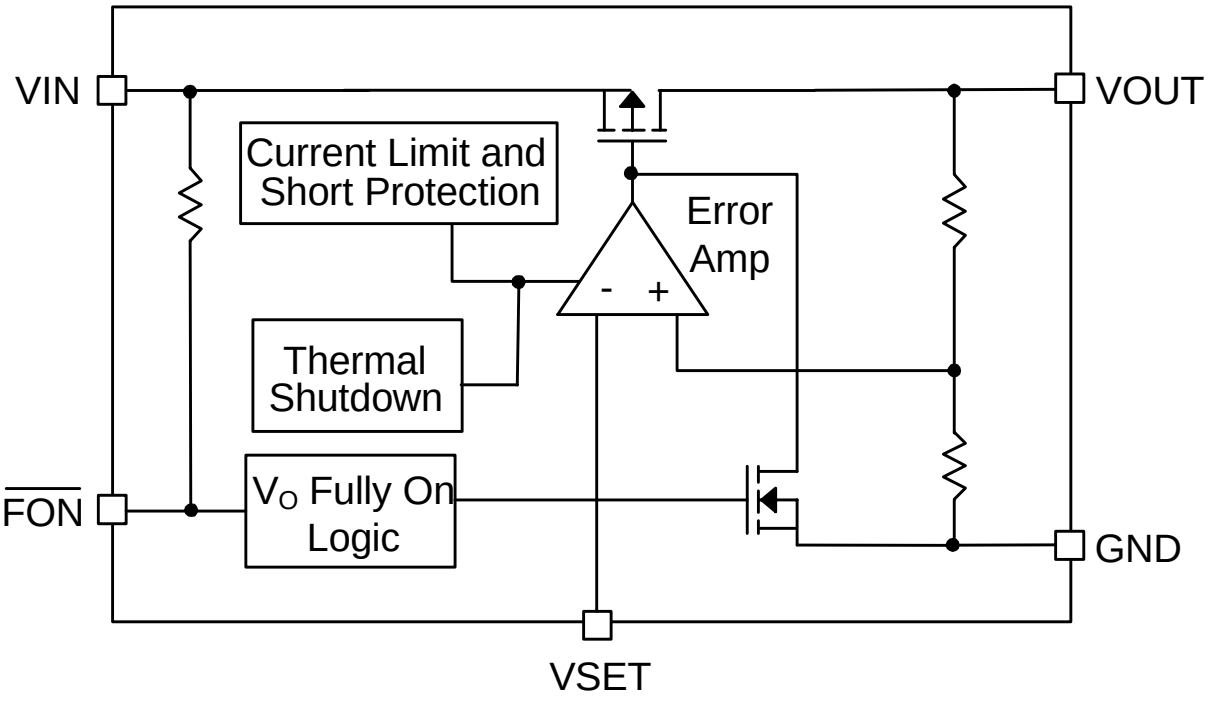
(V_{SET} = 2V, V_{IN} = 5V, I_{OUT} = 0.5A, C_{IN}=C_{OUT}=2.2uF, T_A=25°C unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
VIN Supply Voltage Range	V_{IN}		4.5	-	6	V
Quiescent Current	I_{CCQ}	No Load	-	50	80	uA
Output Voltage/V_{SET} Voltage	V_O/V_{SET}	V_{IN}=5.5V, V_{SET}=1V~3.3V	1.552	1.6	1.648	V/V
Line Regulation		V_{IN}=4.5V to 5.5V	-	0.2	0.5	%
Load Regulation		I_{OUT} =10mA ~ 0.6A	-	30	60	mV
Dropout Voltage	V_{Drop}	I_{OUT} =0.6A, V_{SET}=3.3V	-	200	320	mV
Current Limit	I_{Limt}		700	-	-	mA
Short Circuit Current	I_{Short}	Vo<0.6V	-	250	-	mA
VSET Voltage Range	V_{SET}		0.1	-	3.3	V
VSET Pin Current	I_{SET}	V_{SET}=5V	-	80	200	nA
$\overline{FON}$ Pin Logic Threshold Voltage	V_{FON-H}	Normal Operating	2	-	-	V
	V_{FON-L}	Regulator Fully On	-	-	0.8	V
$\overline{FON}$ Pin Bias Current	I_{FONH}	$\overline{FON}$ = V_{IN}	-	0.003	0.1	μA
	I_{FONL}	$\overline{FON}$ = 0V	-	1	5	
Thermal Shutdown Temp	T_{SD}		-	150	-	°C
Thermal Shutdown Hysteresis			-	30	-	°C

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VIN	IC power supply pin.
$\overline{\text{FON}}$	$\overline{\text{FON}}$ Input. Pulling this pin below 0.4V turns the regulator fully on. Internally pulled high.
VSET	This pin sets the output voltage. Its voltage can form 0.1V to 3.3V to guarantee VOUT 1.6 times of VSET
GND	Ground Pin
VOUT	Output Pin. Its voltage is 1.6 times of VSET

BLOCK DIAGRAM



FUNCTION DESCRIPTIONS

Output Voltage Regulation

The Output Voltage is set by VSET voltage. VOUT output voltage follows the 1.6 times of VSET voltage until it reaches VIN voltage.

Fully-On Control

If the $\overline{\text{FON}}$ pin logic level smaller than 0.8V, the output voltage can be promoted near to VIN voltage. Otherwise, VOUT is normal operating by $\overline{\text{FON}}$ larger than 2.0V.

FUNCTION DESCRIPTIONS

Current-Limit

The APE8876 monitors the current via the output PMOS and limits the maximum current to prevent load and APE8876 from damages during overload or short circuit conditions.

Short Current Protection

When the output voltage drops below 0.6V (typical), which is caused by over load or short circuit, the fold back current limit circuitry limits the output current to 250mA. The fold back current limit is used to reduce the power dissipation during short circuit condition.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APE8876. When the junction temperature exceeds +150°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 30°C, resulting in a pulsed output during continuous thermal overload conditions.

APPLICATION INFORMATION

Capacitor Selection

Normally, use a 2.2µF capacitor on the input and a 2.2µF capacitor on the output of the APE8876. In order to insure the circuit stability, the proper output capacitor value should be larger than 1uF. With X5R and X7R dielectrics, 2.2uF is sufficient at all operating temperatures.

Thermal Considerations

The APE8876 series can deliver a current of up to 600mA over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125° C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT})\ I_O$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$P_{D\ (MAX)} = (T_{J\ (MAX)} - T_A) / Rth_{JA}$$

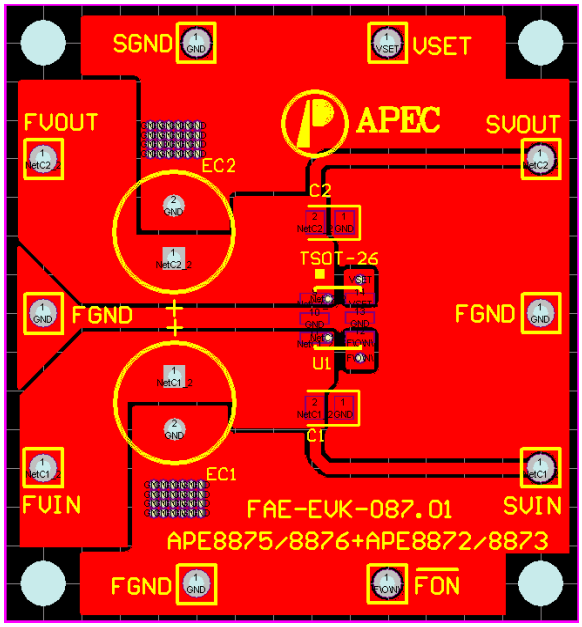
Where $T_{J\ (MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (Rth_{JA}) for TSOT-26 package at recommended minimum footprint is 100°C/W.

FUNCTION DESCRIPTIONS

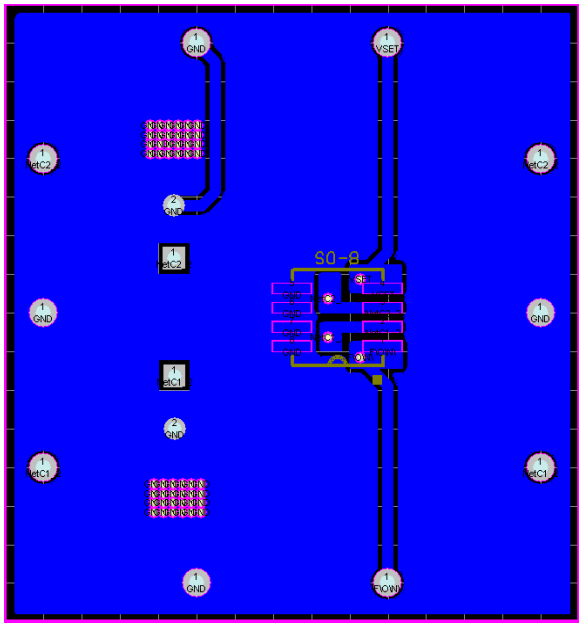
PCB Layout

1. Please place the input capacitors close to the VIN
2. Ceramic capacitors for load must be placed near the load as close as possible
3. To place APE8876 and output capacitors near the load is good for performance.
4. Large current paths that VIN and Output lines must have wide tracks.
5. GND connect large copper area can reduced IC temperature.

PCB Layout Guide

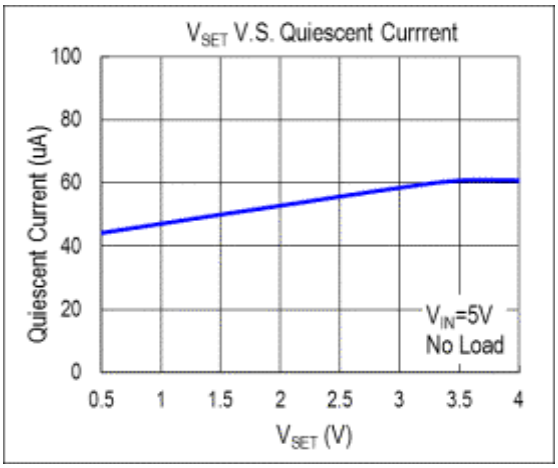


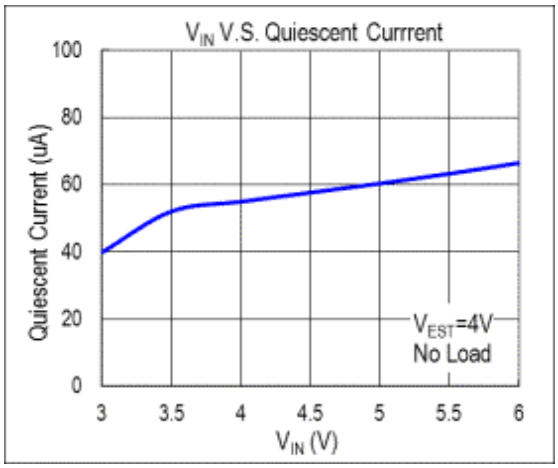
(Top View)

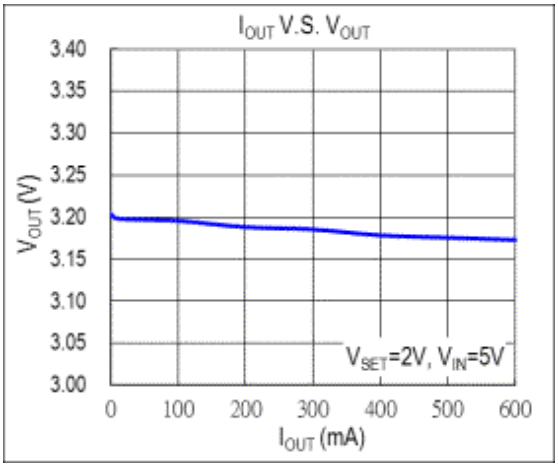


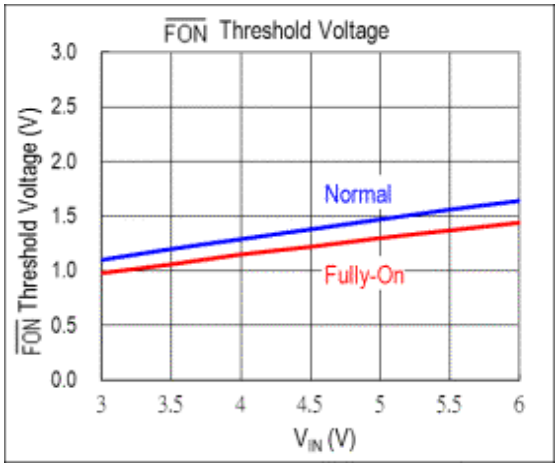
(Bottom View)

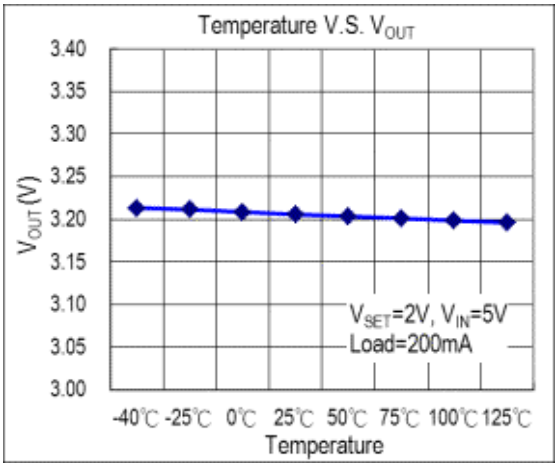
TYPICAL PERFORMANCE CHARACTERISTICS

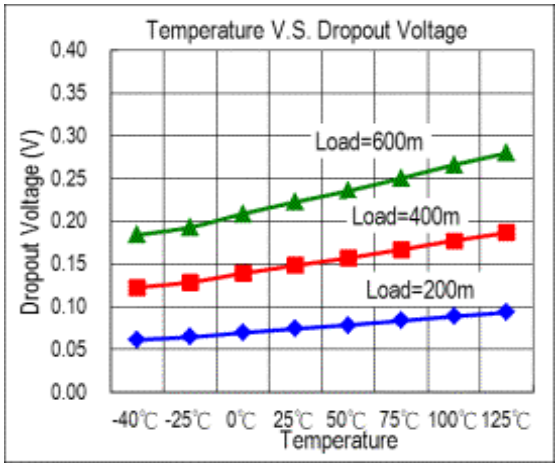












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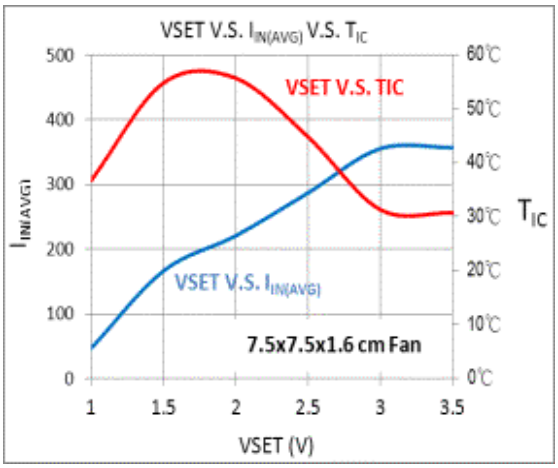
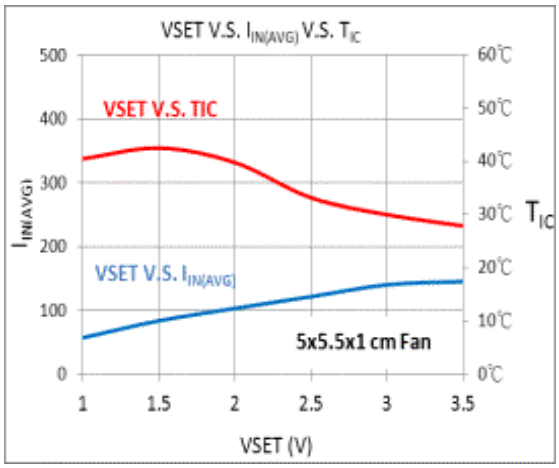
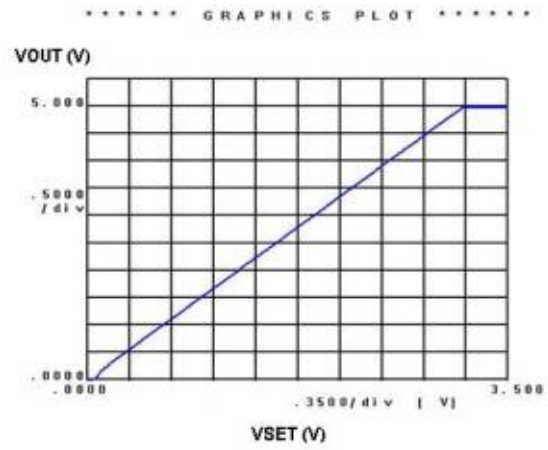
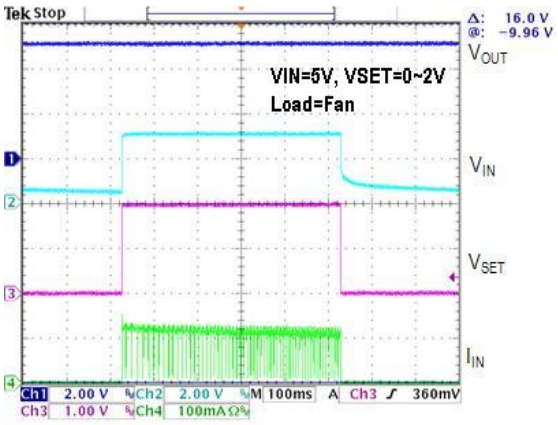


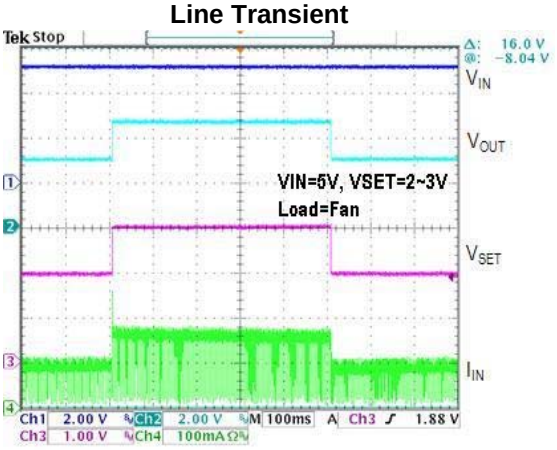




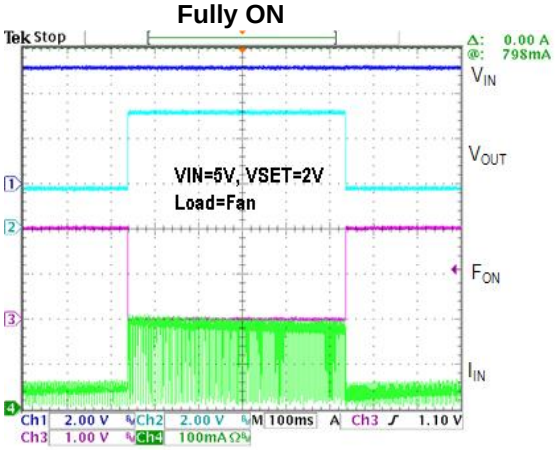
Line Transient



Line Transient

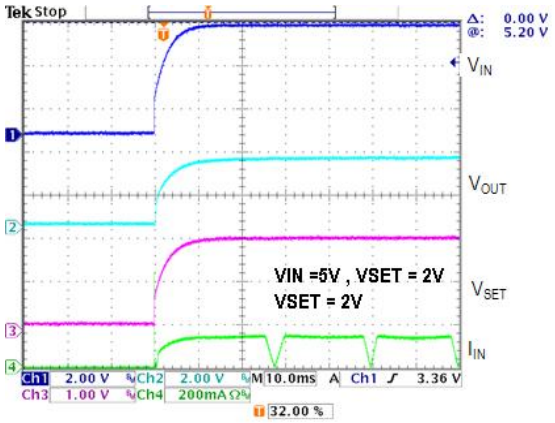


Fully ON



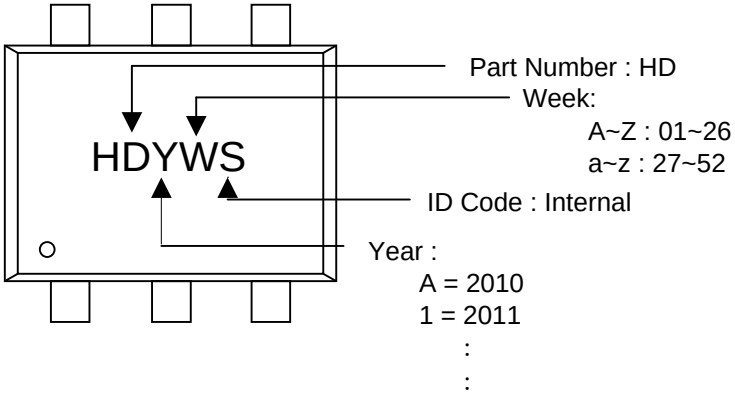
TYPICAL PERFORMANCE CHARACTERISTICS

Power ON

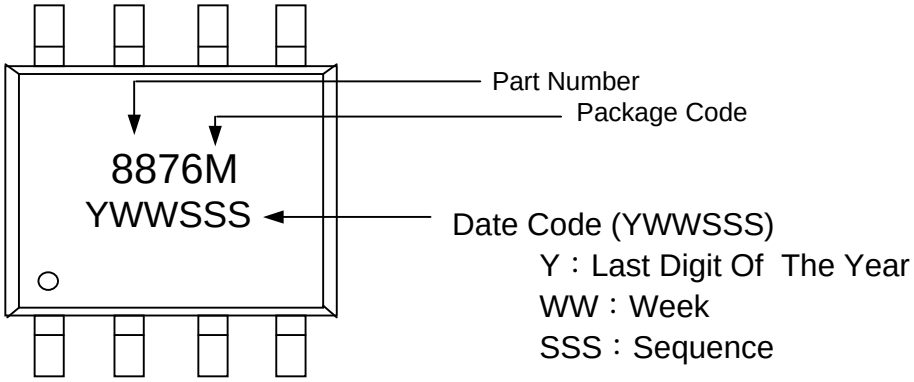


MARKING INFORMATION

TSOT-26

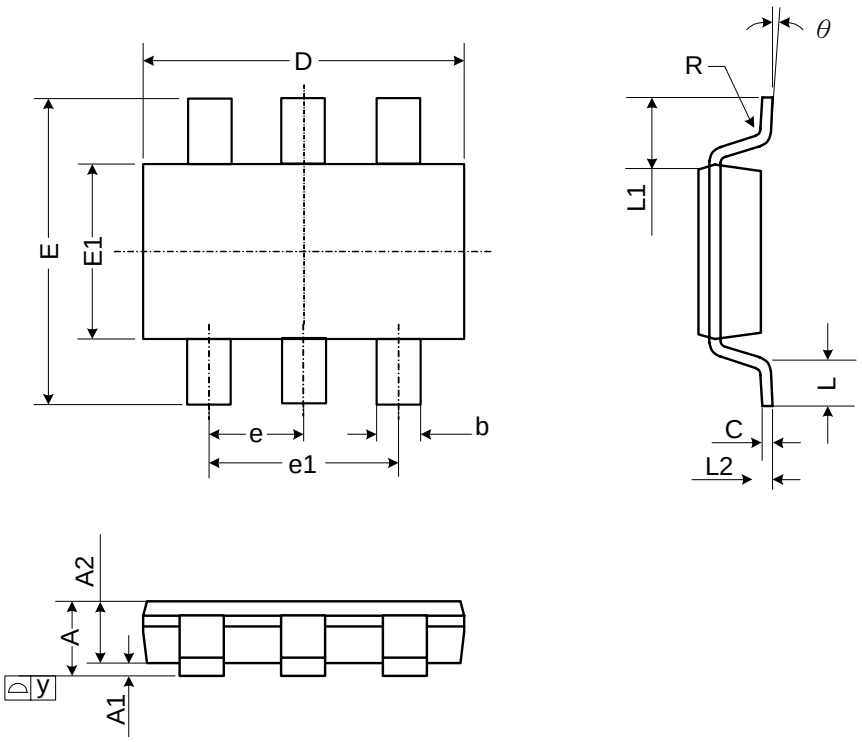


SO-8



PACKAGE OUTLINES

TSOT-26



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.10	-	-	0.043
A1	0.00	-	0.10	0	-	0.004
A2	0.70	0.90	1.00	0.028	0.035	0.039
b	0.30	0.40	0.50	0.012	0.016	0.020
C	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.95 BSC.			0.037 BSC.		
e1	1.90 BSC.			0.075 BSC.		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF.			0.024 REF.		
L2	0.25 BSC.			0.010 BSC.		
y	-	-	0.10	-	-	0.004
R	0.10	-	-	0.004	-	-
θ	0°	-	8°	0°	-	8°

JEDEC outline: MO-193 AA