High Efficiency SuperCap Charger for Photovoltaic Sources

DESCRIPTION

The TS52003 is a DC/DC synchronous switching Super Capacitor Charger with fully integrated power switches, internal compensation, and full fault protection. The TS52003 utilizes a temperature-independent photovoltaic Maximum Power Point Tracking (MPPT-Lite™) calculator to optimize power output from the source during Full-Charge mode. The switching frequency of 1MHz enables the use of small filter components, which result in smaller board space and reduced BOM costs.

In Full-Charge mode the duty cycle is controlled by the MPPT-Lite™ regulator. Once termination voltage is reached, the regulator operates in voltage mode. When the regulator is disabled (EN is low), the device draws less than 15uA quiescent current from V_{OUT}.

The TS52003 integrates a wide range of protection circuitry; including input supply under-voltage lockout, output over-voltage protection, current limit, and thermal shutdown.

The TS52003 includes supervisory reporting through the nFLT (Inverted Fault) open drain output to interface other components in the system. Device programming is achieved by an I²C interface through SCL and SDA pins.

FEATURES

- **Utilizes a temperature-independent PV MPPT-Lite™ regulation scheme**
- **VOUT reverse current blocking**
- **Wide input voltage range: 3.2V to 7.2V**
- Up to 1.5A continuous output current
- Programmable temperature-compensated termination voltage with a ± 1% tolerance
- User programmable termination voltage
- High efficiency – up to 92% at typical load
- Current mode PWM control in constant voltage
- Input supply under voltage lockout
- Full protection for V_{OUT} over-voltage
- Device over-current and over-temperature protection
- I2C program interface with EEPROM registers
- V_{OUT} reverse current blocking
- Charge status indication

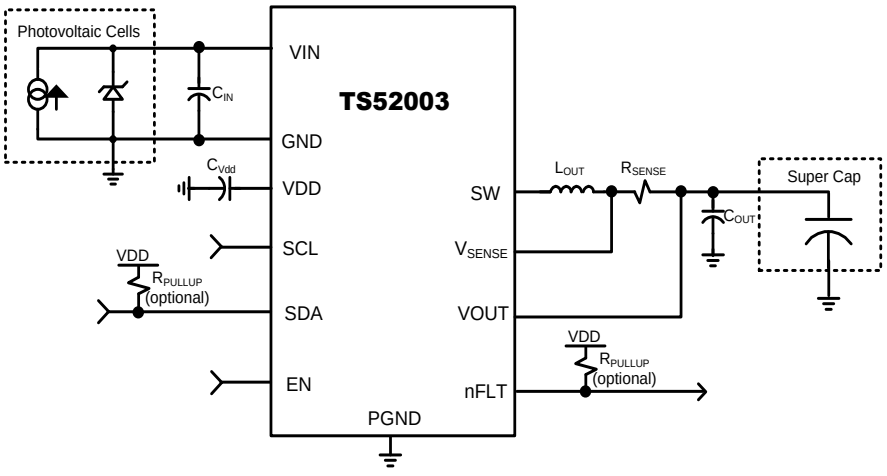
SUMMARY SPECIFICATIONS

- Packaged in a 16pin QFN (4x4)

APPLICATIONS

- Off-grid systems
- Wireless sensor networks
- Smoke detectors
- HVAC controls

TYPICAL APPLICATION



PINOUT

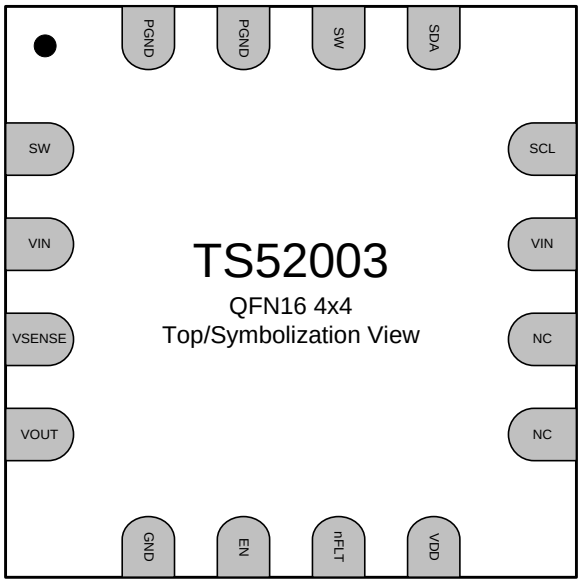


Figure 1b: Package Pinout Diagram

PIN DESCRIPTION

Pin Symbol	Pin #	Function	Description
SW	1	Switching Voltage Node	Connected to 4.7uH (typical) inductor
VIN	2	Photovoltaic Input Voltage	Input voltage
VSENSE	3	Current Sense Positive Input	Positive input for the MPP current loop.
VOUT	4	Super Cap Voltage	Regulator Feedback Input
GND	5	GND	Primary ground for the majority of the device except the low-side power FET.
EN	6	Enable Input	Above 2.2V the device is enabled. GND the pin to disable the device. Includes internal pull-up.
nFLT	7	Inverted Fault	Open-drain output.
VDD	8	Internal 3.3V Supply Output	Connected to 100nF capacitor to GND
	9	Unused	GND in application
	10	Unused	GND in application
VIN	11	Photovoltaic Input Voltage	Input voltage
SCL	12	Clock Input	I^2C clock input.
SDA	13	Data Input/Output	I^2C data open-drain output.
SW	14	Switching Voltage Node	Connected to 4.7uH (typical) inductor
PGND	15	Power GND	GND supply for internal low-side FET/integrated diode
PGND	16	Power GND	GND supply for internal low-side FET/integrated diode

FUNCTIONAL BLOCK DIAGRAM

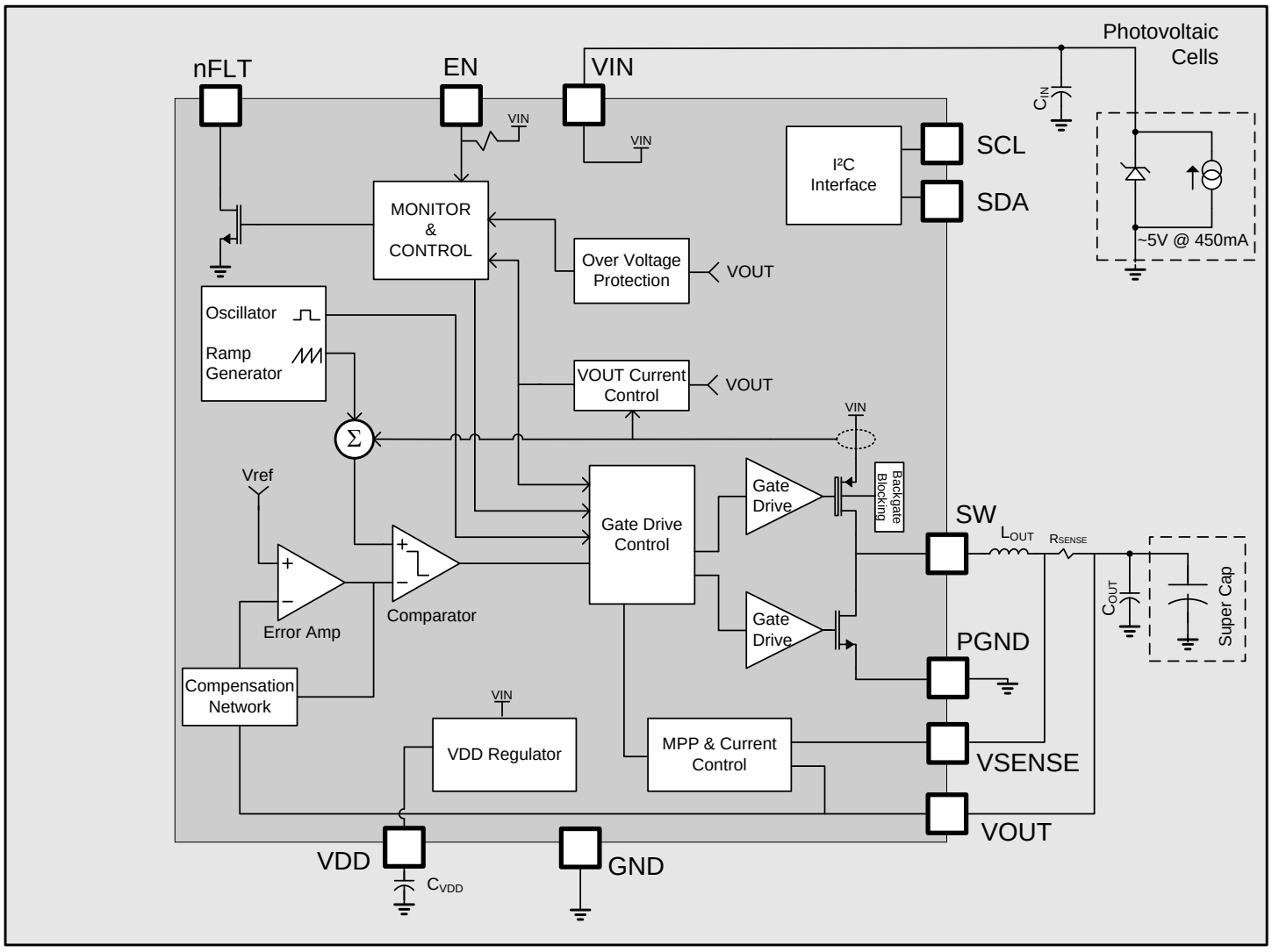


Figure 2: TS52003 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Over operating free–air temperature range unless otherwise noted(1,2,3)

Parameter	Range	Unit
VIN, EN, nFLT, SCL, SDA, VOUT, VSENSE	-0.3 to 8	V
SW	-1 to 8.8	V
VDD	-0.3 to 3.6	V
Operating Junction Temperature Range, T_J	-40 to 125	°C
Storage Temperature Range, T_{STG}	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Machine Model	+/-200	V
Lead Temperature (soldering, 10 seconds)	260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	50	°C/W

Note 1: Assumes 4x4 QFN-16 in 1 in^2 area of 2 oz copper and 25°C ambient temperature.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Photovoltaic Input Operating Voltage	3.2	5.3	7.2	V
R_{SENSE}	Sense Resistor		50		mΩ
L_{OUT}	Output Filter Inductor Typical Value (Note 1)		4.7		uH
C_{OUT}	Output Filter Capacitor Typical Value (Note 2)		4.7		uF
$C_{OUT-ESR}$	Output Filter Capacitor ESR			100	mΩ
C_{IN}	Input Supply Bypass Capacitor Typical Value (Note 3)	3.3	10		uF
C_{VDD}	VDD Supply Bypass Capacitor Value (Note 2)	70	100	130	nF
T_A	Operating Free Air Temperature	-40		85	°C
T_J	Operating Junction Temperature	-40		125	°C

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple.
Note 2: For best performance, a low ESR ceramic capacitor should be used.
Note 3: For best performance, a low ESR ceramic capacitor should be used. If C_{IN} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{IN}.

CHARACTERISTICS

Electrical Characteristics, T_J = -40C to 125C, VIN = 5.3V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN Supply Voltage						
VIN	Photovoltaic Voltage Input		3.2	5.3	7.2	V
$I_{CC-NORM}$	Quiescent current Normal Mode	I_{LOAD} = 0A		3		mA
$I_{CC-DISABLE}$	Quiescent current Disable Mode	EN = 0V		15	50	uA
VOUT Leakage						
$I_{OUT-LEAK}$	Leakage Current	EN = 0V, Vout = 2.7V			10	uA
$I_{OUT-BACK}$	Reverse Current	Vout > VIN, Vout = 2.7V			10	uA
VIN Under-Voltage Lockout						
VIN_{-UV}	Input Supply Under-Voltage Threshold	VIN Increasing		3.15		V
VIN_{-UV_HYST}	Input Supply Under-Voltage Threshold Hysteresis		100	200		mV
OSC						
F_{OSC}	Oscillator Frequency		0.9	1	1.1	MHz
nFLT Open Drain Output						
T_{nFLT}	nFLT Release Timer			0		ms
$I_{OH-nFLT}$	High-Level Output Leakage	V_{nFLT} = 5.3V		0.1		uA
$V_{OL-nFLT}$	Low-Level Output Voltage	I_{nFLT} = -1mA			0.4	V
EN/SCL/SDA Input Voltage Thresholds						
V_{IH}	High Level Input Voltage		2.2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{HYST}	Input Hysteresis			200		mV
I_{IN-EN}	Input Leakage	V_{EN}=VIN		0.1		uA
		V_{EN}=0V		-2.0		uA
I_{IN-SCL}	Input Leakage	V_{SCL}=VIN		55		uA
		V_{SCL}=0V		-0.1		uA
I_{IN-SDA}	Input Leakage	V_{SDA}=VIN		0.1		uA
		V_{SDA}=0V		-0.1		uA
V_{OL-SDA}	Low-Level Output Voltage	I_{SDA} = -1mA			0.4	V
Thermal Shutdown						
TSD	Thermal Shutdown Junction Temperature		150	170		C
TSD_{HYST}	TSD Hysteresis			10		C

CHARGER CHARACTERISTICS

Electrical Characteristics, T_J = -40C to 125C, VIN = 5.3V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Charging Regulator: L=4.7uH and C=4.7uF						
I_{OUT-FC}	Output Current Limit in Full-Charge Mode	I_{OUT} = 1.5A	I_{OUT} - 10%	I_{OUT}	I_{OUT} + 10%	A
V_{OUT}	Termination Voltage Tolerance		V_{OUT} - 1%	V_{OUT}	V_{OUT} + 1%	V
t_{FC}	Full-Charge Timer		200		1400	min
R_{DSON}	High Side Switch On Resistance	I_{SW} = -1A, T_J=25C		250		mΩ
	Low Side Switch On Resistance	I_{SW} = 1A, T_J=25C		150		mΩ
I_{OUT}	Max Output Current			1.5		A
I_{OCD}	Over-Current Detect	HS switch current		2.5		A
V_{OUT-OV}	V_{OUT} Over-Voltage Threshold		101% V_{OUT}	102% V_{OUT}	103% V_{OUT}	
V_{OUT-OV_HYST}	V_{OUT} Over-Voltage Hysteresis		0.2% V_{OUT}	0.4% V_{OUT}	0.6% V_{OUT}	
$DUTY_{MAX}$	Max Duty Cycle			98		%

I²C INTERFACE TIMING REQUIREMENTS

Electrical Characteristics, T_J = -40C to 125C, VIN = 5.3V (unless otherwise noted)

Symbol	Parameter	Standard Mode		Fast Mode(1)		Unit
		Min	Max	Min	Max	
f_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		µs
t_{scl}	I²C clock low time	4.7		1.3		µs
t_{sp}(2)	I²C tolerable spike time	0	50	0	50	ns
t_{sds}	I²C serial data setup time	250		250		ns
t_{sdh}	I²C serial data hold time	0		0		µs
t_{icr}(2)	I²C input rise time		1000		300	ns
t_{icf}(2)	I²C input fall time		300		300	ns
t_{ocf}(2)	I²C output fall time; 10 pF to 400 pF bus		300		300	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup time	4.7		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold time	4		0.6		µs
t_{sps}(2)	I²C Stop condition setup time	4		0.6		µs

(1) The I²C interface will operate in either standard or fast mode.
(2) Parameters not tested in production.

FUNCTIONAL DESCRIPTION

The TS52003 is a fully-integrated super capacitor charger IC based on a highly-efficient switching topology. It includes a Maximum Power Point Tracking (MPPT) function to optimize its input voltage to extract the maximum possible power from a photovoltaic cell. It includes configurability for termination voltage and charge current. A 1 MHz internal switching frequency facilitates low-cost LC filter combinations.

When enabled, the TS52003 will provide the maximum power available from a photovoltaic cell until the output voltage reaches the termination point. At that point, it will begin to regulate voltage. It will do so until a fault is detected, it is disabled or the output voltage drops below the termination point.

INTERNAL PROTECTION DETAILS

Internal Current Limit
The current through the inductor is sensed on a cycle by cycle basis and if current limit is reached, it will abbreviate the cycle. Current limit is always active when the regulator is enabled.

Thermal Shutdown
If the temperature of the die exceeds 170C (typical), the SW outputs will tri-state to protect the device from damage. The nFLT and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160C (typical), the device will attempt to start up again. If the device reaches 170C, the shutdown/restart sequence will repeat.

VIN Under-Voltage Lockout
The device is held in the off state until VIN reaches 3.15V. There is a 200mV hysteresis on this input, which requires the input to fall below 2.95V before the device will disable.

VOUT Over-Voltage Protection
The TS52003 has an output protection circuit designed to shutdown the charging profile if the output voltage is greater than the termination voltage. The termination voltage can change based on user programming, so the protection threshold is set to 2% above the termination voltage. Shutting down the charging profile puts the TS52003 in a fault condition.

SERIAL INTERFACE

The TS52003 features an I²C slave interface which offers advanced control and diagnostic features. I²C operation offers configuration control for termination voltages, charge currents, and charge timeouts. I²C operation also offers fault and warning indicators. Whenever a fault is detected, the associated status bit in the STATUS register is set and the nFLT pin is pulled low. Whenever a warning is detected, the associated status bit in the STATUS register is set, but the nFLT pin is not pulled low. Reading of the STATUS register resets the fault and warning status bits, and the nFLT pin is released after all fault status bits have been reset.

I²C SUBADDRESS DEFINITION

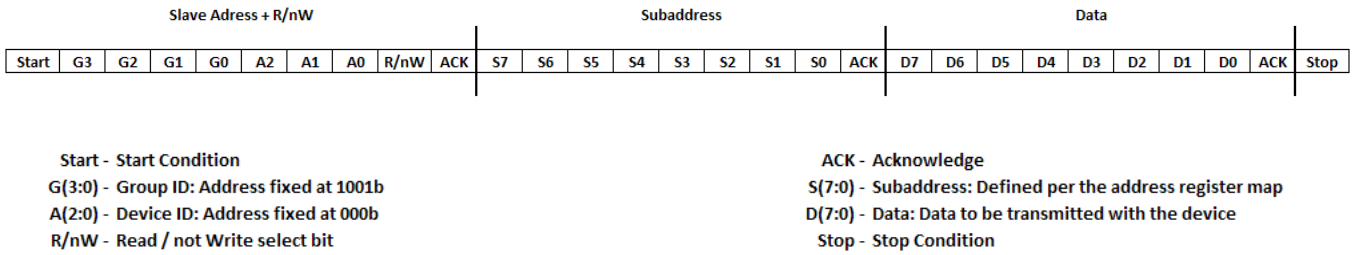


Figure 3: Sub-address in I²C Transmission

I²C BUS OPERATION

The TS52003 has a slave I²C interface that supports standard and fast mode data rates, auto-sequencing, and is compliant to I²C standard version 3.0.

I²C is a two-wire serial interface where the two lines are serial clock (SCL) and serial data (SDA). SDA must be connected to a positive supply through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. The device that initiates the I²C transaction becomes the master of the bus. Communication is initiated by the master sending a Start condition, a high-to-low transition on SDA, while the SCL line is high. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/nW). After receiving the valid address byte, the device responds with an acknowledge (ACK). An ACK is a low on SDA during the high of the ACK related clock pulse. On the I²C bus, during each clock pulse only one data bit is transferred. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as Start or Stop control commands. A low-to-high transition on SDA while the SCL input is high indicates a Stop condition and is sent by the master (see Figure 4).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The SDA line must be released by the transmitter before the receiver can send an ACK bit. The receiver that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. To ensure proper operation, setup and hold times must be met. An end of data is signaled by the master receiver to the slave transmitter by not generating an acknowledge after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. The transmitter must then release the data line to enable the master to generate a Stop condition.

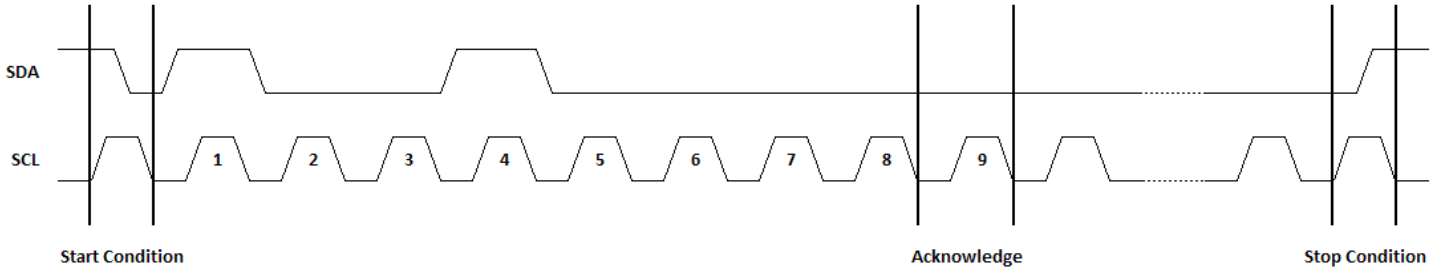


Figure 4: I²C Start / Stop Protocol

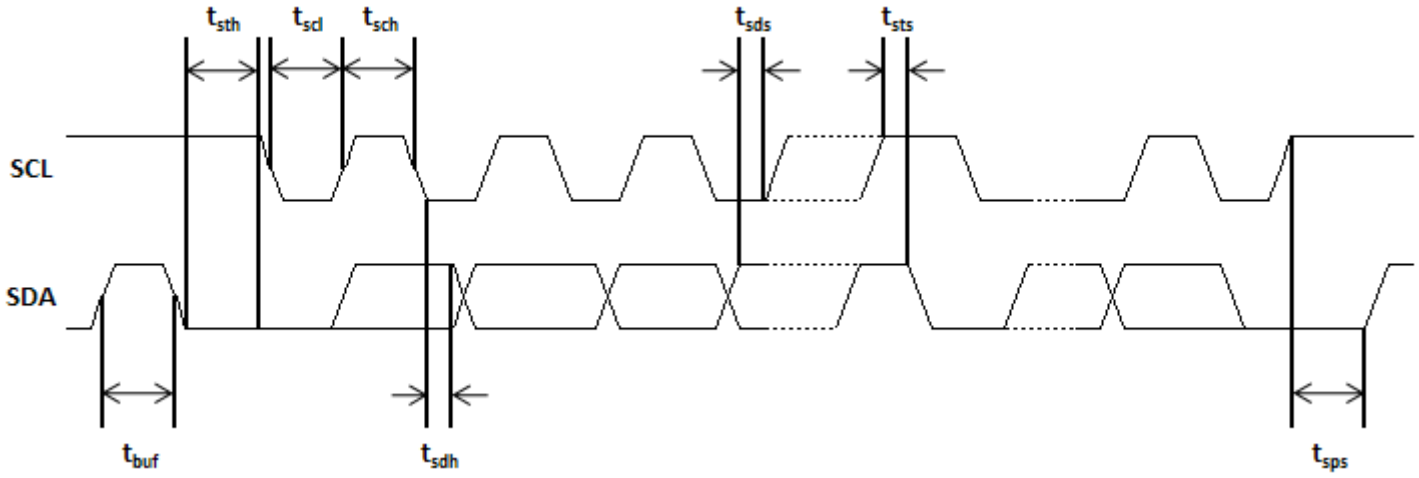


Figure 5: I²C Data Transmission Timing

REGISTER DESCRIPTION (Device Address = 0x48)

REGISTER	ADDRESS (HEX)	NAME	DEFAULT	DESCRIPTION
0	00	STATUS	0x00	Status bit register
1	N/A	N/A	N/A	Register not implemented
2	02	CONFIG1(1)	EEPROM	Configuration register
3	N/A	N/A	N/A	Register not implemented
4	04	CONFIG3(1)	EEPROM	Configuration register
5-16	N/A	N/A	N/A	Registers not implemented
17	11	CONFIG_ENABLE	0x00	Enable configuration register access
18	12	EEPROM_CTRL(1)	0x00	EEprom control register

STATUS REGISTER (STATUS)

Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VOUT_OV	Not Used	Not Used	Not Used	TSD	Not Used	VIN_UV	Not Used
READ/WRITE	R	R	R	R	R	R	R	R

FIELD NAME	BIT DEFINITION(2)
VOUT_OV	Vout over-voltage
TSD	Thermal shutdown
VIN_UV	VIN under-voltage

(1) CONFIG and EEPROM_CTRL registers are only accessible when CONFIG_ENABLE register is written.

(2) Fault is defined as VOUT_OV. Warnings are defined as TSD, and VIN_UV. Faults cause the nFLT pin to be pulled low, Warnings do not cause the nFLT pin to be pulled low. All status bits are cleared after register read access. nFLT pin will go high impedance (open drain output) after the status register has been read and all status bits have been reset.

CONFIGURATION REGISTER (CONFIG1)

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not Used		V_TERM [2:0]			Not Used		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FIELD NAME	BIT DEFINITION
V_TERM [2:0]	Voltage Termination configuration 000 – 2.48 V 001 – 2.54 V 010 – 2.60 V 011 – 2.66 V 100 – 2.68 V 101 – 2.72 V 110 – 2.74 V 111 – 4.92 V (Setting will not meet accuracy specifications)

CONFIGURATION REGISTER (CONFIG3)

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	MAX_CHRG_CURR [3:0]				Not Used			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FIELD NAME	BIT DEFINITION
MAX_CHRG_CURR[3:0]	Maximum charge current configuration 0000 – 50 mA 0001 – 100 mA 0010 – 200 mA 0011 – 300 mA 0100 – 400 mA 0101 – 500 mA 0110 – 600 mA 0111 – 700 mA 1000 – 800 mA 1001 – 900 mA 1010 – 1000 mA 1011 – 1100 mA 1100 – 1200 mA 1101 – 1300 mA 1110 – 1400 mA 1111 – 1500 mA

ENABLE CONFIGURATION REGISTER (CONFIG_ENABLE)

Address – 0x11h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	Not used	EN_CFG
READ/WRITE	R	R	R	R	R	R	R	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
EN_CFG	Enable access control bit for configuration registers 2 and 4 0 – Disable access 1 – Enable access

EEPROM CONTROL REGISTER (EEPROM_CTRL)

Address – 0x12h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	Not used	EE_PROG
READ/WRITE	R	R	R	R	R	R	R	R/W
RESET VALUE	0	0	0	0	0	0	0	0

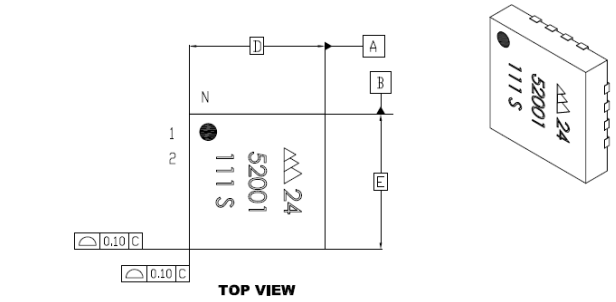
FIELD NAME	BIT DEFINITION
EE_PROG(1)	EEPROM program control bit for configuration registers 2 and 4 0 – Disable EEPROM programming 1 – Enable EEPROM programming with data from configuration registers 2 and 4

(1) EE_PROG Note: Inputs VIN and EN must be present for 200ms.

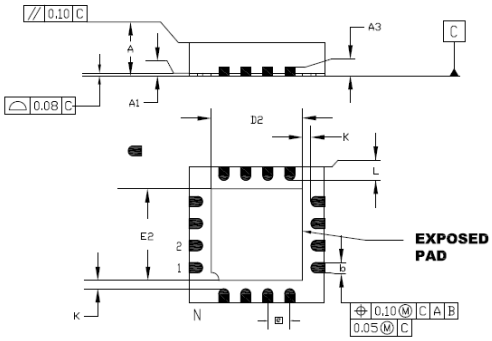
EXTERNAL COMPONENT SELECTION

The internal compensation is optimized for a 4.7uF output capacitor and a 4.7uH inductor. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic is recommended.

PACKAGE MECHANICAL DRAWINGS

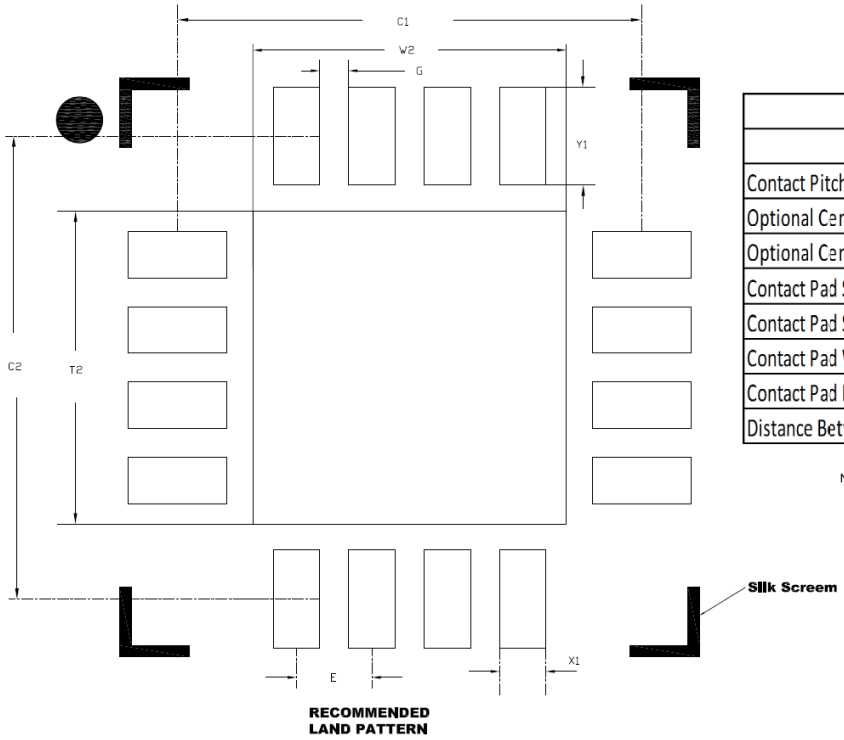


TOP VIEW



BOTTOM VIEW

Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	2.55	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	2.55	2.70	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2	-	-	2.70
Optional Center Pad Length	T2	-	-	2.70
Contact Pad Spacing	C1	-	4.00	-
Contact Pad Spacing	C2	-	4.00	-
Contact Pad Width (X16)	X1	-	-	0.40
Contact Pad Length (X16)	Y1	-	-	0.85
Distance Between Pads	G	0.25	-	-

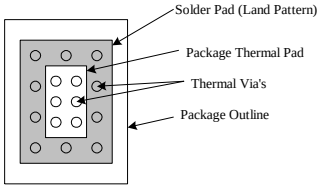
Notes:

Dimensions and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Refernce Dimension, usually without tolerance, for information only.

APPLICATION USING A MULTI-LAYER PCB

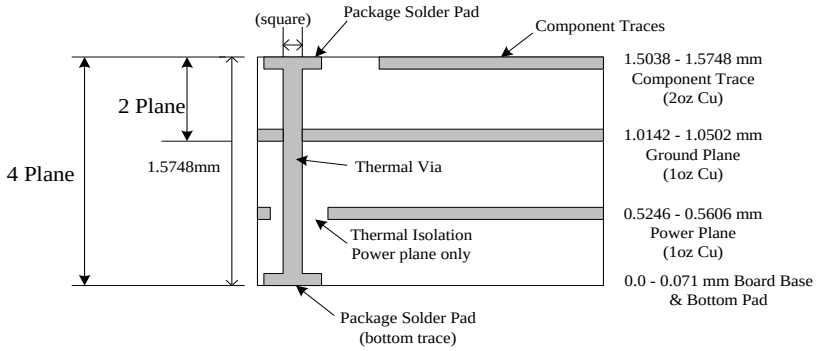
To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following are guidelines for mounting the exposed pad IC on a Multi-Layer PCB with ground a plane.



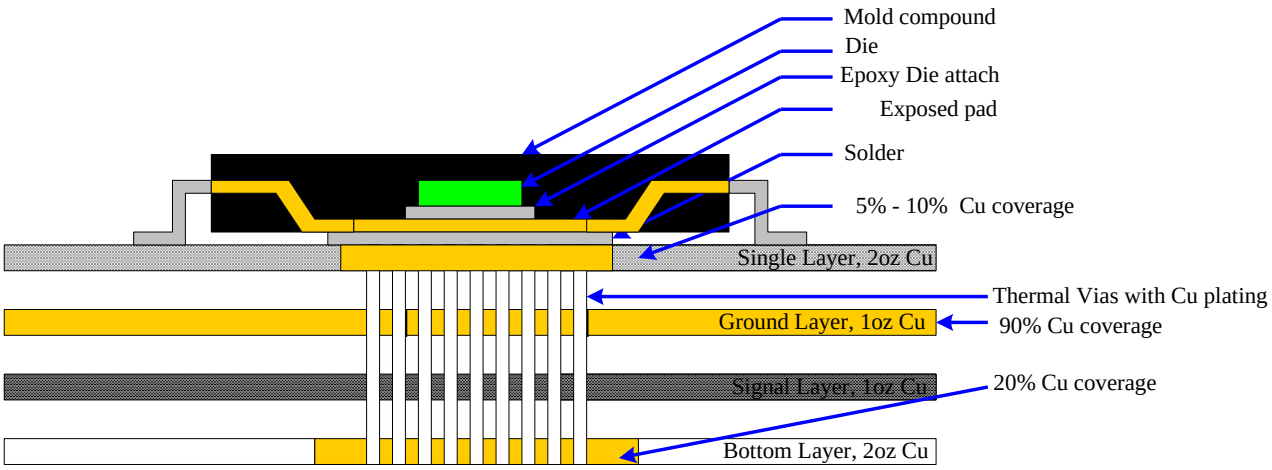
Package and PCB Land Configuration
For a Multi-Layer PCB

JEDEC standard FR4 PCB Cross-section:



Multi-Layer Board (Cross-sectional View)

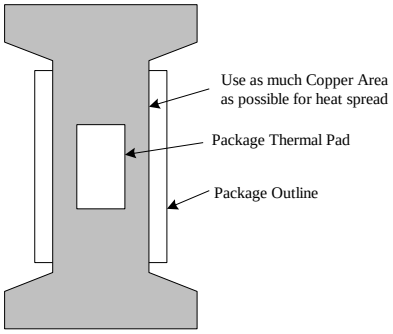
In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, thickness of copper, etc.



Note: NOT to Scale

The above drawing is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators may have to be de-rated for ambient temperatures above 85C. The de-rate value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

APPLICATION USING A SINGLE LAYER PCB



Layout recommendations for a Single Layer PCB: utilize as much Copper Area for Power Management. In a single layer board application the thermal pad is attached to a heat spreader (copper areas) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above it is advisable to use as much copper traces as possible to dissipate the heat.

IMPORTANT:

If the attachment method is NOT implemented correctly, the functionality of the product is not guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

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