FEATURES

- 2.5/1.25Gbps downstream with auto-detection, 1.25Gbps upstream
- Ultra low jitter Integrated EPON SerDes (2.5/1.25Gbps)
- IEEE 802.3ah EPON MAC
- Triple Churning Key decryption
- China EPON standard OAM control
- 802.3ah OAM control
- Independent 10/100 and 10/100/1000 Subscriber Ports
- 802.3 10/100 MAC and 10/100/1000 MAC
- MAC Address Learning for up to 64 MAC Addresses per Ethernet port for 802.1D Bridging
- Highly flexible 802.1Q VLAN support
- 802.1p/q support
- 40 fully-configurable queues
- 1.5 MB of integrated packet buffering

- Line-rate layer 2/3/4 packet classification and filtering for up to 256 entries
- Per-port 802.3x flow control
- 802.3ah Forward Error Correction (FEC)
- Up to eight Logical Link IDs (LLID)
- Internal Management Information Base (MIB) counters for network statistics
- Remote Monitoring (RMON) statistics
- Embedded 80C51 processor with integrated memory
- IEEE 1149.1 JTAG Boundary Scan
- Low Power 3.3V I/O and 1.2V Core supply
- 128-pin LQFP with exposed pad, and TFBGA-169 packages
- Pin compatibility with TK3713 and TK3714
- Industrial temperature operation, -40°C to +85°C

DESCRIPTION

The TK3715 chip for Optical Network Units (ONU) is an IEEE 802.3ah-compliant System-on-Chip (SoC) Ethernet Passive Optical Network (EPON) Bridge. The TK3715 supports all the functions needed to comply with the China standard for EPON. It provides high-speed, fiber optic broadband access for residential and business CPE (Customer Premises Equipment) ONUs. The auto-sensing Turbo-EPON™ mode operates at 1.25GHz downstream with legacy systems and 2.5GHz downstream with Turbo-EPON OLTs, such as the TK3723. The TK3715 is compatible with all Teknovus OLT chipsets. The TK3715 is cost-optimized for markets using the China standard for EPON. The high level of integration in the TK3715 greatly simplifies ONU design. The TK3715 contains an 802.3ah EPON MAC, a SerDes, line-rate L2/L3/L4 classification and filtering, China EPON decryption, Forward Error Correction (FEC), integrated packet buffering, two independent subscriber ports and an embedded processor. The processor supports a sophisticated ONU management system, including alarms, provisioning, DHCP and IGMP functions for a stand-alone IPTV solution at the ONU. Glueless interfaces are provided for an external EPON transceiver, FLASH and 10/100/1000 PHYs.

The TK3715 can be managed from the OLT over the EPON using 802.3ah standard OAM messaging and China OAM extensions.

Combined with the hardware-based DBA of the Teknovus OLT chipset and the Teknovus Host Interface Software, the TK3715 is ideal for ONUs designed for IPTV. This complete EPON system solution provides all the necessary low-level management software, allowing developers to get new products to market quickly.

The TK3715 is offered in low-cost 128-pin Low-profile Quad Flat Pack (LQFP) and 169-ball Thin and Fine Pitch Ball Grid Array (TFBGA) packages. The TFBGA package with its 11x11mm body size is ideally suited for SFP applications.
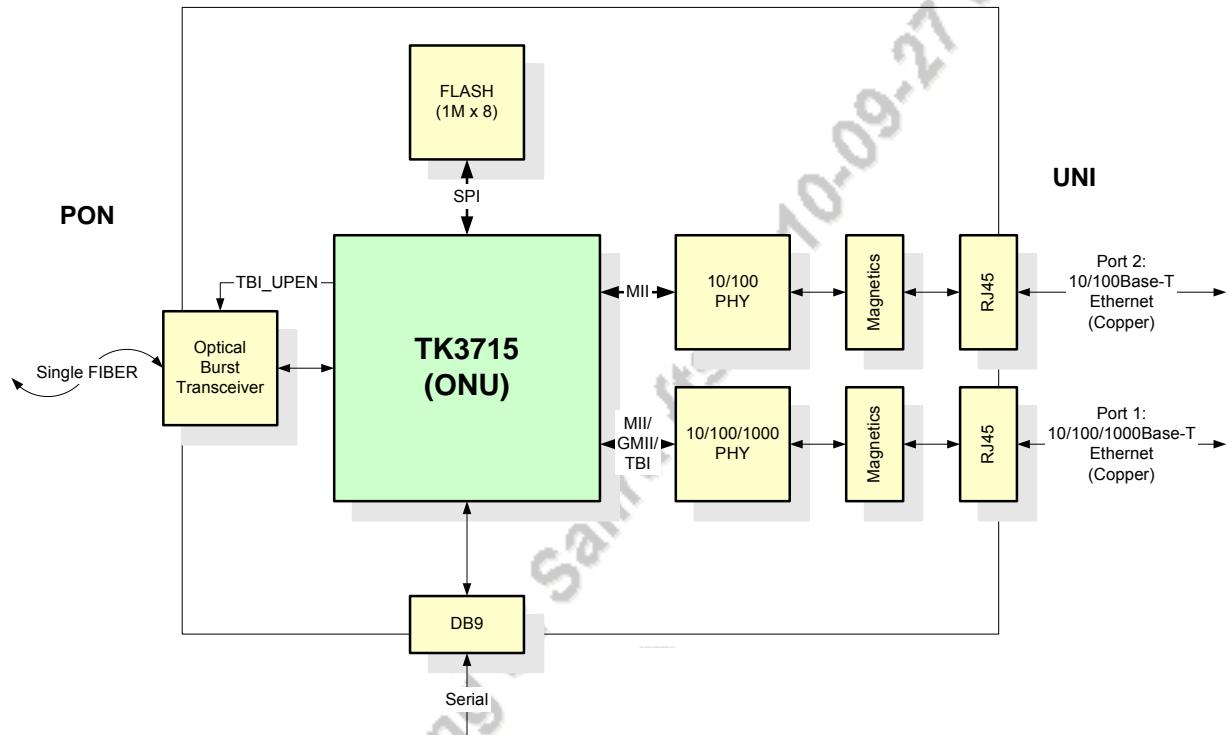
Figure 1.   Block Diagram of TK3715-Based ONU

Revision History

This section records the change history of this Data Sheet.

Table 1.   Revision History

Date	Version	Revision Description
April 23, 2008	1.00	- Initial Formal Release

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1   TK3715 Pin Information

Figure 2.   TK3715 Pin Diagram in 128-LQFP Package

TK3715
TFBGA-169

(Bottom View)
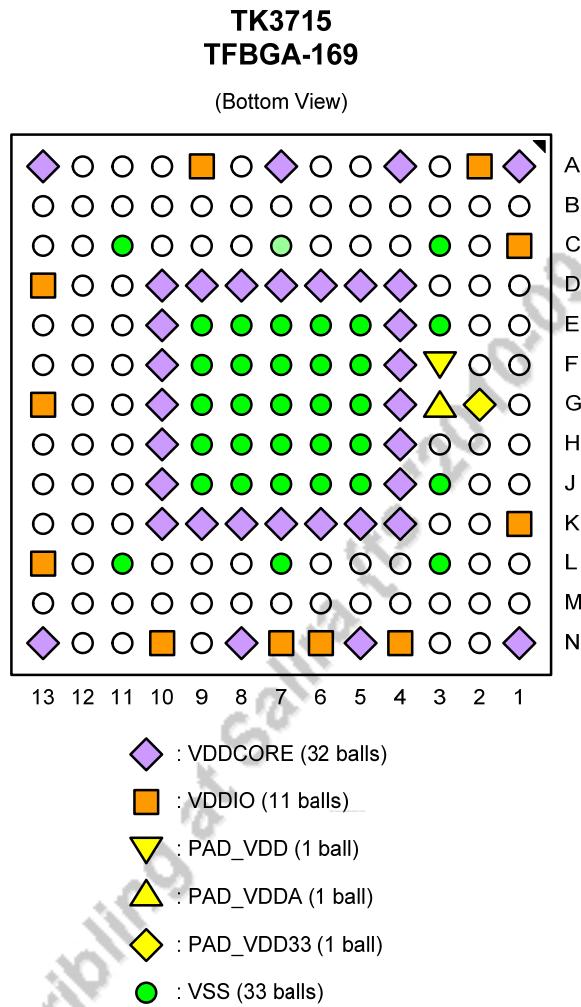
Figure 3.   TK3715 Ball Array in TFBGA-169 Package

1.1　TK3715 Pin Descriptions

Legend:

I = Input	I/O = Input/Output	O/Z = Output which can be placed in high-impedance state
P = Power	NC = No Connect	

All signal levels are CMOS except as noted. All CMOS pins contain internal pull-up resistors. Internal pull-up resistors value range between 40K-100Kohms.

Table 2.　Local-Side 10/100/1000 MII/GMII/TBI Interface (Port 1)

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
9	K12	GMII_RXCLK/ TBI_RBC0	I*	This is a triple function pin: • MII: 25.0/2.5MHz Receive Clock. Generated by PHY to clock-in GMII_RXD[3:0], GMII_RXER, and GMII_RXDV • GMII: 125MHz Receive Clock. Generated by PHY to clock-in GMII_RXD[7:0], GMII_RXER, and GMII_RXDV • TBI: 62.5MHz Receive RBC0 Clock. Generated by SerDes to clock-in TBI_RXD[9:0] (odd code)
122	L9	GMII_TXCLK/ TBI_RBC1	I*	This is a dual function pin: • MII: 25.0/2.5MHz Transmit Clock. Generated by PHY to clock-out GMII_TXD[3:0], GMII_TXER, and GMII_TXEN • TBI: 62.5MHz Receive RBC1 Clock. Generated by SerDes to clock-in TBI_RXD[9:0] (even code) • GMII: unused; pull down with 1K- 4.7Kohm resistor
124	L10	GMII_RXD0/ TBI_RXD0	I	MII/GMII/TBI: Receive Data [0] from PHY/SerDes
125	M10	GMII_RXD1/ TBI_RXD1	I	MII/GMII/TBI: Receive Data [1] from PHY/SerDes
127	N11	GMII_RXD2/ TBI_RXD2	I	MII/GMII/TBI: Receive Data [2] from PHY/SerDes
128	M11	GMII_RXD3/ TBI_RXD3	I	MII/GMII/TBI: Receive Data [3] from PHY/SerDes
2	N12	GMII_RXD4/ TBI_RXD4	I	This is a dual function pin: • GMII/TBI: Receive Data [4] from PHY/SerDes • MII: unused; leave unconnected (NC)
3	M12	GMII_RXD5/ TBI_RXD5	I	This is a dual function pin: • GMII/TBI: Receive Data [5] from PHY/SerDes • MII: unused; leave unconnected (NC)
4	K11	GMII_RXD6/ TBI_RXD6	I	This is a dual function pin: • GMII/TBI: Receive Data [6] from PHY/SerDes • MII: unused; leave unconnected (NC)

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LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
5	M13	GMII_RXD7/ TBI_RXD7	I	This is a dual function pin: • GMII/TBI: Receive Data [7] from PHY/SerDes • MII: unused; leave unconnected (NC)
7	L12	GMII_RXDV/ TBI_RXD8	I	This is a dual function pin: • MII/GMII: Receive Data Valid from PHY • TBI: Receive Data [8] from SerDes
8	J11	GMII_RXER/ TBI_RXD9	I	This is a dual function pin: • MII/GMII: Receive Data Error from PHY • TBI: Receive Data [9] from SerDes
121	N9	GMII_CRS/ TBI_COMMA	I	This is a triple function pin: • MII: Carrier Sense. Indicates when the line is busy • TBI: COMMA. Indicates valid Comma detected. If not available then pull up this input with 10Kohm resistor • All Other Modes: unused; leave unconnected (NC) (GMII is full-duplex only)
120	M9	GMII_COL	I	This is a dual function pin: • MII: Collision. In half-duplex mode, indicates a collision • All Other Modes: unused; leave unconnected (NC) (GMII is full-duplex only)
117	M8	GMII_GTXCLK/ TBI_TXCLK	O	This is a triple function pin: • GMII: 125MHz Transmit Clock. Used by Gigabit PHY for clocking-in GMII_TXD[7:0], GMII_TXER, and GMII_TXEN • TBI: 125MHz Transmit/Reference Clock. Used by SerDes for clocking-in TBI_TXD[9:0] • MII: unused; leave unconnected (NC)
115	L8	GMII_TXD0/ TBI_TXD0	O	MII/GMII/TBI: Transmit Data [0] to PHY/SerDes
114	M7	GMII_TXD1/ TBI_TXD1	O	MII/GMII/TBI: Transmit Data [1] to PHY/SerDes
112	M6	GMII_TXD2/ TBI_TXD2	O	MII/GMII/TBI: Transmit Data [2] to PHY/SerDes
111	L6	GMII_TXD3/ TBI_TXD3	O	MII/GMII/TBI: Transmit Data [3] to PHY/SerDes
108	M5	GMII_TXD4/ TBI_TXD4	O	This is a dual function pin: • GMII/TBI: Transmit Data [4] to PHY/SerDes • MII: unused; leave unconnected (NC)
107	L5	GMII_TXD5/ TBI_TXD5	O	This is a dual function pin: • GMII/TBI: Transmit Data [5] to PHY/SerDes • MII: unused; leave unconnected (NC)
105	M4	GMII_TXD6/ TBI_TXD6	O	This is a dual function pin: • GMII/TBI: Transmit Data [6] to PHY/SerDes • MII: unused; leave unconnected (NC)
104	N3	GMII_TXD7/ TBI_TXD7	O	This is a dual function pin: • GMII/TBI: Transmit Data [7] to PHY/SerDes • MII: unused; leave unconnected (NC)

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
101	L4	GMII_TXEN/ TBI_TXD8	O	This is a dual function pin: • MII/GMII: Transmit Data Enable to PHY • TBI: Transmit Data [8] to SerDes
100	N2	GMII_TXER/ TBI_TXD9	O	This is a dual function pin: • MII/GMII: Transmit Data Error to PHY • TBI: Transmit Data [9] to SerDes

* When not used, pull down unused clock inputs with the 1K-4.7Kohm resistors, and leave all other pins unconnected.

Table 3.   Local-Side 10/100 MII Interface (Port 2)

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
28	E12	MII_RXCLK	I*	Receive Clock. Generated by PHY to clock-in MII_RXD[3:0], MII_RXER, and MII_RXDV
30	D11	MII_RXD0	I	Receive data [0] from 10/100 PHY to TK3715
31	D12	MII_RXD1	I	Receive data [1] from 10/100 PHY to TK3715
32	C13	MII_RXD2	I	Receive data [2] from 10/100 PHY to TK3715
33	C12	MII_RXD3	I	Receive data [3] from 10/100 PHY to TK3715
27	E13	MII_RXDV	I	Receive Data Valid. Signals the presence of data on MII_RXD[3:0]
25	E11	MII_RXER	I	Receive Error. Indicates a transmit coding error has occurred
21	G11	MII_CRS	I	Carrier Sense. Indicates when the line is busy
22	F13	MII_COL	I	Collision. In half-duplex mode, indicates a collision
24	F11	MII_TXCLK	I*	Transmit Clock. Generated by PHY to clock-out MII_TXD[3:0], MII_TXER, and MII_TXEN
16	H13	MII_TXD0	O	Transmit data [0] from TK3715 to PHY
17	H11	MII_TXD1	O	Transmit data [1] from TK3715 to PHY
19	G12	MII_TXD2	O	Transmit data [2] from TK3715 to PHY
20	F12	MII_TXD3	O	Transmit data [3] from TK3715 to PHY
14	H12	MII_TXEN	O	Transmit Data Enable. Signals the presence of data on MII_TXD[3:0]
13	J13	MII_TXER	O	Transmit Data Error

* When not used, pull down both clock inputs with the 1K-4.7Kohm resistors, and leave all other pins unconnected (NC).

Table 4.   MDIO Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
10	K13	MDIO_DATA	I/O	Management Data I/O. Serial Access for configuration of external PHY(s)
11	J12	MDIO_CLK	O	Management Data Clock. Clock for R/W of device configuration register

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Turbo-EPON™ SoC Bridge for China Standard ONU

Table 5.   Ethernet PON Transceiver Serial Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
82	F1	PAD_RXP	I*	Positive Receive Serial Data from optical transceiver
83	G1	PAD_RXN	I*	Negative Receive Serial Data from optical transceiver
78	E2	PAD_TXN	O*	Negative Transmit Serial Data to optical transceiver
79	F2	PAD_TXP	O*	Positive Transmit Serial Data to optical transceiver
89	J2	SER_ATB_0	O	SerDes Analog Test Bus. For internal testing only; do not connect (NC) for normal operation
90	H3	SER_ATB_1	O	
85	H2	PAD_REXT	I	External Reference Resistor. Connect through a 5Kohm (+/-1%) resistor to Ground
92	K2	TBI_UPEN	O	Laser Enable to EPON optical transceiver
87	H1	PAD_REF_CLK_P	I**	Positive Upstream Clock reference from external VCO or oscillator (TJ$_{p-p}$ < 40ps)
88	J1	PAD_REF_CLK_N	I**	Negative Upstream Clock reference from external VCO or oscillator (TJ$_{p-p}$ < 40ps)
71	D2	UPS_CLK_OUT	O	Internal clock output. For internal testing only; do not connect (NC) for normal operation
69	C2	TBI_UPD_CLK	O	Alternate GMII/TBI 125MHz Transmit Clock. This pin can be used instead of GMII_GTXCLK/TBI_TXCLK pin

*   This interface is non-standard PECL. Refer to Section 3.3: DC Characteristics.

** This LVPECL interface is internally terminated. AC coupling capacitors are recommended. PAD_REF_CLK_N may be tied off to 1.2V..1.3V reference voltage for single-ended operation. Refer to Section 2.6: Reference Oscillator for more details.

Table 6.   UART Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
48	A8	URT_RXD0	I	UART Serial Input Data Port 0
47	B8	URT_TXD0	O	UART Serial Output Data Port 0
44	A10	URT_RXD1	I	UART Serial Input Data Port 1 (debug mode only); leave unconnected (NC) for normal operation
45	B9	URT_TXD1	O	UART Serial Output Data Port 1 (debug mode only); leave unconnected (NC) for normal operation

Table 7.   Reference Clocks and Global Reset

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
94	K3	CLK_125	I	125.0 MHz Reference Clock (+/-100ppm)
35	B13	CLK_25	O	25.0 MHz Output Reference Clock. This clock may be used to drive the Ethernet PHY(s)

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LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
68	B1	CLK_125_SEL	I	Clock mode configuration. When set high (1), the core clock will operate off of the CLK_125. When set low (0), the core clock will operate off of the PAD_REF_CLK_P/N inputs. Refer to Section 2.6: Reference Oscillator for more details on clocking options.
52	B7	RST_N	I	System Reset (active low)

Table 8.   JTAG Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
95	L1	TDI	I	JTAG Test Data Input Leave unconnected (NC) for normal operation
97	M3	TMS	I	JTAG Test Mode Select Leave unconnected (NC) for normal operation
98	M1	TCK	I	JTAG Clock Leave unconnected (NC) for normal operation
96	L2	TRSTN	I	JTAG Test Reset (active low) Pull down with 1K-4.7Kohm to disable JTAG functionality
99	M2	TDO	O	JTAG Test Data Output

Table 9.   GPIO Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
65	C4	GPIO0	I/O	General Purpose I/O [0] (default input)
63	A3	GPIO1	I/O	General Purpose I/O [1] (default input)
62	B4	GPIO2	I/O	General Purpose I/O [2] (default input)
61	C5	GPIO3	I/O	General Purpose I/O [3] (default input)
58	B5	GPIO4	I/O	General Purpose I/O [4] (default input)
57	A5	GPIO5	I/O	General Purpose I/O [5] (default input)
55	B6	GPIO6	I/O	General Purpose I/O [6] (default input)
54	A6	GPIO7	I/O	General Purpose I/O [7] (default input)
37	A12	GPIO8	I/O	General Purpose I/O [8] (default input)
36	B12	GPIO9	I/O	General Purpose I/O [9] (default input)
74	D1	GPIO10	I/O	General Purpose I/O [10] (default input)
73	D3	GPIO11	I/O	General Purpose I/O [11] (default input)
66	B2	GPO_SO	O	General Purpose Shift Data Output
67	B3	GPO_CLK	O	General Purpose Shift Clock

Table 10.   Processor Bus Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
49	C8	INT_N	I	Processor Interrupt (active low)
53	C6	PF_INT_N	I	When TRSTN pin is low (0), this is Power Failure Interrupt input to 80C51 Processor (active low)
39	C10	SPI_DIN	I	Serial FLASH Memory Data to the TK3715
40	A11	SPI_DOUT	O	Serial FLASH Memory Data from the TK3715
42	C9	SPI_CS_N	O	Serial FLASH Memory Chip Select (active low)
38	B11	SPI_SCLK	O	Serial FLASH Memory Clock (default 15.625MHz)

Table 11.   Test and Configuration Interface

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
76	E1	SM_N	I	IC Scan Test Mode Enable (active low). Pull up for normal operation
41	B10	TEST_MODE_N	I	Test Mode Enable (active low). Pull up for normal operation

Table 12.   Digital Power and Ground

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
6, 18, 29, 46, 64, 70, 93, 106, 113, 116, 123	A2, A9, C1, D13, G13, K1, L13, N4, N6, N7, N10	VDDIO	P	3.3 V I/O Supply Voltage
1, 12, 15, 23, 26, 34, 43, 50, 51, 56, 59, 60, 72, 77, 91, 102, 103, 109, 110, 118, 119, 126	A1, A4, A7, A13, D4, D5, D6, D7, D8, D9, D10, E4, E10, F4, F10, G4, G10, H4, H10, J4, J10, K4, K5, K6, K7, K8, K9, K10, N1, N5, N8, N13	VDDCORE	P	1.2 V Core Supply Voltage
129 (Exposed Pad*)	C3, C7, C11, E3, E5, E6, E7, E8, E9, F5, F6, F7, F8, F9, G5, G6, G7, G8, G9, H5, H6, H7, H8, H9, J3, J5, J6, J7, J8, J9, L3, L7, L11	VSS	P	Ground Supply (also thermal pad in LQFP package)
75	-	GND	P	Ground (Test Mode)

* This is the main VSS ground connection in LQFP-128 package. Ensure sufficient current return path and thermal connectivity for the entire IC. Refer to Section 4.1.1: LQFP-128 Exposed Pad PCB Design Guidelines for more details.

Table 13.   Internal SerDes Power

LQFP Pin	TFBGA Ball	Signal Name	I/O	Signal Description
80, 81	F3	PAD_VDD	P*	SerDes VDD 1.2V supply
86	G3	PAD_VDDA	P*	SerDes Analog VDD 1.2V supply
84	G2	PAD_VDD33	P*	SerDes VDD 3.3V supply

* Each pin should be filtered individually. Refer to Section 2.13.2: I/O Power Supply. "Ripple" noise amplitude must be limited to less than 50mV (peak-to-peak for 50KHz..100MHz frequencies).

2 TK3715 Functional Description

The TK3715 is an IEEE 802.3ah standard Ethernet PON (EPON) to 10/100 and 10/100/1000 Ethernet bridge for Optical Network Unit (ONU) applications. The TK3715 incorporates an EPON MAC, an 802.1D bridge, a switching element, and a 10/100 Ethernet MAC and a 10/100/1000 Ethernet MAC for subscriber access. An integrated processor in the TK3715 provides an embedded management system, including configuration, self management, and auto discovery. Together, the TK3715 ONU chip, the Teknovus OLT chips, and the Teknovus Host Interface Software provide a complete EPON solution.

The two Media Access Controllers (one 10/100 Ethernet MAC and one 10/100/1000 Ethernet MAC) support half-duplex and full-duplex operation for end user traffic. Three Ethernet Lookup Engines (LUEs) enable traffic prioritization, local address filtering, and statistics gathering. Twenty internal FIFOs provide buffering for upstream and downstream traffic and OAM traffic. The 80C51 processor provides management control. It responds to in-band OAM commands and Host Interface messages for configuration and statistics gathering. Refer to Figure 4.
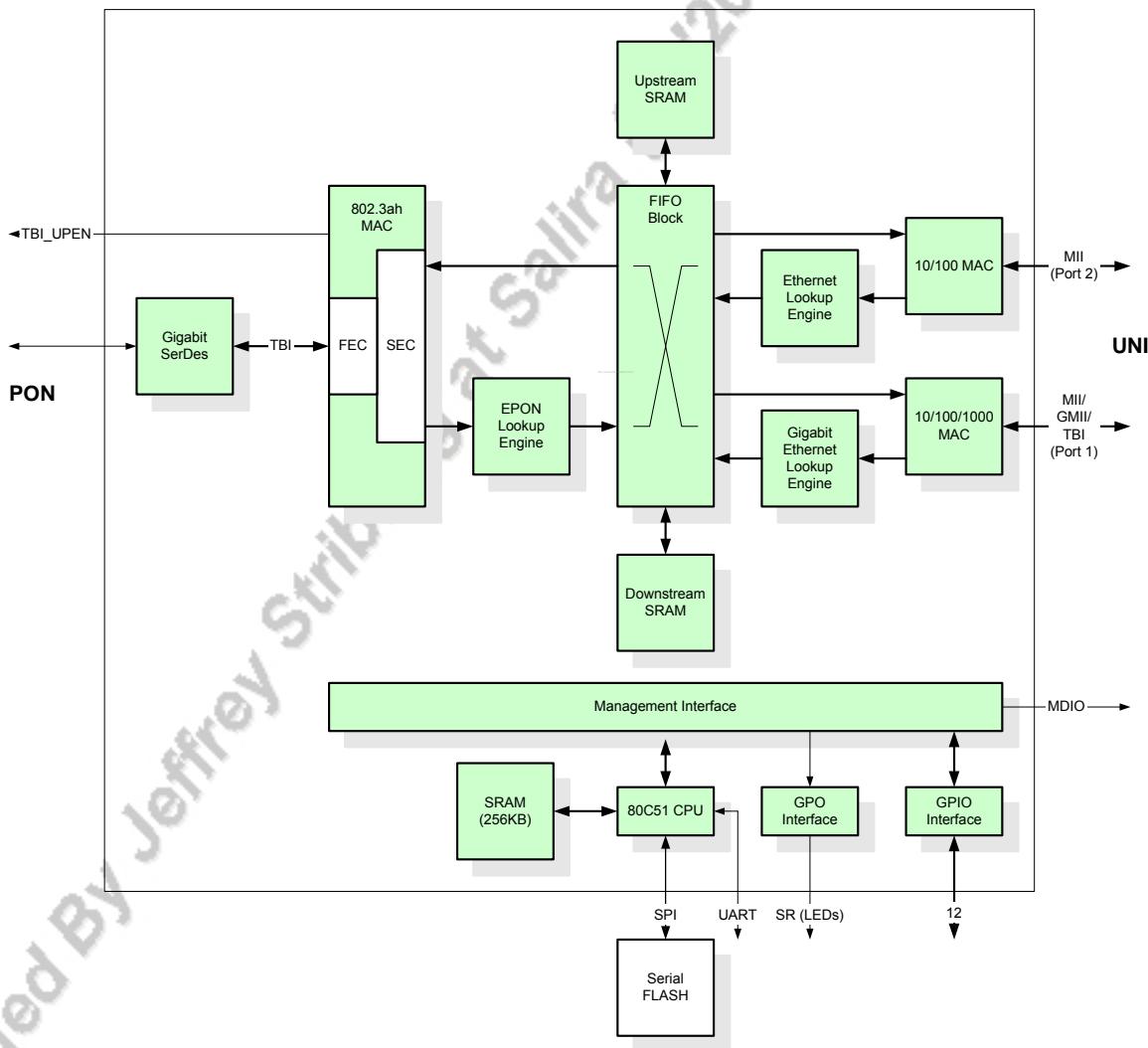
Figure 4.   TK3715 Block Diagram

2.1   10/100 Ethernet MAC and 10/100/1000 Ethernet MAC

The TK3715 contains two IEEE 802.3-compliant Ethernet MACs: one 10/100 MAC and one 10/100/1000 Gigabit MAC. Both half-duplex and full-duplex modes of operation are supported for the 10/100 MAC. Full-duplex operation is supported for the 10/100/1000 MAC. RMON statistics are gathered for both interfaces.

The 10/100 Ethernet MAC interfaces to an external PHY via a standard MII interface. Refer to Figure 5. The 10/100/1000 Ethernet MAC connects to an external PHY via an MII/GMII interface, or to an external gigabit SerDes via a TBI interface.

Both MACs discard frames based on invalid CRC-32 checksums. If they are configured for 802.3x flow control operation, the MACs filter incoming 802.3x MAC Control frames.

A standard MDIO interface is provided to control external PHYs and/or Ethernet Switches.
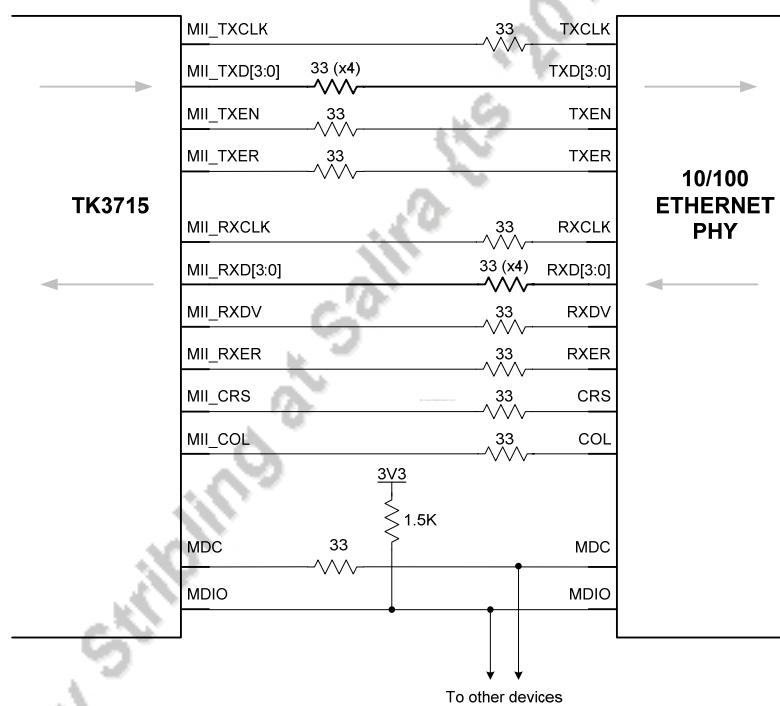
Figure 5.   MII Interface with 10/100 Ethernet PHY

2.2   Classification and Filtering

There are three types of Ethernet Lookup Engines (LUEs). Each LUE corresponds to one of the interface ports:

- The Gigabit Lookup Engine (GLU), for incoming Ethernet data from Port 1 (10/100/1000 interface).
- The Ethernet Lookup Engine (ELU), for incoming Ethernet data from Port 2 (10/100 interface).
- The Downstream Lookup Engine (DLU), for incoming Ethernet data from the EPON MAC Port.

The LUEs are configurable via the Host Interface. Refer to the ONU Host Interface Specification for programming details.

The LUEs provide source address learning, local address filtering, and static rule filtering on the incoming Ethernet data. Each Ethernet port contains a single lookup table SRAM of 256 entries. This table stores both the dynamic (learned) and static filtering entries. Each Ethernet port supports up to 64 learned addresses. The remaining table locations are used for static entries. If auto learning is not enabled, all entries are available for static entries.

The LUEs provide line rate classification and filtering for Layer 2, Layer 3, and Layer 4 packets. The supported fields include the following:

- MAC SA/DA
- VID
- VLAN CoS
- IPv4/IPv6 SA/DA
- IPv4/IPv6 priority field
- TCP/UDP source/destination port

New fields can be defined by the operator. The classification rules can also be re-configured by the operator.

Each destination FIFO is mapped to a strict priority scheduler, as follows:

- In the upstream direction, the ONU supports one strict priority scheduler per logical link.
- In the downstream direction, the ONU supports one strict priority scheduler per Ethernet port.

Up to 8 rules can be combined to support complex classification operations, using a boolean AND condition. For example:

> If ((IPv4SA >= 192.168.200.1) and (IPv4SA <= 192.168.200.20) and
> (ToS == 3))
>
> Send traffic to FIFO 4

Priority values can be assigned to the rules to prevent conflicts. The numerically lower value receives the higher priority. If one rule has a priority value of 0 and a conflicting rule has a priority value of 14, the 0-value rule will be implemented, and the 14-value rule will be ignored. For example:

> Rule x, Priority=14: If (IPv4SA == 192.168.1.100)
>
> Send traffic to FIFO 3
>
>
> Rule y, Priority=0: If (VID exists in frame)
>
> Drop

In this example, a frame with VID will be dropped, even if the frame's IPv4 SA is set to 192.168.1.100.

The LUEs provide the connection from the Ethernet ports to the FIFO queues. The two upstream LUEs may not share a destination queue. The destination queue ultimately maps to the LLID and quality of service for a flow. It can be selected by a static rule checking the Ethernet destination address and source address, the VLAN tag ID, the VLAN tag service, or the differentiated services field.

2.2.1   MAC Address Learning and Filtering

The TK3715 supports MAC Source Address (SA) learning in the upstream direction. MAC address learning prevents unnecessary traffic from being sent to the OLT. The TK3715 does not analyze MAC addresses in the downstream direction unless a specific classification or filter rule has been provisioned.

MAC SA learning is performed by the two upstream LUEs. The LUEs build and maintain a table of MAC address entries gathered from the SAs of incoming frames.

The TK3715 supports two learning modes:

- **802.1d Learning**. When a frame is received with a Destination Address (DA) that matches an SA entry in the table, the frame is discarded.
- **MAC Access Control**. When a frame is received with a Destination Address (DA) that does not match an SA entry in the table, the frame is discarded until the DA is learned.

Only one learning mode can be selected at a time. The learning modes are selected using OLT Host Interface Software.

Both learning modes support two configurable features for learning new MAC addresses: **Age Limit** and **Entry Limit**.

Age Limit

The Age Limit can be configured to delete MAC table entries that are not re-learned in a user-defined time period. Values entered in the Age Limit field are automatically rounded down to the nearest power of 2. For example, if the user enters a value between 64 and 127, the value will be rounded down to 64 (which is 2^6). If the user enters a value between 128 and 255, the value will be rounded down to 128 (2^7). The maximum Age Limit is $2^N * 8.75$ ms for N = 0 to 15.

The Age Limit is provisioned in units of 8.75 ms. The minimum time that an entry will remain in the table is 7/8 of the provisioned time. The maximum time that an entry will remain in the table is the provisioned time.

If the Age Limit is set to 0, aging is not performed. In this case, entries can be manually cleared or overwritten. They are also removed by the Entry Limit feature, if it is enabled.

Entry Limit

The MAC table can be configured to limit the number of entries. For the 802.1d Learning mode, the per-port limit can be set to any value from 0 to 64. For the MAC Access Control mode, the per-port limit can be set to any value from 0 to 32.

When the MAC table reaches the configured limit, existing entries are over-written by new entries. Existing entries are over-written according to how the Age Limit feature is configured, as follows:

- **Age Limit is Off** (set to 0). The entry at the bottom of the list is overwritten, according to highest order location. This entry might not have the oldest timestamp.
- **Age Limit is On** (set to a non-0 value). The entry with the oldest timestamp is overwritten. If two or more entries share the oldest timestamp, one of these entries will be overwritten.

If the Entry Limit is set to 0, entry limiting is not performed. In this case, all frames are sent to the OLT, regardless of DA.

Note: Additional ONU filter rules, if any, will filter corresponding frames when the Entry Limit feature is disabled.

2.2.2 Packet Modification

The LUEs provide support for adding and deleting VLAN tags from a frame. The table results can set or clear an "Add VLAN tag" bit with a rule level associated to this function. The VID and COS fields in the VLAN tag can be set as a result in a rule. If two rules set the VID/COS at the same rule priority, the results will be bit wise OR'ed together. The "Delete VLAN tag" bit allows for the removal of the VLAN tag from the frame. A VLAN tag must be present in the frame for the "Delete VLAN tag" bit to modify the frame. If a frame has both the Add and Delete tag set, the old tag will be removed and a new tag will be inserted.

2.2.3 Static Entry Filtering

The lookup table can be configured with very simple or very complex rules to discard or classify traffic. These rules allow for selection of Layer 2 protocol, Layer 2 LLC, VLAN, IPv4/v6 header, or UDP/TCP header fields. Typical fields include the VLAN Tag ID, Layer 2 Ethertype, and the TOS Precedence value.

2.2.4 Match Fields

Static entries specify a comparison of a field from the frame with a value in the rule. The match select for the rule may require that the two values are equal, less than, greater than, or not equal. The existence of a field can also be used as a test condition. For example, the user may want to discard all frames without a VLAN tag. In this case, the VLAN tag is specified as a field, and match select of the rule is "not present". When a comparison is specified on a field that is not present in the frame, the comparison will not match.

In addition, two bit-test match types are defined: "MATCH BIT" and "MATCH NOT BIT". These match types are used to test if a single bit within a frame is set or not set. The user sets a single bit in the lookup value. The field selected in the rule is then checked against this bit. For the "MATCH BIT" match type, if the bit set in the lookup value is set in the field, it is considered a match. For the "MATCH NOT BIT" match type, if the bit set in the lookup value is not set in the field, it is considered a match. One application for this match type is to test if the multicast bit is set in an L2 destination address.

2.2.5 IPv6 Extension Header Parsing

In the case of IPv6 Extension Headers, Field 11 is fixed to parse the final Next Header value. The following Next Header values are interpreted as Extension Headers:

Table 14. IPv6 Next Header

Number in previous "Next Header" field	Header Contents
0	Hop-by-Hop Options
60	Destination Options
43	Routing
44	Fragment
51	Authentication

Any other "Next Header" value is interpreted as the final header (L3 Protocol Type). Its value will be parsed into Field 11.

2.2.6 Rule Levels

The LUEs provide 16 levels of rule priority for the two output results. A single packet may match more than one static rule. When this occurs, the rule priority is used to determine the result. Lower rule priority numbers take precedence over higher numbers. For example, a static entry may have a level 4 rule that forwards all IP packets, and a level 3 rule that discards packets for IP destination 192.168.1.x. In this case, an IP packet with a matching address will be discarded.

Dynamic entries have a default rule value of 2. Dynamic discards can be overridden by programming a static rule with a higher priority.

Some static filtering rules require multiple fields to be matched. For example, a system may be configured as follows: only TCP/IP packets on port 30, sent to a certain destination IP address range, can be forwarded. This type of rule can be accomplished by chaining 3 rules together. The first rule can match the TCP port number on the layer 2 header, while the second and third rules can match the address and port number. The rules in a rule chain must be written to consecutive locations in the lookup table. If all rules in a chain match, the result specified by the final rule in the chain will be executed.

Note: The number of chained entries can not exceed 8.

2.3 Packet Buffer Configuration

The FIFO block provides buffering for upstream and downstream traffic. The FIFO block manages the 20 upstream queues and 20 downstream queues. The 20 upstream queues can be configured to send data to the processor or to any LLID. The 20 downstream queues can be configured to send data to the processor or to one of the two Ethernet ports. The queues are allocated space from a pool of six 256KB blocks of internal SRAM. Between one and four of the blocks can be assigned to the downstream queues. The remaining blocks are used for upstream queues.

2.3.1 Connecting Queues

Once the 40 logical queues are defined, they must be connected to an input and output port. A queue can not be connected to multiple input sources. Packets can be duplicated to two queues in both the upstream and downstream directions.

The upstream queue input sources are the two upstream LUE blocks and a transmit buffer from the processor. The result of the LUE processing is the destination queue number. The LUE blocks may feed multiple queues, but the configuration must guarantee that the LUEs don't use the same queue. If a queue is used for upstream packet transmission from the processor buffer, it can not be used by the LUE blocks.

The upstream queue output destinations are the EPON MAC and a receive buffer to the processor. Within the EPON MAC, the eight Logical Link Identifiers (LLIDs) are possible destinations. The EPON MAC configuration allows for an LLID to have multiple queues as sources.

The downstream queue input sources are the EPON MAC and a transmit buffer from the processor. The Downstream Lookup Engine (DLU) determines the mapping from input frame type to downstream queue number. The EPON MAC can not share a queue destination with the processor buffer.

The downstream queue output destinations are the two Ethernet MACs and a receive buffer to the processor. Each queue is configured in the FIFO block to select a destination. Multiple queues can share a single

destination. For example, all 20 downstream queues may be configured to a single Ethernet port. When multiple queues are configured for the same destination, they are serviced in strict priority. The lowest numbered queue has the highest priority. A single queue can output to either the processor or to one or both Ethernet ports. When a queue is configured for both Ethernet ports, packets are duplicated to both interfaces. Refer to Figure 6.
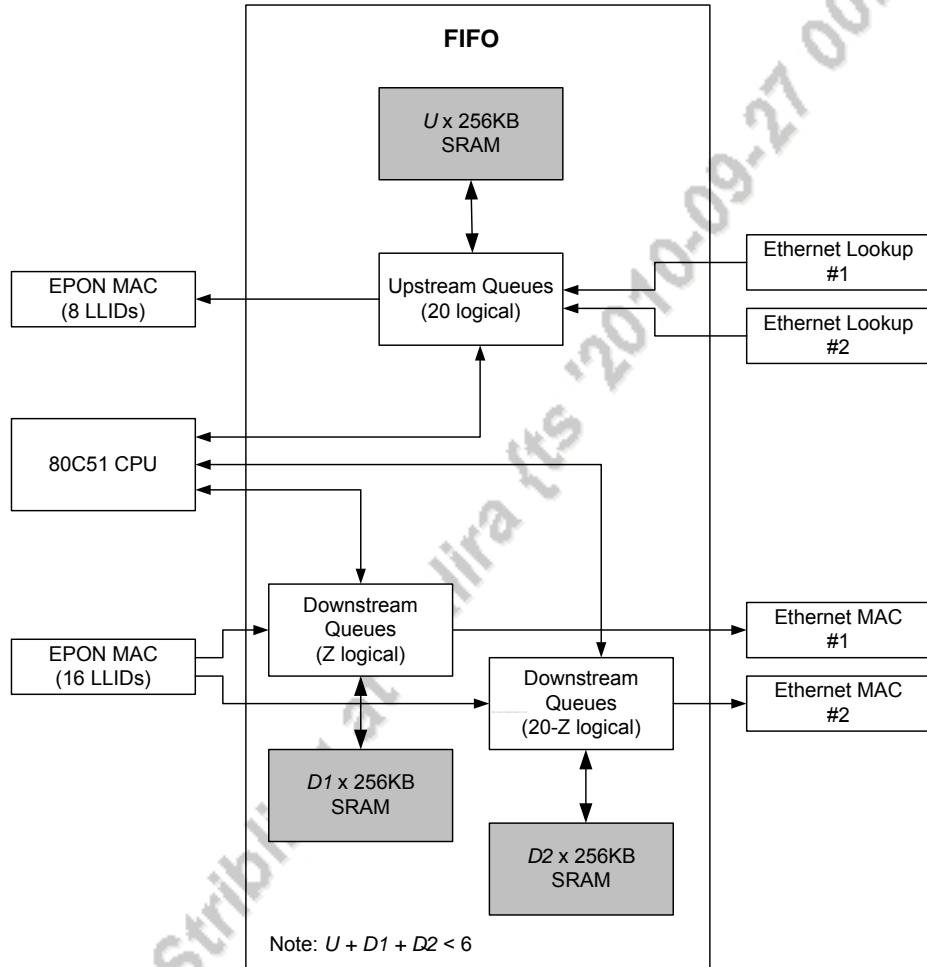
Figure 6.   FIFO Interconnection Structure

2.4   Ethernet PON MAC

The EPON MAC is responsible for filling grants and generating report messages. It is configured via the Host Interface Software or the personality section of FLASH memory.

LLID Index 0 supports reporting as defined in the China standard for EPON. The EPON MAC monitors the 20 upstream FIFO queues, in order to create report messages. It maps the 20 upstream FIFO queues into priority groups. Up to eight priority groups can be configured. Based on these groups, the MAC generates "Queue Report" values in the report messages.

Report messages contain two queue sets. The second queue set reports the entire depth of the upstream queues. The first queue set reports queue depth up to a programmable threshold.

The EPON MAC contains a frame length FIFO. The frame length FIFO tracks the frame length and FIFO queue number for frames to be transmitted upstream. The frame length FIFO has two purposes. First, it accumulates

frame length information for all queues mapped to the LLID Index. (Frame length information is accumulated up to the programmable threshold.) Second, it enforces priority order when frames are taken from the FIFO queues and transmitted upstream. Frame lengths are pushed into the frame length FIFO in strict queue priority order. Queue 0 is the highest priority. The sum of the frame lengths is accumulated. Frame lengths are added to the frame length FIFO until adding one more would exceed the threshold. When a grant is filled, entries are removed from the frame length FIFO. These entries determine the transmission order. As frames are sent upstream, the frame length FIFO is replenished in parallel.

At the end of a grant, a report frame is sent if requested by the OLT.

The EPON MAC is also responsible for inserting time stamps into the EPON management frames generated by the host processor.

The EPON MAC provides decryption for downstream traffic. The MAC uses China standard decryption (triple churning). Decryption is performed on a per LLID basis. Firmware manages the key exchange.

The EPON MAC generates an 8-byte frame preamble that includes the LLID of the link and security key selection. The preamble is covered by a CRC8 as defined in IEEE 802.3ah. The inter-packet gap is 96nS for 1Gbps EPON and 64nS for 2Gbps EPON.

The TK3715 supports 802.3ah Forward Error Correction (FEC). Frames are delineated by detecting the S_FEC and T_FEC characters. A hamming code is used to detect the first match with N number of bits of the expected delineator.
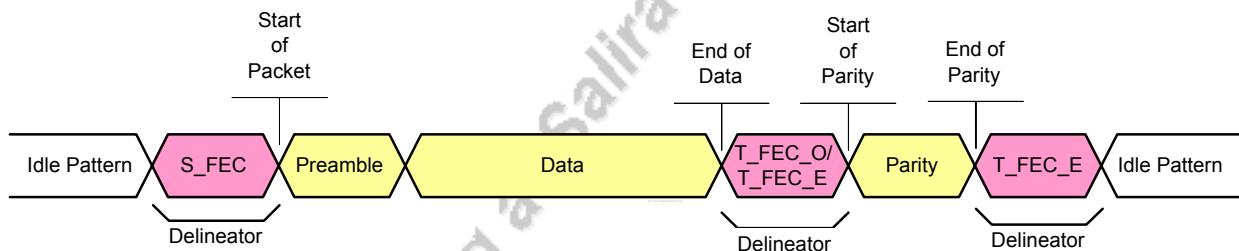
Figure 7.   FEC Packet Delineation

The FEC then uses the Reed Solomon (255, 239) code to correct up to 8 bit errors per block of data.

The receiver can receive both FEC and non-FEC encoded frames. The transmitter may be set to transmit FEC or non-FEC encoded frames.

Note: The performance of the FEC may vary based on the choice of optics and error distribution into the SerDes. FEC adds between 15us and 25us of additional latency to the data path.

2.5   EPON Transceiver Interface

The TK3715 contains an ultra-low jitter, integrated 2.5Gbps/1.25Gbps SerDes. The SerDes provides a direct connection to an EPON optical transceiver. The SerDes has the following features:

- Clock and Data Recovery (CDR) and de-serialization on downstream
- Serialization on upstream
- 8B/10B encoding and decoding
- 50Ω impedance support
- Various loop-back functions
- Auto self-test
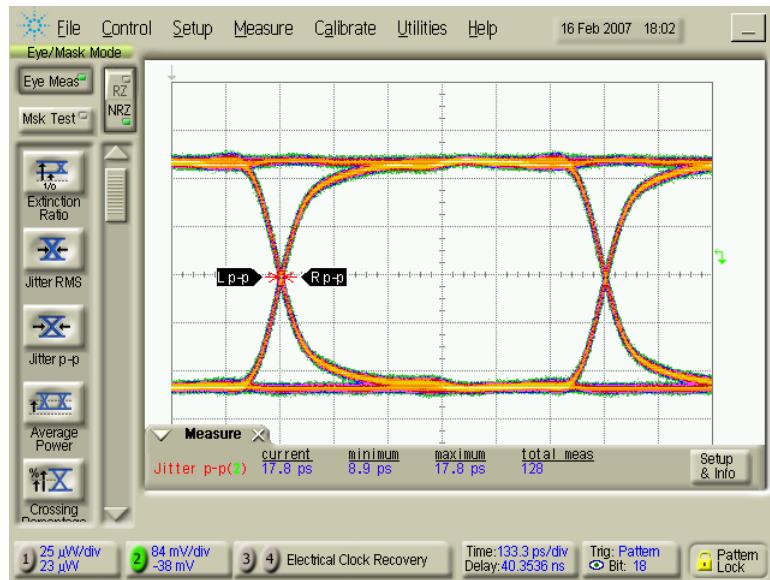
Figure 8.   SerDes Typical Unfiltered Electrical Eye Diagram

The integrated SerDes can be connected directly to the EPON transceivers using the recommended circuit in Figure 9.

Traces from the TK3715 to the transceiver must have controlled impedance. Traces must be routed as differential pairs with no stubs and a minimum number of vias. Termination networks should be located as close to the input pins as possible. All resistors should be 1%.
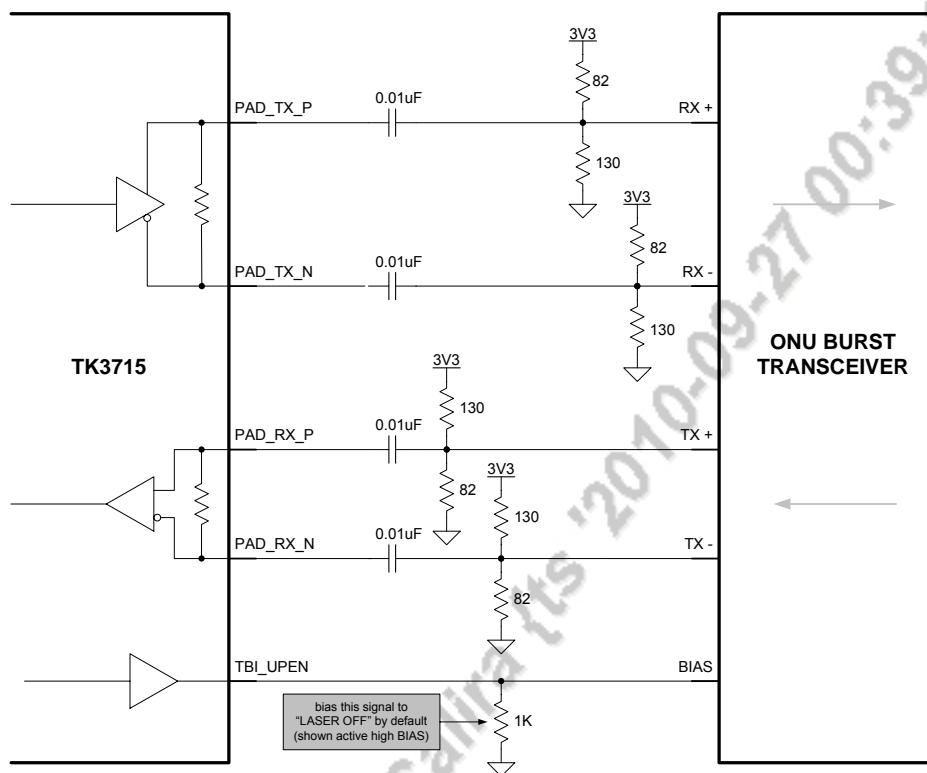
Figure 9.   Internal SerDes Connection to EPON Transceiver

The TBI_UPEN signal enables the PON transceiver for upstream transmission. Polarity and timing of this signal are programmable. Refer to the ONU Host Interface Specification for details on programming this signal.

Note: Teknovus recommends that the default state of this signal be controlled during power-up and reset. This is done by forcing the optical transceiver into the OFF state (no light being transmitted in the upstream direction). This will prevent unsolicited bursts of light on the EPON network.

Some optical transceivers have optional connections for presence detect, signal detect, receive signal strength, I^2C control, etc. These signals may be routed to the GPIO pins, if desired. Refer to the ONU Host Interface Specification for details on how to connect and control these pins.

2.6   Reference Oscillator

The TK3715 requires at least one 125.00MHz reference clock source. In the case of a single oscillator solution, there are two options: the LVPECL differential oscillator (Figure 10) and the single-ended oscillator (Figure 11).

PAD_REF_CLK_P/N inputs require either differential LVPECL (Figure 10) or a single-ended LVTTL source (Figure 11). The optional CLK_125 input accepts LVTTL-type signals only.

Both clock solutions require a high quality 125.00MHz (+/-100ppm or better) low jitter (TJ < 40ps random + deterministic) oscillator. Differential oscillators provide the best performance due to their enhanced jitter performance.

Recommended parts for a single-ended solution include:

- Ecliptek EC2600ETTS-125.000M or EH2600ETTS-125.000M
- ECS ECS-3953M-1250-BN

- MF Electronics T3392-125M

Optionally, single-ended oscillator signals can be "translated" with an LVTTL-to-LVPECL converter IC, and connected to TK3715 PAD_REF_CLK_P/N inputs.

Jitter performance of the built-in SerDes depends heavily on the quality of the reference clock. Therefore, it is important to select a high quality oscillator with good jitter characteristics. Single-ended oscillators provide an economical solution. Refer to Figure 11.

Note: Teknovus requires that Programmable Crystal Oscillators are **not** used in this application.
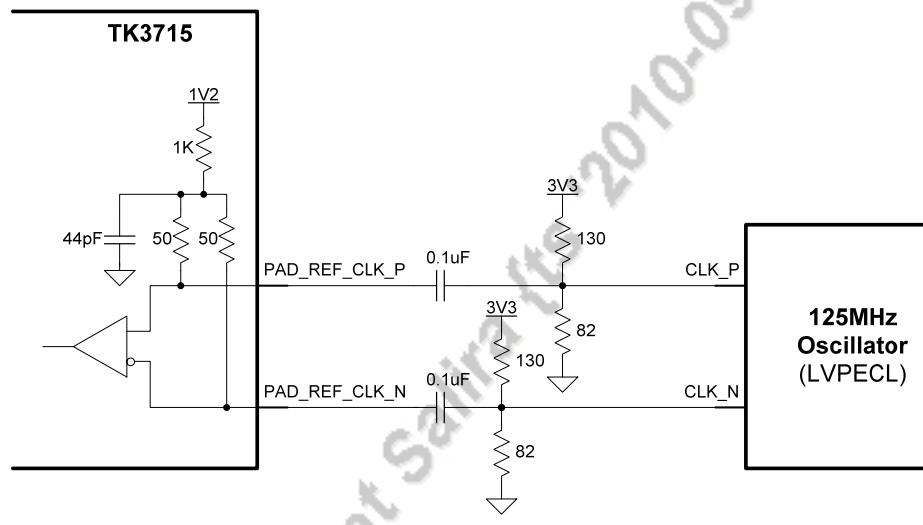
Figure 10.   Differential Clock Interface
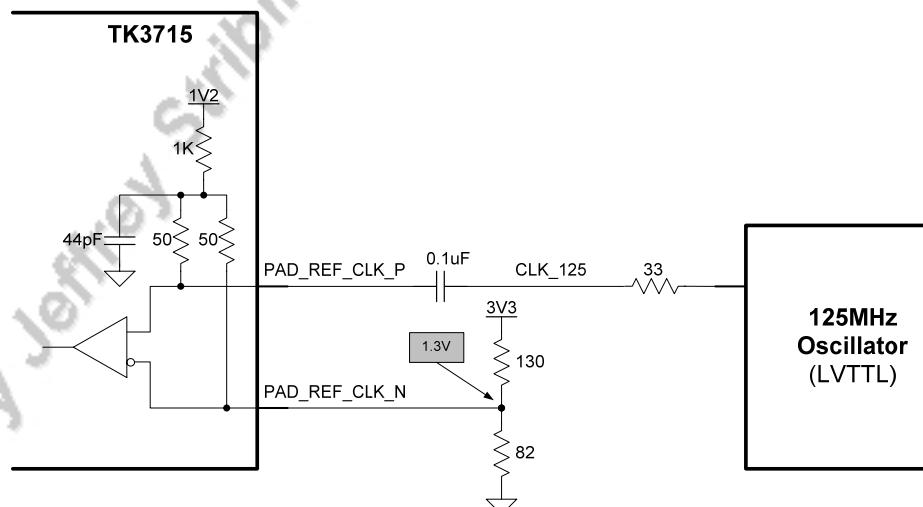
Figure 11.   Single-ended Clock Interface

The TK3715 supports two methods of loop-timing on the PON. The first method uses the Teknovus loop-time mode. Refer to Figure 12. This approach minimizes horizontal eye jitter and minimizes cost by eliminating an external CDR/PLL.
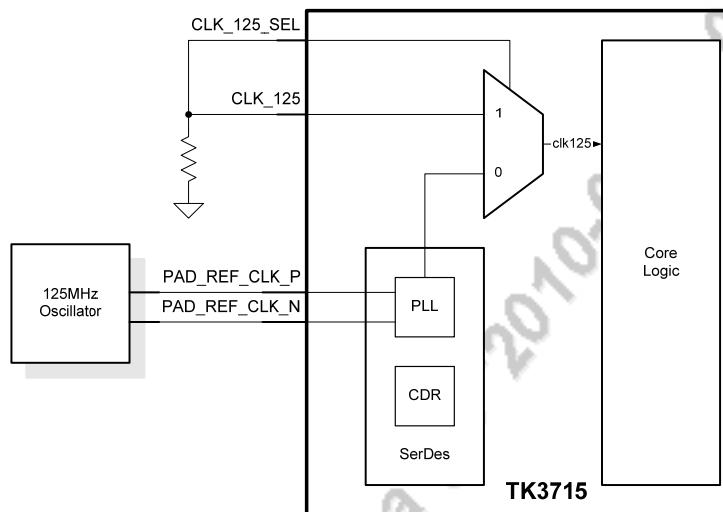
Figure 12.   Teknovus Loop-Timed Clock Mode

The second method uses true loop timing, with an external SerDes for receive clock recovery and jitter reduction. Refer to Figure 13. In both the Figure 12 and Figure 13 solutions, either a single-ended interface or a differential interface can be used for the PAD_REF_CLK_P/N signal.

Note: Only the differential interface is shown.
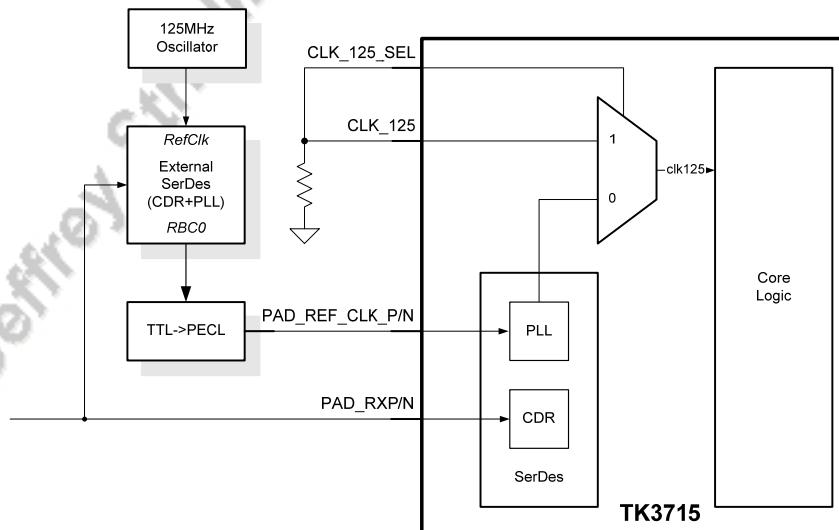
Figure 13.   PLL Loop-Timed Clock Mode

2.7   Internal 80C51 Processor

The 80C51 Processor is responsible for running Teknovus ONU firmware. It provides management (control-path) functionality, but is not required for data-path packet processing. The 80C51 requires external FLASH memory connected by a serial SPI interface. It requires 1MB of FLASH memory. Larger FLASH chips are supported. However, the extra memory will not be used. The 80C51 reads its firmware program and default ONU configuration data from the FLASH.

The TK3715 provides internal 256K x 8 SRAM. The SRAM is used as program memory for the 80C51 processor, and not for packet buffering.

A glueless interface is also provided for a standard 1M x 8 Serial FLASH memory. The Teknovus Host interface software is stored with the configuration data in the FLASH.

The FLASH memory must be capable of operating at least 16MHz clock rate and have 64KB sectors/blocks that are erasable with D8(hex) command. The following 8Mbit Serial FLASH memories are currently supported by Teknovus firmware:

- NexFlash NX25P80-V
- Winbond W25P80-V, W25P16-V, W25X80V
- ST Micro M25P80-V
- Macronix MX25L8005
- Eon Silicon EN25P80, EN25F80.
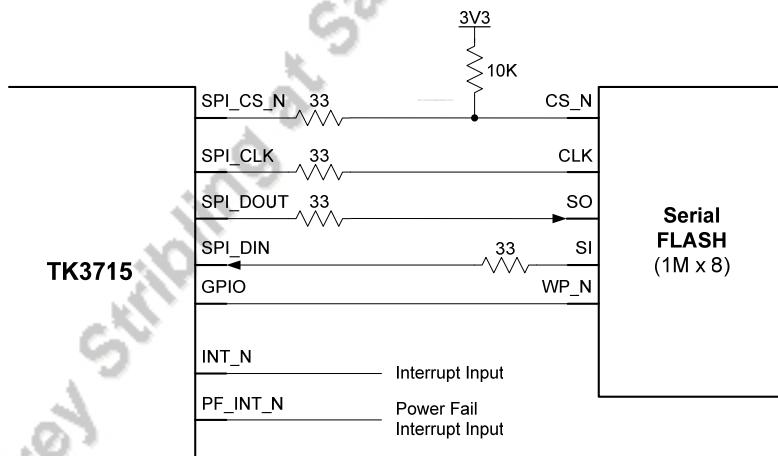

Figure 14.   FLASH Memory Connections

2.8   GPIO and GPO Interface

Twelve uncommitted GPIO pins are provided in the TK3715. A serial GPO interface is also provided. GPIO pins can be programmed as inputs or outputs. Refer to Figure 15. GPIO and GPO pins are programmable via the Personality Editor application.

Note: Teknovus does not recommend sinking or sourcing more than 8mA on any GPIO pin.
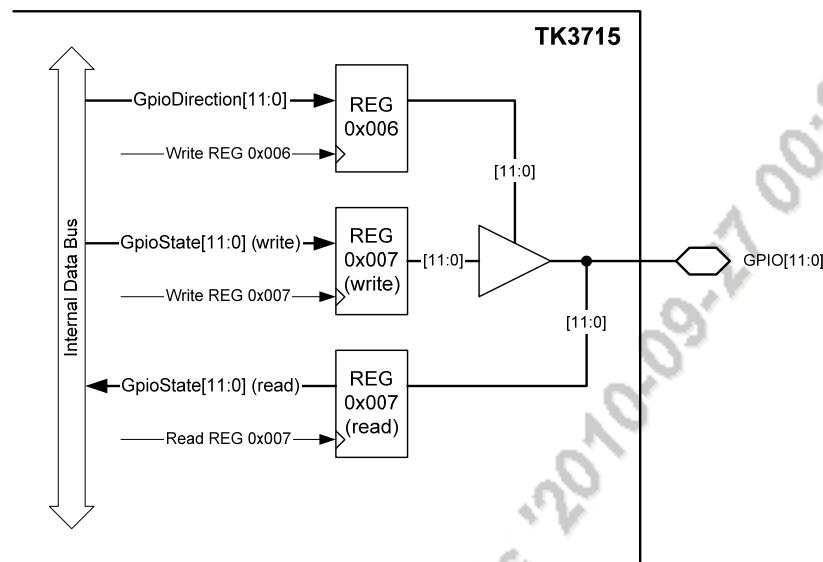
Figure 15.   Simplified GPIO Pin Block Diagram

The GPO interface is used with a serial shift register to drive LEDs. Acceptable shift registers include the TI CD74AC164 8-bit Shift Register. Up to 16 serial registers may be used externally. The hardware will shift out when updates are made to the internal register. The GPO may toggle outputs during shift cycles, and is recommended primarily for LEDs. The hardware also has the option to "flash" the LEDs at a visible rate. Refer to Figure 16.
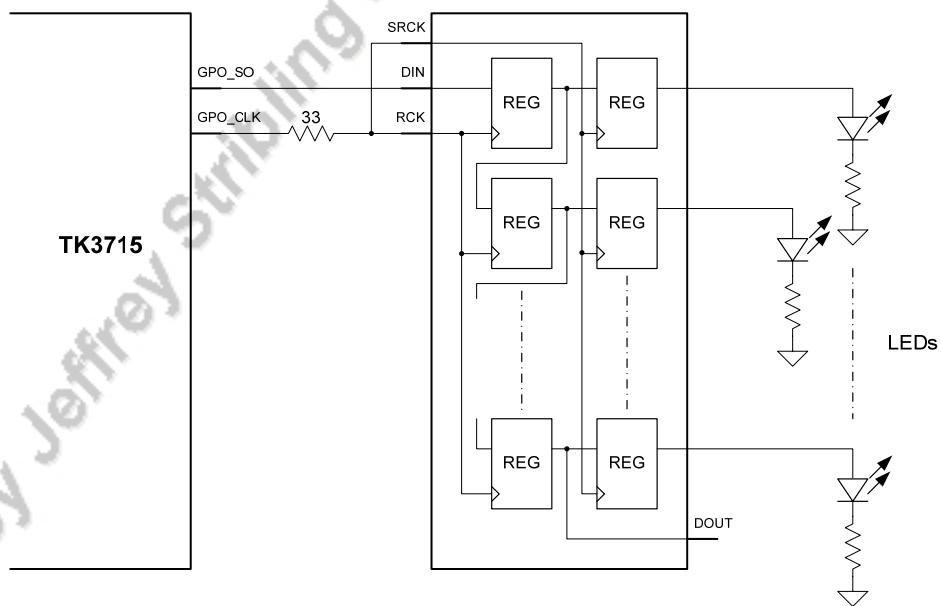
Figure 16.   Sample GPO Interface

2.9 UART Interface

The TK3715 provides two UART interfaces. The first interface enables debugging, and provides command line access to the ONU. The second UART interface is used for host monitor and emulator modes, and should be left unconnected.

The baud rate is generated from the 125.00MHz reference oscillator. An external RS-232 buffer, such as the Maxim MAX3222E, can be used to connect to a standard RS-232 connector. The Teknovus Host Interface software default line settings are as follows (refer to Figure 17):

- Baud Rate 9600
- No-Parity
- 8 bit Data
- 1 Stop bit

The first pin, UART_DOUT, refers to UART transmit data (output) from the TK3715. The second pin, UART_DIN, refers to UART receive data (input) to the TK3715. The UART interface is asynchronous; it does not include any clock.
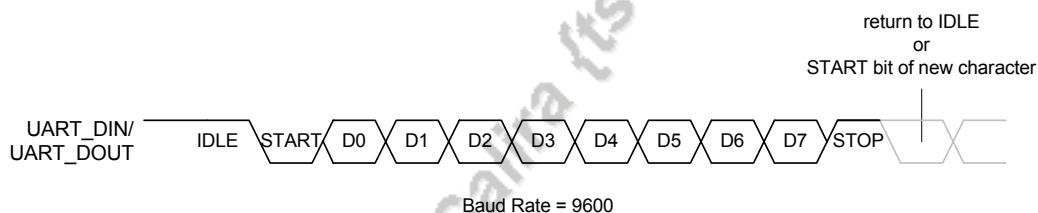
Figure 17. UART Interface Timing

2.10 Ethernet Serial Management Interface (MDIO)

The Ethernet serial management interface (MDIO) consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface, it is possible to control and configure multiple PHY devices, gather status and error information, and determine the type and capabilities of the attached PHY devices.
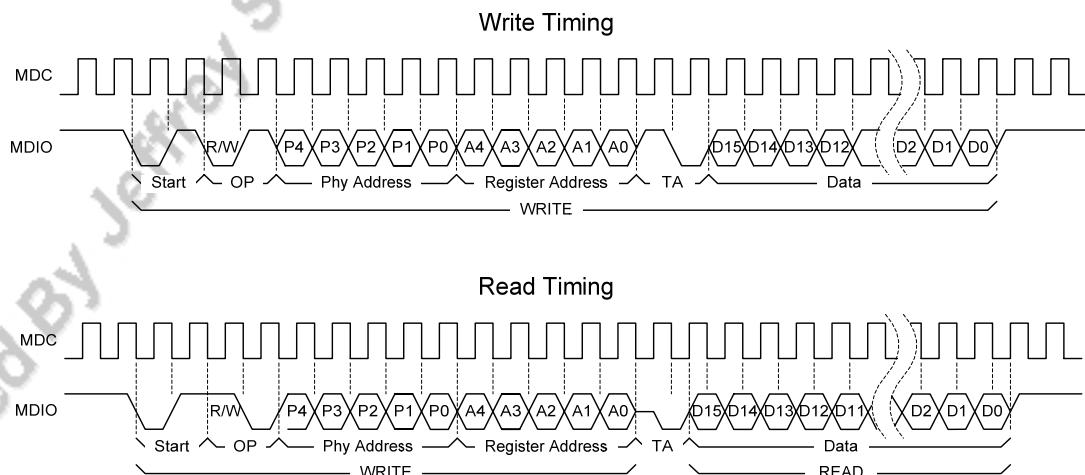
Figure 18. MII Serial Management Read and Write Timing Diagrams

2.11   JTAG Interface

A standard JTAG interface is provided for in-circuit testing. During normal TK3715 operation, JTAG is not functional. All JTAG pins should be pulled high except for the TRSTN pin. The TRSTN pin should be pulled low during normal TK3715 operation. TRSTN and JTAG_SEL pins should be pulled high during TK3715 JTAG operation. Please contact Teknovus for programming details. Teknovus offers a 4-bit instruction register that supports IEEE 1149.1 mandatory instructions, BYPASS, EXTEST and SAMPLE/PRELOAD. In addition, IDCODE and CLAMP instructions are supported. Chip identity and the manufacturer's identity can be read using the JTAG interface. Refer to Table 15 for supported instructions and their operation codes.

Table 15.   JTAG Instructions and Operations

Code	Instruction	Selected Register	Result			
0000	EXTEST	BSR	Outputs cells apply their values to ports. Input cells sample values on ports.			
0001	IDCODE	DEVICE IDENTITY	Captures 32-bit Identity with following fields.			
			Bits	**Field**	**Decimal**	**Hex**
			0	Default Value	1	0x1
			1:11	Teknovus Identity	515	0x203
			12:27	Part Number	3714*	0x0E82
			28:31	Part Version	1	0x0001
0010	SAMPLE/ PRELOAD	BSR	Sets up boundary scan cells to either sample values moving in or out of devices, or to preload the known values in Boundary Scan cells prior to the next operation.			
0011	CLAMP	BSR + BYPASS	First preset values in output cells are taken to output ports. BYPASS register is then selected between TDI and TDO pins.			
0100 to 1111	BYPASS	BYPASS	TDO pin gets the value of TDI pin on clock, all logic is bypassed.			

* Indicates an error for which an Errata Sheet has been issued.

Table 15 shows the IDCODE instruction illustration. The LSB (bit-0) for the 32-bit DEVICE IDENTITY register will always be "1".

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	1	1

Version 0x0001 — Part Number 0x0E82 (3714) — Teknovus JEDEC Identity 0x203
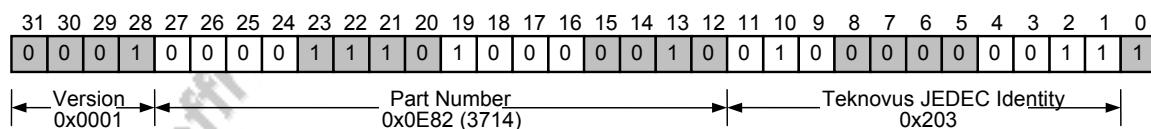
Figure 19.   Device Identity Register and its Fields for IDCODE Instruction

2.12   Power Sequencing and Reset

The 3.3V power supply should be brought up ahead of the 1.2V power supply. This provides proper biasing of the ESD protection diodes. The RST_N input must be held low for >100ms after the power supplies have stabilized. This allows the crystal oscillators to stabilize and all internal circuitry to initialize before code execution begins.

2.13 Noise Decoupling and Power Supply Recommendations

A multilayer PCB structure is recommended to limit power supply "ripple" noise. This structure will also prevent signal noise coupling through power planes. The most important capacitor is the capacitance between the ground and power layers in the PCB itself. Teknovus recommends putting the power and ground planes next to each other in the middle of the board with minimal spacing (<4.0mils). This increases capacitive coupling between the power and the ground planes, which filters noise from power planes to ground.

Note: All ground pins (including analog and thermal) should be tied together through a common system ground plane(s). Do not insert any inductor or ferrite bead between analog and digital ground planes.

2.13.1 Core Logic Power Supply

The core circuitry for the TK3715 operates at 1.2V. The power supply for core circuitry does not require any special filtering.

Note: Teknovus recommends that you de-couple as many VDDCORE pins as possible with a pair of 0.1uF and 0.01uF capacitors. The placement of each pair of capacitors is critical. They should be mounted as closely as possible to the de-coupled pin. The 0.01uF on the smaller value capacitor should be as close to the device as possible.

2.13.2 I/O Power Supply

Most of the TK3715 I/O pins operate at 3.3V. The power supply for I/O buffers does not require any special filtering.

Note: Teknovus recommends that each of the 11 VDDIO pins is de-coupled with a pair of 0.1uF and 0.01uF capacitors. The placement of each pair of capacitors is critical. They should be mounted as closely as possible to the de-coupled pin. The 0.01uF on the smaller value capacitor should be as close to the device as possible.
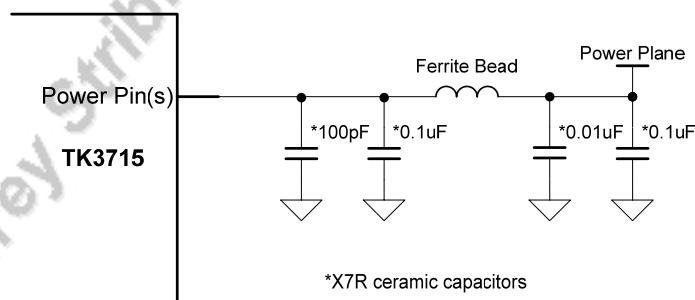
Figure 20. Power Supply Filter

3 TK3715 AC and DC Specifications

3.1 Absolute Maximum Ratings

Table 16.   Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	$V_{DD1.2}$	VDDCORE, PAD_VDD/VDDA	-0.25	1.32	V
	$V_{DD3.3}$	VDDIO, PAD_VDD33	-0.25	3.60	V
Storage Temperature	T_{stg}	-	-65	150	ºC
Junction Temperature	T_{Jmax}	-	-40	125	ºC
Voltage applied to any input pin	V_{PIN}	Undershoot/overshoot < 20% of the cycle on VSS/VDD	-0.25	VDD + 0.25	V
Power Dissipation	P_{MAX}	Zero Air Flow	-	2000	mW
I/O Latch-Up Current	$I_{LATCHUP}$	-	-200	200	mA
ESD Voltage at any pin	$V_{ESD(HBM)}$	Human Body Model	-2.0	2.0	KV

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Teknovus recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

3.2 Recommended Operating Conditions

Table 17. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	$V_{DD1.2}$	25ºC	1.14	1.20	1.26	V
	$V_{DD3.3}$	25ºC	3.14	3.30	3.46	V
Supply Voltage Noise	ΔV_{DD}	peak-to-peak (50KHz-100MHz)	-	-	50	mV
Operating Ambient Temperature	T_A	-	-40	25	85	ºC
Operating Junction Temperature	T_J	-	-30	70	110	ºC
Thermal Resistance Junction to Ambient for LQFP-128	Θ_{JA}*	JEDEC 2-layer PCB with no air flow	-	-	19.9	ºC/W
Thermal Resistance Junction to Ambient for TFBGA-169	Θ_{JA}*	JEDEC 4-layer PCB with no air flow	-	-	20.8	ºC/W
Thermal Resistance Junction to Case for LQFP-128	Θ_{JC}**	JEDEC with no air flow	-	-	10.7	ºC/W
Thermal Resistance Junction to Case for TFBGA-169	Θ_{JC}**	JEDEC with no air flow	-	-	4.3	ºC/W
Power Dissipation***	P_{VDDIO}	25ºC, 3.3V	-	115	250	mW
	$P_{VDDCORE}$	25ºC, 1.2V	-	420	750	mW
	P_{VDD_SERDES}	25ºC, 1.2V (PAD_VDD/VDDA)	-	130	170	mW
		25ºC, 3.3V (PAD_VDD33)	-	60	100	mW
	P_D	25ºC	-	725	1270	mW

* $\Theta_{JA} = (T_J - T_A)/P_{MAX}$

** $\Theta_{JC} = (T_J - T_C)/P_{TOP}$ where P_{TOP} is Power Dissipation from the top of the package

*** For 1.25Gbps and 2.5Gbps Rx rates

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3.3   DC Characteristics

Table 18.   DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current	$I_{DD3.3}$	25ºC, 3.3V	-	52	-	mA
	$I_{DD1.2}$	25ºC, 1.2V	-	460	-	mA
CMOS Input High Voltage	V_{IH}	25ºC	2.00	-	3.60	V
CMOS Input Low Voltage	V_{IL}	25ºC	-0.30	-	0.80	V
CMOS Output High Voltage	V_{OH}	25ºC	2.40	-	-	V
CMOS Output Low Voltage	V_{OL}	25ºC	-	-	0.40	V
CMOS Input Leakage Current	I_I	V_I = 3.3V or 0V	-	-	±10	uA
CMOS Tri-state Output Leakage Current	I_{OZ}	V_{OZ} = 3.3V or 0V	-	-	±10	uA
CMOS Output High Current	I_{OH}	C_{LOAD} = 50pF @ V_{OH} = 2.4V	5.8	9.5	13.3	mA
CMOS Output Low Current	I_{OL}	C_{LOAD} = 50pF @ V_{OL} = 0.4V	4.7	9.9	16.9	mA
PAD_RXP/N Inputs Differential Voltage	V_{ID}	Differential (peak-peak)	400	-	1200	mV
PAD_RXP/N Inputs Common Mode Voltage	V_{ICM}	-	600	-	1000	mV
PAD_RXP/N DC Input Impedance	R_{ISE}	Single-Ended	40	50	60	Ω
PAD_RXP/N DC Input Impedance	R_{ID}	Differential	80	100	120	Ω
PAD_TXP/N Absolute Output Differential Voltage (into floating 100Ω load)	V_{OD}	Differential (peak-peak)	400	-	1000	mV
PAD_TXP/N Outputs Common Mode Voltage	V_{OCM}	-	400	600	900	mV
PAD_TXP/N DC Output Impedance	R_{OSE}	Single-Ended	40	50	60	Ω
PAD_TXP/N DC Output Impedance	R_{OD}	Differential	80	100	120	Ω
PAD_TXP/N Short Circuit Current	I_{SHORT}	-	-30	-	30	mA
PAD_REF_CLK_P/N Input Differential Voltage	$V_{IDREFCLK}$	Differential (peak-peak)	200	800	1600	mV
PAD_REF_CLK_P/N Inputs Common Mode Voltage	$V_{CMREFCLK}$	-	1000	1200	1400	mV
PAD_REF_CLK_P/N Input Impedance	Z_{REFCLK}	Differential	70	100	130	Ω
Frequency Tolerance (CLK_125, PAD_CLK_REF_P/N)	CLK_{125MHz}	-	-100	-	+100	ppm
Input Capacitance	C_{IN}	-	-	5	-	pF

3.4 AC Characteristics

3.4.1 System and SerDes Clocks Timing

Table 19. System and SerDes Reference Clocks Timing

Description	Symbol	Min	Max	Unit
CLK_125, PAD_REF_CLK_P/N Pulse Width (High)	t_1	3.6	4.4	ns
CLK_125, PAD_REF_CLK_P/N Pulse Width (Low)	t_2	3.6	4.4	ns
CLK_125, PAD_REF_CLK_P/N Duty Cycle	-	40	60	%
CLK_125, PAD_REF_CLK_P/N Clock Period	t_3	7.9992	8.0008	ns
CLK_125, PAD_REF_CLK_P/N Total Jitter (peak-peak)	TJ_{p-p}	-	40	ps
CLK_25 Pulse Width (High)	t_1	18.0	22.0	ns
CLK_25 Pulse Width (Low)	t_2	18.0	22.0	ns
CLK_25 Duty Cycle	-	45.0	55.0	%
CLK_25 Clock Period	t_3	39.996	40.004	ns

CLK_125, PAD_REF_CLN_P/N (inputs),
CLK_25 (output)
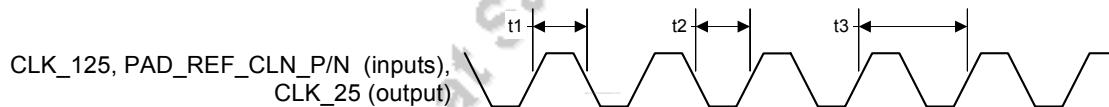
Figure 21.   System and SerDes Clock Timing

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3.4.2   Local-Side MII Input Timing of the 10/100 Ethernet Port

Table 20.   Local-Side MII Input Timing of the 10/100 Ethernet Port

| Description	Symbol	Min	Max	Unit
MII_RXCLK Pulse Width (High) (100Mbps)	t_1	18.0	22.0	ns
MII_RXCLK Pulse Width (High) (10Mbps)		180.0	220.0	ns
MII_RXCLK Pulse Width (Low) (100Mbps)	t_2	18.0	22.0	ns
MII_RXCLK Pulse Width (Low) (10Mbps)		180.0	220.0	ns
MII_RXCLK Duty Cycle	-	40	60	%
MII_RXCLK Clock Period (100Mbps)	t_3	36.0	44.0	ns
MII_RXCLK Clock Period (10Mbps)		360.0	440.0	ns
MII_RXDV, MII_RXER, MII_RXD[3..0] Setup to MII_RXCLK Rising Edge	t_4	10.0	-	ns
MII_RXDV, MII_RXER, MII_RXD[3..0] Hold after MII_RXCLK Rising Edge	t_5	0.0	-	ns
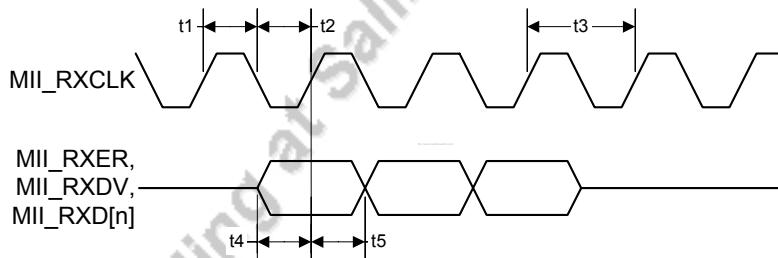
Figure 22.   Local-Side MII Input Timing of the 10/100 Ethernet Port

3.4.3 Local-Side MII Output Timing of the 10/100 Ethernet Port

Table 21. Local-Side MII Output Timing of the 10/100 Ethernet Port

| Description	Symbol	Min	Max	Unit
MII_TXCLK Pulse Width (High) (100Mbps)	t_1	18.0	22.0	ns
MII_TXCLK Pulse Width (High) (10Mbps)		180.0	220.0	ns
MII_TXCLK Pulse Width (Low) (100Mbps)	t_2	18.0	22.0	ns
MII_TXCLK Pulse Width (Low) (10Mbps)		180.0	220.0	ns
MII_TXCLK Duty Cycle	-	40	60	%
MII_TXCLK Clock Period (100Mbps)	t_3	36.0	44.0	ns
MII_TXCLK Clock Period (10Mbps)		360.0	440.0	ns
MII_TXEN, MII_TXER, MII_TXD[3:0] Setup to MII_TXCLK Rising Edge*	t_4	10.0/ 15.0	-	ns
MII_TXEN, MII_TXER, MII_TXD[3:0] Hold after MII_TXCLK Rising Edge*	t_5	10.0/ 0.0	-	ns

* Programmable Value (PHY/MAC mode).
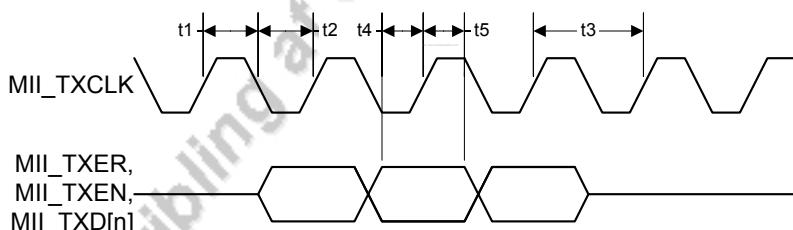
Figure 23. Local-Side MII Output Timing of the 10/100 Ethernet Port

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3.4.4 Local-Side MII/GMII Input Timing of the 10/100/1000 Ethernet Port

Table 22.   Local-Side MII/GMII Input Timing of the 10/100/1000 Ethernet Port

Description	Symbol	Min	Max	Unit
GMII_RXCLK Pulse Width (High) (100Mbps)	t_1	18.0	22.0	ns
GMII_RXCLK Pulse Width (High) (10Mbps)		180.0	220.0	ns
GMII_RXCLK Pulse Width (Low) (100Mbps)	t_2	18.0	22.0	ns
GMII_RXCLK Pulse Width (Low) (10Mbps)		180.0	220.0	ns
GMII_RXCLK Duty Cycle	-	40	60	%
GMII_RXCLK Clock Period (100Mbps)	t_3	36.0	44.0	ns
GMII_RXCLK Clock Period (10Mbps)		360.0	440.0	ns
GMII_RXDV, GMII_RXER, GMII_RXD[3..0] Setup to GMII_RXCLK Rising Edge	t_4	10.0	-	ns
GMII_RXDV, GMII_RXER, GMII_RXD[3..0] Hold after GMII_RXCLK Rising Edge	t_5	0.0	-	ns
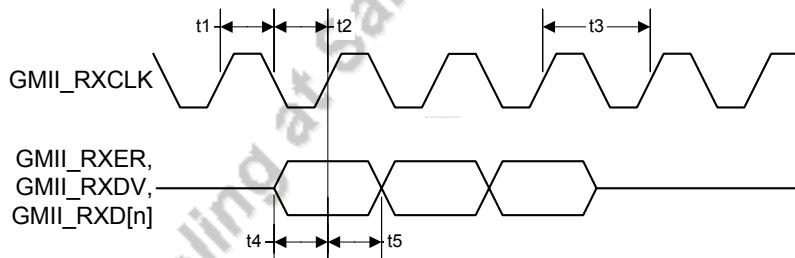
Figure 24.   Local-Side MII/GMII Input Timing of the 10/100/1000 Ethernet Port

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3.4.5 Local-Side MII/GMII Output Timing of the 10/100/1000 Ethernet Port

Table 23.   Local-Side MII/GMII Output Timing of the 10/100/1000 Ethernet Port

| Description	Symbol	Min	Max	Unit
GMII_TXCLK Pulse Width (High) (100Mbps)	t_1	18.0	22.0	ns
GMII_TXCLK Pulse Width (High) (10Mbps)		180.0	220.0	ns
GMII_TXCLK Pulse Width (Low) (100Mbps)	t_2	18.0	22.0	ns
GMII_TXCLK Pulse Width (Low) (10Mbps)		180.0	220.0	ns
GMII_TXCLK Duty Cycle	-	40	60	%
GMII_TXCLK Clock Period (100Mbps)	t_3	36.0	44.0	ns
GMII_TXCLK Clock Period (10Mbps)		360.0	440.0	ns
GMII_TXEN, GMII_TXER, GMII_TXD[3..0] Setup to GMII_TXCLK Rising Edge*	t_4	10.0/ 15.0	-	ns
GMII_TXEN, GMII_TXER, GMII_TXD[3..0] Hold after GMII_TXCLK Rising Edge*	t_5	10.0/ 0.0	-	ns

* Programmable Value (PHY/MAC mode).
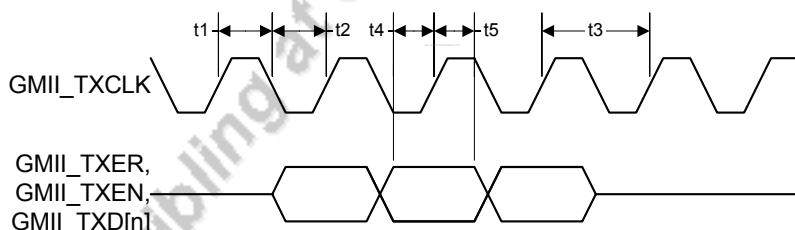
Figure 25.   Local-Side MII/GMII Output Timing of the 10/100/1000 Ethernet Port

3.4.6 Local-Side TBI/GMII Input Timing

Table 24. Local-Side TBI Input Timing

Description	Symbol	Min	Max	Unit
TBI_RBC[1..0] Clock Pulse Width (High)	t_1	7.5	-	ns
TBI_RBC[1..0] Clock Pulse Width (Low)	t_2	7.5	-	ns
TBI_RBC[1..0] Clock Duty Cycle	-	40	60	%
TBI_RBC[1..0] Clock Period	t_3	15.0	-	ns
TBI_RXD[9..0] Setup to TBI_RBC[1..0] Rising Edge	t_4	2.0	-	ns
TBI_RXD[9..0] Hold after TBI_RBC[1..0] Rising Edge	t_5	1.0	-	ns
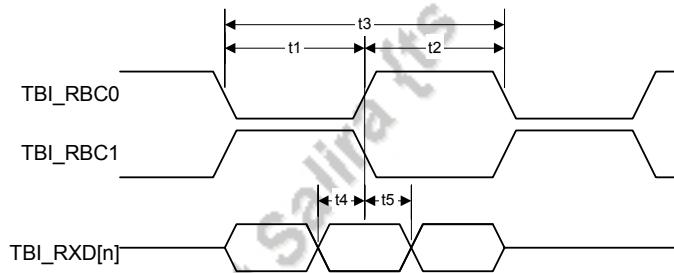
Figure 26. Local-Side TBI Input Timing

Table 25. Local-Side GMII Input Timing

| Description	Symbol	Min	Max	Unit
GMII_RXCLK Pulse Width (High)	t_1	2.5	-	ns
GMII_RXCLK Pulse Width (Low)	t_2	2.5	-	ns
GMII_RXCLK Duty Cycle	-	40	60	%
GMII_RXCLK Clock Period	t_3	7.5	-	ns
GMII_RXDV, GMII_RXER, GMII_RXD[7..0] Setup to GMII_RXCLK Rising Edge	t_4	2.0	-	ns
GMII_RXDV, GMII_RXER, GMII_RXDV, GMII_RXD[7..0] Hold after GMII_RXCLK Rising Edge	t_5	0.0	-	ns
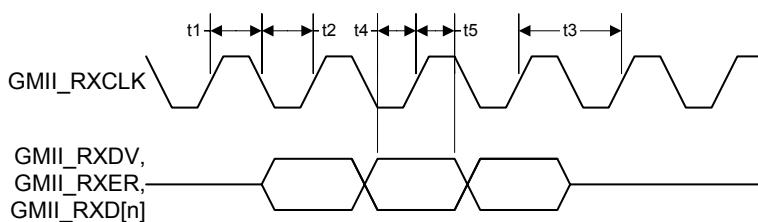
Figure 27. Local-Side GMII Input Timing

3.4.7 Local-Side TBI/GMII Output Timing

Table 26.   Local-Side TBI/GMII Output Timing

| Description	Symbol	Min	Max	Unit
GMII_GTXCLK/TBI_TXCLK Pulse Width (High)	t_1	2.5	-	ns
GMII_GTXCLK/TBI_TXCLK Pulse Width (Low)	t_2	2.5	-	ns
GMII_GTXCLK/TBI_TXCLK Duty Cycle	-	45	55	%
GMII_GTXCLK/TBI_TXCLK Clock Period	t_3	7.5	8.5	ns
GMII_TXEN, GMII_TXER, GMII_TXD[7..0], TBI_TXD[9..0] Setup to GMII_GTXCLK/TBI_TXCLK Rising Edge	t_4	2.5	-	ns
GMII_TXEN, GMII_TXER, GMII_TXD[7..0], TBI_TXD[9..0] Hold after GMII_GTXCLK/TBI_TXCLK Rising Edge	t_5	1.5	-	ns
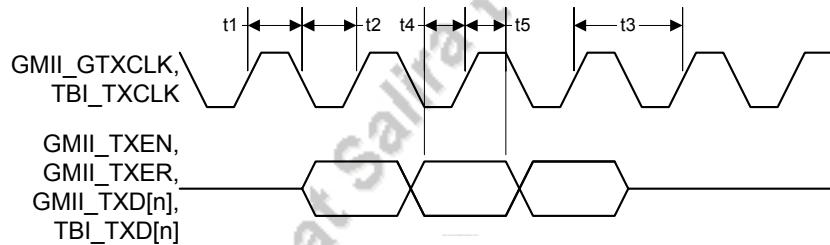
Figure 28.   Local-Side TBI/GMII Output Timing

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3.4.8   Ethernet Serial Management Timing (MDIO)

Table 27.   Ethernet Serial Management Timing

Description	Symbol	Min	Max	Unit
MDC Pulse Width (High)	t_1	510.0	514.0	ns
MDC Pulse Width (Low)	t_2	510.0	514.0	ns
MDC Clock Period	t_3	1.020	1.028	ns
MDIO (Output) Setup to MDC Rising Edge	t_4	40.0	-	ns
MDIO (Output) Hold Time from MDC Rising Edge	t_5	40.0	-	ns
MDIO (Input) Setup to MDC Falling Edge	t_6	20.0	-	ns
MDIO (Input) Hold Time from MDC Falling Edge	t_7	20.0	-	ns

Figure 29.   MDIO Timing

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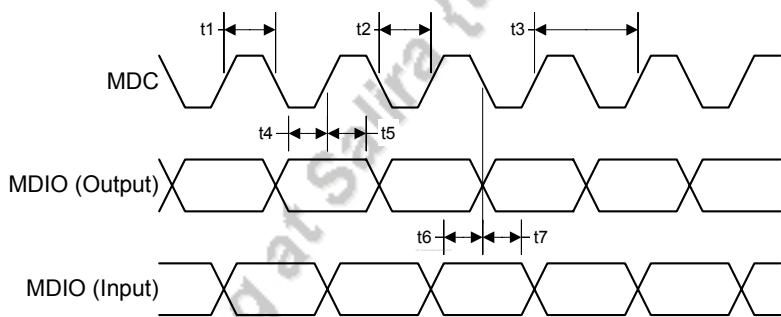
3.4.9   SerDes Timing

Table 28.   SerDes Output Timing

Description	Symbol	Min	Typ	Max	Unit
PAD_TXP/N Rise time	t_1	100.0	-	200.0	ps
PAD_TXP/N Fall time	t_2	100.0	-	200.0	ps
PAD_TXP to PAD_TXN Skew	t_3	-	-	50.0	ps
SerDes Total Transmit Jitter	TJ_{E-12}[1,2]	-	67.3	152.0[1]	ps
SerDes Total Transmit Jitter	TJ_{p-p}[2]	-	43.0	-	ps

[1] Defined at BER 10^{-12} above 637KHz as recommended by IEEE Draft P802.3ah™/D3.3; Section 60.6 (Table 60-11 for TP1).

[2] Using LVPECL 125MHz oscillator with TJ_{p-p} of less than 40ps (pk-pk) for reference clock signals PAD_REF_CLK_P/N.
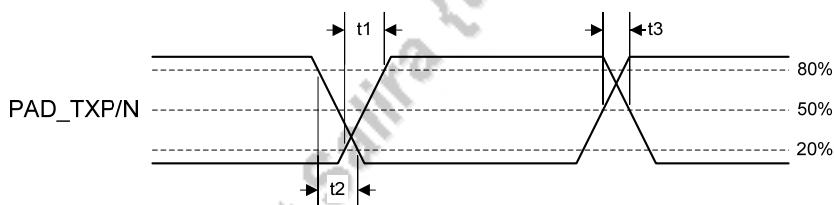
Figure 30.   SerDes Output Timing

Table 29.   SerDes Input Timing

Description	Symbol	Min	Typ	Max	Unit[3]
SerDes Total Input Jitter Tolerance	TJ_{E-12}[1,2]	0.749[1]	-	-	UI
SerDes Deterministic Input Jitter Tolerance	DJ_{p-p}[1,2]	0.462[1]	0.850	-	UI

[1] As recommended by IEEE Draft P802.3ah™/D3.3; Section 60.6 (Table 60-10 for TP4).

[2] Using LVPECL 125MHz oscillator with TJ_{p-p} of less than 40ps (pk-pk) for reference clock signals PAD_REF_CLK_P/N.

[3] UI = Unit Interval = 800ps for 1.25Gbps; 400ps for 2.5Gbps.

3.4.10   SPI Timing

Table 30.   SPI Timing

Description	Symbol	Min	Max	Unit
SPI_SCLK Pulse Width (High)	t_1	16.0	64.0	ns
SPI_SCLK Pulse Width (Low)	t_2	16.0	64.0	ns
SPI_CS_N Inactive Time	t_3	64.0	-	ns
SPI_CS_N Low to SPI_SCLK Setup Time	t_4	12.0	-	ns
SPI_ DOUT Setup to SPI_SCLK Rising Edge	t_5	12.0	-	ns
SPI_ DOUT Hold after SPI_SCLK Rising Edge	t_6	12.0	-	ns
SPI_ CS_N Hold after SPI_SCLK Falling Edge	t_7	28.0	-	ns
SPI_ DIN Setup to SPI_SCLK Rising Edge	t_8	12.0	-	ns
SPI_ DIN Hold after SPI_SCLK Rising Edge	t_9	12.0	-	ns
SPI_SCLK Rising Edge to SPI_DIN High-Z	t_{10}	12.0	(t_1+t_2)	ns
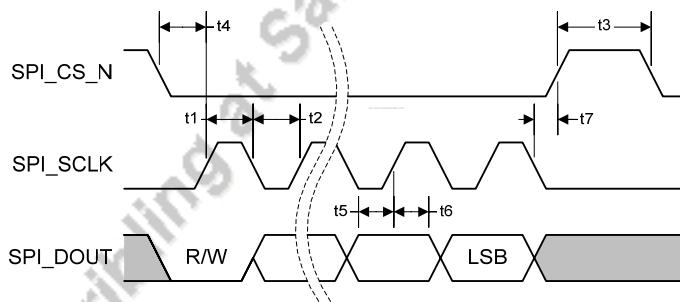
Figure 31.   SPI Write Timing
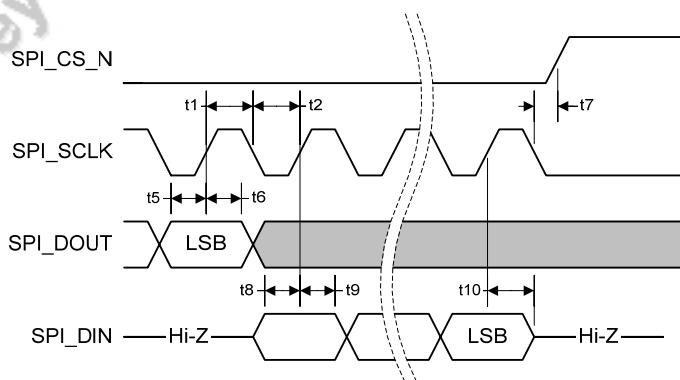
Figure 32.   SPI Read Timing

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3.4.11   Reset and CLK_25 Timing

Table 31.   Reset and CLK_25 Timing

| Description	Symbol	Min	Max	Unit
Power On to RST_N High	t_1	10.0	-	ms
RST_N Pulse Width	t_2	1.0	-	ms
CLK_25 Valid before RST_N De-assertion	t_3	500	-	us
CLK_25 Invalid After RST_N Assertion	t_4	-	200	ns
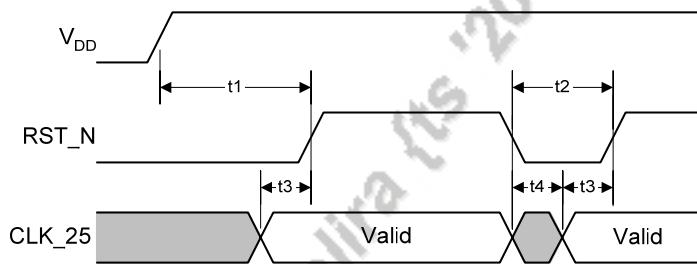
Figure 33.   Reset and CLK_25 Timing

# 4   TK3715 Physical Dimensions

4.1   LQFP-128 Package
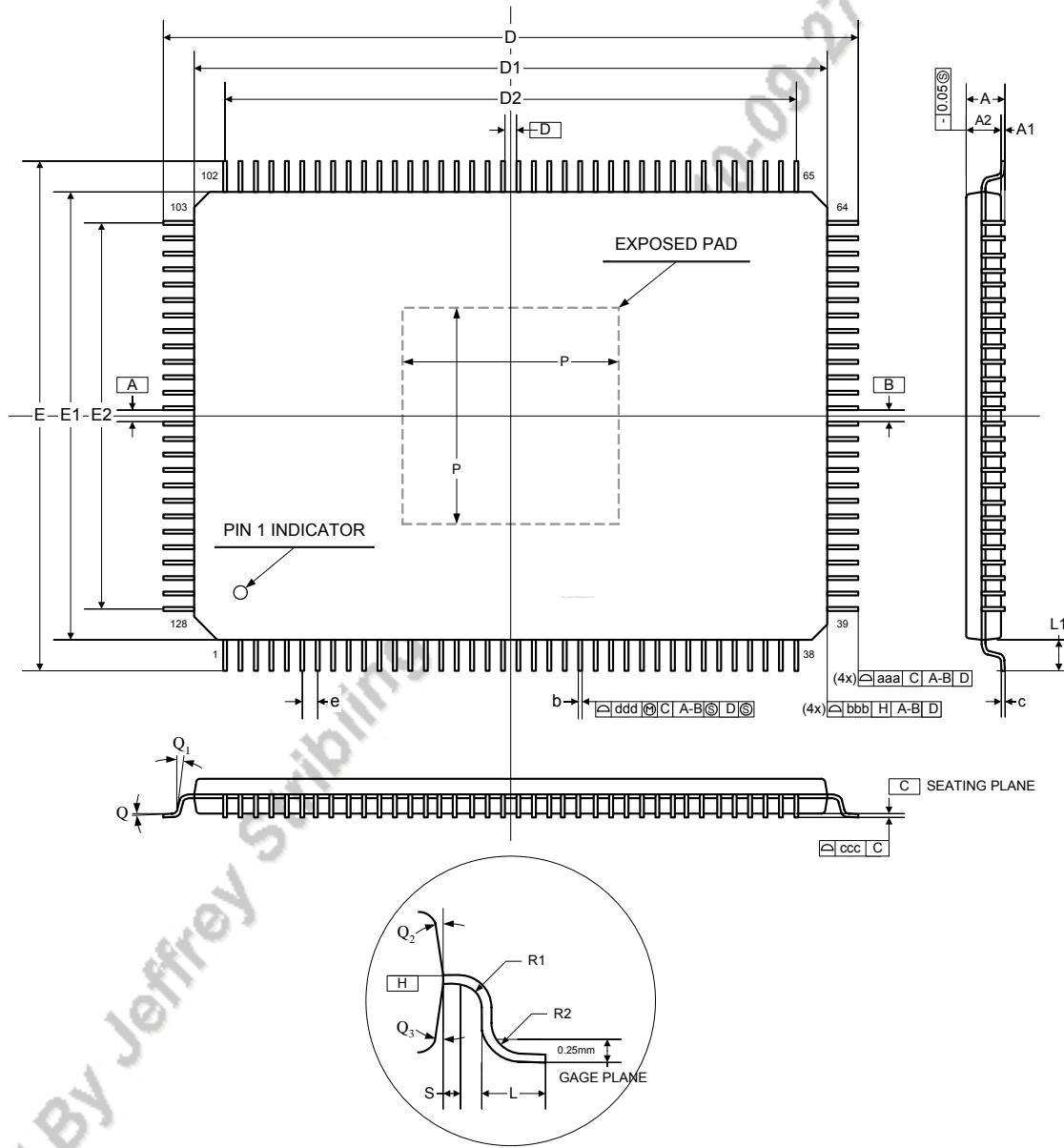
Figure 34.   LQFP-128 Package Drawing

Table 32.   LQFP-128 Package Dimensions

Reference	Min	Typ	Max	Unit
A	-	-	1.60	mm
A1	0.05	-	0.15	mm
A2	1.35	1.40	1.45	mm
D	22.00 BSC.			mm
D1	20.00 BSC.			mm
D2	18.50			mm
E	16.00 BSC.			mm
E1	14.00 BSC.			mm
E2	12.50			mm
R1	0.08	-	-	mm
R2	0.08	-	0.20	mm
Q	0D	3.5º	7D	mm
Q_1	0º	-	-	mm
Q_2	11D	12.0º	13D	mm
Q_3	11D	12.0º	13D	mm
c	0.09	-	0.20	mm
L	0.45	0.60	0.75	mm
L_1	1.00 REF			mm
S	0.20	-	-	mm
P	8.00	-	8.10	mm
b	0.17	0.20	0.27	mm
e	0.50 BSC.			mm
aaa	0.20			mm
bbb	0.20			mm
ccc	0.08			mm
ddd	0.08			mm

Notes:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

2. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08mm.

3. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm.

4.1.1   LQFP-128 Exposed Pad PCB Design Guidelines

The TK3715 LQFP-128 package has an exposed pad at the bottom to provide the primary heat removal path. It also provides grounding to the Printed Circuit Board (PCB). The exposed pad allows reduction of the loop inductance, providing an excellent grounding method for high frequency applications.

The exposed pad must be soldered directly to the PCB to benefit from the improved thermal and electrical behavior. A land pattern must be incorporated on the PCB within the footprint of the package. The land pattern must correspond to the exposed metal pad on the package. Refer to Figure 35.
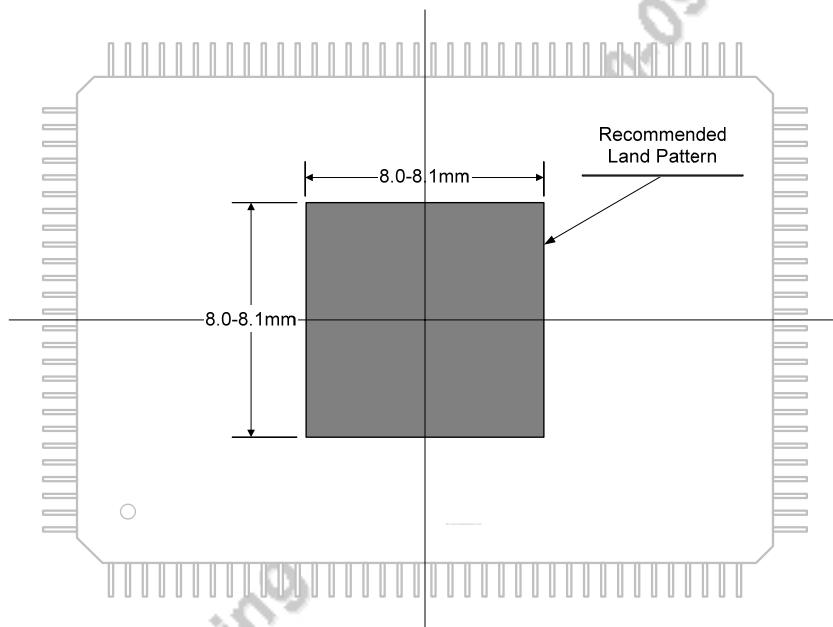

Figure 35.   Recommended Land Pattern

The land pattern on the PCB performs the heat transfer and the electrical grounding from the package to the board. This is done through a solder joint. Thermal vias and/or the plated hole (solder port) are required to effectively conduct heat from the surface of the PCB to the ground plane(s). These vias and/or the plated hole act as "heat pipes."

In some cases, only thermal vias are used to connect the exposed pad to the underlying ground planes. In these cases, an array of vias must be incorporated on the land pattern at 1.0 to 1.5mm grid. This will achieve maximum thermal and electrical performance. Refer to Figure 36. It is recommended that the array of vias is constructed with at least 25 vias. Teknovus also recommends that via diameter be 0.30 to 0.35mm, with at least 0.5 oz. copper via barrel plating.
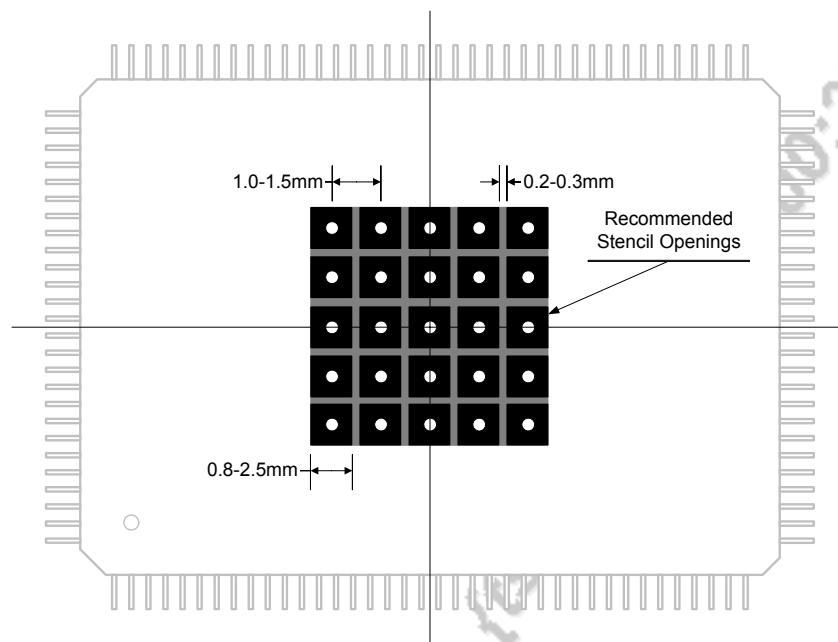
Figure 36.   Recommended Vias Grid Dimensions and Stencil Openings

The thermal vias and the plated hole together provide a superior thermal and electrical solution. They also improve re-manufacturing capabilities. In this solution, the array of vias can be incorporated on the land pattern at 1.0 to 1.5mm grid. The plated hole should have a 2.5mm diameter. Refer to Figure 37. Via diameter should be 0.30 to 0.35mm, with at least 0.5 oz. copper via barrel plating.
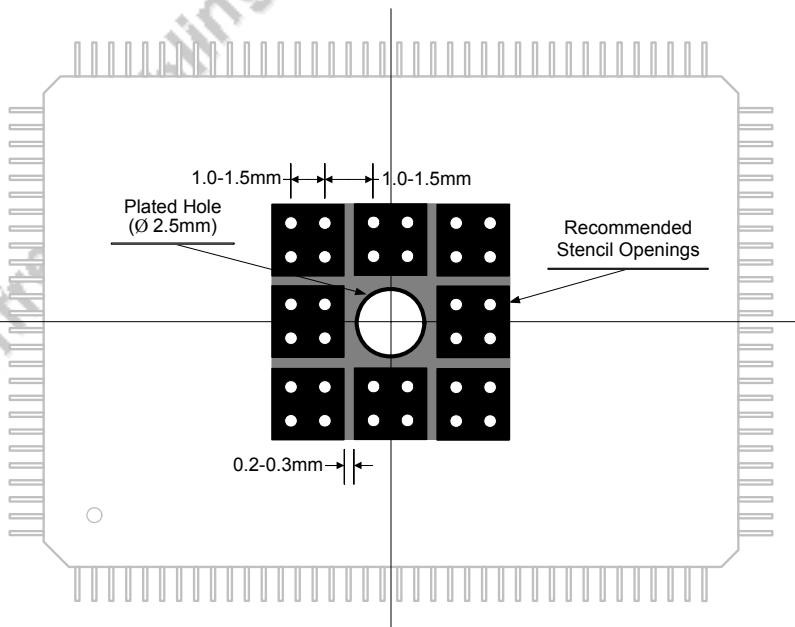

Figure 37.   Vias and Plated Hole Dimensions

Solder paste must be applied to both the exposed pad of the TK3715 package and the land pattern on the PCB. This will ensure proper soldering. The package stand-off must be considered when determining the stencil thickness. For a nominal stand-off of 0.1mm, Teknovus recommends a stencil thickness of 0.125 to 0.200mm.

A large stencil opening may result in poor release. Therefore, the aperture opening should be subdivided into an array of smaller openings of less than 2.5mm. Refer to the black areas in Figure 36 and Figure 37. The guidelines above enable the solder joint area to be 80% to 90% of the exposed pad area.

4.2 TFBGA-169 Package
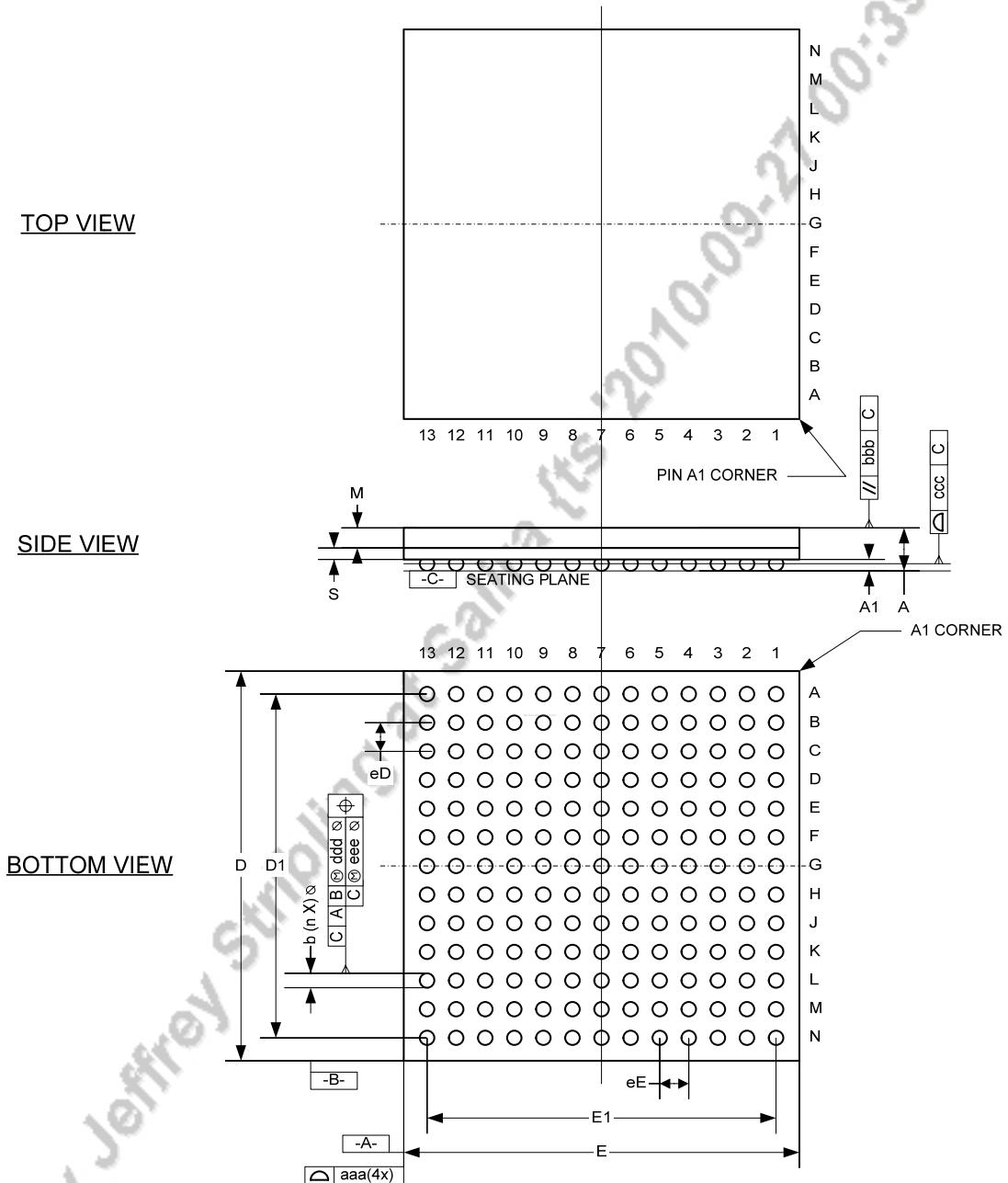
Figure 38.   TFBGA-169 Package Drawing

Table 33. TFBGA-169 Package Dimensions

Reference		Symbol	Common Dimension	Unit
Package Type		-	TFBGA	-
Ball Count		n	169	-
Body Size	X	E	11.000	mm
	Y	D	11.000	mm
Ball Pitch	X	eE	0.800	mm
	Y	eD	0.800	mm
Total Thickness		A	1.200 Max.	mm
Mold Thickness		M	0.530 Ref.	mm
Substrate Thickness		S	0.360 Ref.	mm
Ball Diameter		-	0.350	mm
Stand Off		A1	0.220 ~ 0.320	mm
Ball Width		b	0.320 ~ 0.420	mm
Package Edge Tolerance		aaa	0.150	mm
Mold Flatness		bbb	0.200	mm
Co-planarity		ccc	0.080	mm
Ball Offset (Package)		ddd	0.150	mm
Ball Offset (Ball)		eee	0.080	mm
Edge Ball Center To Center	X	E1	9.600	mm
	Y	E1	9.600	mm

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5 TK3715 Ordering Information
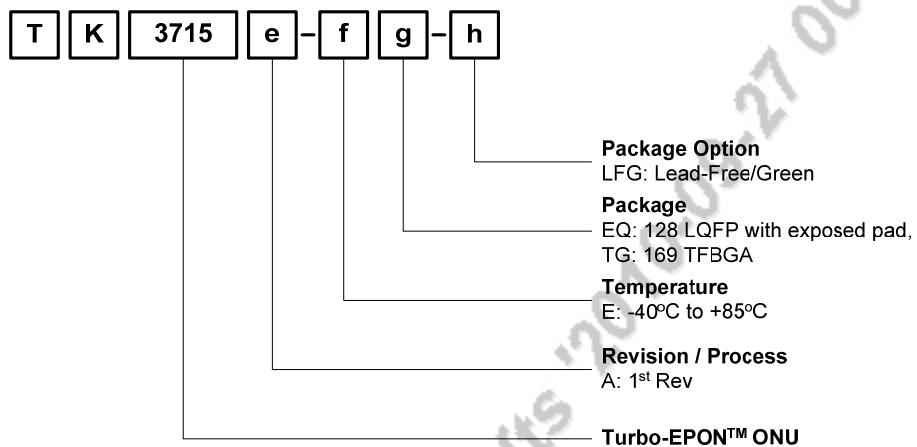
Figure 39. TK3715 Ordering Information

NOTICE

A **Data Sheet** is a technical document that describes the functionality of a device or component, including the electrical characteristics, packaging, and signal connections. In the semiconductor industry, Data Sheet information develops as the product progresses through its life-cycle. Therefore, in accordance with industry standards, Teknovus categorizes its Data Sheets as follows:

- **Product Preview** – A Product Preview documents the current state of a new product or concept. Functional definitions may be included, but all information is subject to change, including the company's commitment to develop and manufacture the product. Changes are not subject to Product Change Notification.

- **Advance Information** – Advance Information refers to the Data Sheet for a product that is in design or early prototyping. The Data Sheet includes the pin-out or ball-out and package definition, but these definitions may change due to evolving design, function, or timing requirements. All AC or DC operating parameters are subject to change, pending device characterization. Changes are communicated to customers via emailed Product Change Notifications.

- **Preliminary** – A Preliminary Data Sheet describes a device that is in the early stages of volume manufacturing. AC and DC operating parameters are subject to change, pending further characterization of multiple wafer lots. Changes are communicated to customers via emailed Product Change Notifications.

- **No Label** – Contents of an unlabeled Data Sheet should be stable, although contents may be updated due to refined characterization, bug discovery, and manufacturing issues. Changes are communicated to customers via emailed Product Change Notifications.

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