S6B0725A

104 SEG / 65 COM DRIVER & CONTROLLER FOR STN LCD

Aug. 2001

Ver. 1.5

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

S6B0725A Specification Revision History		
Version	**Content**	**Date**
0.0	Initial version	2000.07
1.0	1. VLCD pin: Input or output pin → only output pin (page 8, 24) 2001. Regulator resistor select: (1,1,0), (1,1,1) → not available (page 27, 38) 2001. VLCD absolute maximum rating:-0.3V to 15V → -0.3V to 13V (page 47) 4. X4 voltage boosting VCI range: 2.4V to 3.3V → 2.4V to 3.0V (page 48) 5. Power consumption: TBD valid value	2000.10
1.1	Oscillator frequency (f_{CL}): (TYP.) 4.75KHz → 5.45KHz (page 48)	2000.11
1.2	VLCD capacitor is greater than 1μF (page 8, 61)	2001.01
1.3	1. Figure 15 is changed (page 27) 2001. Figure 2-1, 2-2 are added (page 14) 2001. Figure 21 is changed (page 43) 4. Table 21 is changed (page 50) 5. Added detail information for several items	2001.03
1.4	Added dynamic current consumption at 4 times boosting operation (page 48)	2001.05
1.5	Correct some misspellings	2001.08

CONTENTS

INTRODUCTION

The S6B0725A is a single-chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 104 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 104 segment driver circuits, so that a single chip can drive a 65 x 104 dot display. This chip is able to minimize power consumption because it performs display data RAM read/write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amp for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Display Driver Output Circuits

– 65 common outputs and 104 segment outputs

On-chip Display Data RAM

– Capacity: 65 x 104 = 6,760 bits
– RAM bit data " 1" : a dot of display is illuminated
– RAM bit data " 0" : a dot of display is not illuminated

Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/7 or 1/9	65 × 104
1/55	1/6 or 1/8	55 × 104
1/49	1/6 or 1/8	49 × 104
1/33	1/5 or 1/6	33 × 104

Microprocessor Interface

– High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
– SPI (Serial Peripheral Interface) available. (Only write operation)

Various Function Set

– Display ON / OFF, set initial display line, set page address, set column address, read status, write/read display data, select segment driver output, reverse display ON / OFF, entire display ON / OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for VLCD voltage regulation, electronic volume, set static indicator state.
– H/W and S/W Reset available
– Static drive circuit equipped internally for indicators with 4 flashing mode

Built-in Analog Circuit

- On-chip oscillator circuit for display clock
- High performance voltage converter (with booster ratios of x3 and x4)
- High accuracy voltage regulator (temperature coefficient: -0.05 ± 0.03%/°C or external input)
- Electronic contrast control function (64 steps)
- Vref = 2.1V ± 3% (VLCD voltage adjustment voltage)
- High performance voltage follower (V1 to V4 voltage divider resistors and OP-Amp for increasing drive capacity)

Operating Voltage Range

- Supply voltage (V_{DD}): 2.4 to 3.6 V
- LCD driving voltage (V_{LCD}): 4.5 to 9.0 V

Low Power Consumption

- Operating power: 120 µA typical (conditions: V_{DD} = 3V, x 3 boosting (VCI = V_{DD}), V0 = 7.6V, Internal power supply ON, display OFF and normal mode is selected)
- Standby power: 10 µA maximum (during power save[standby] mode)

Operating Temperatures

- Wide range of operating temperatures : -40 to 85°C

CMOS Process

Package Type

- Gold bumped chip

BLOCK DIAGRAM

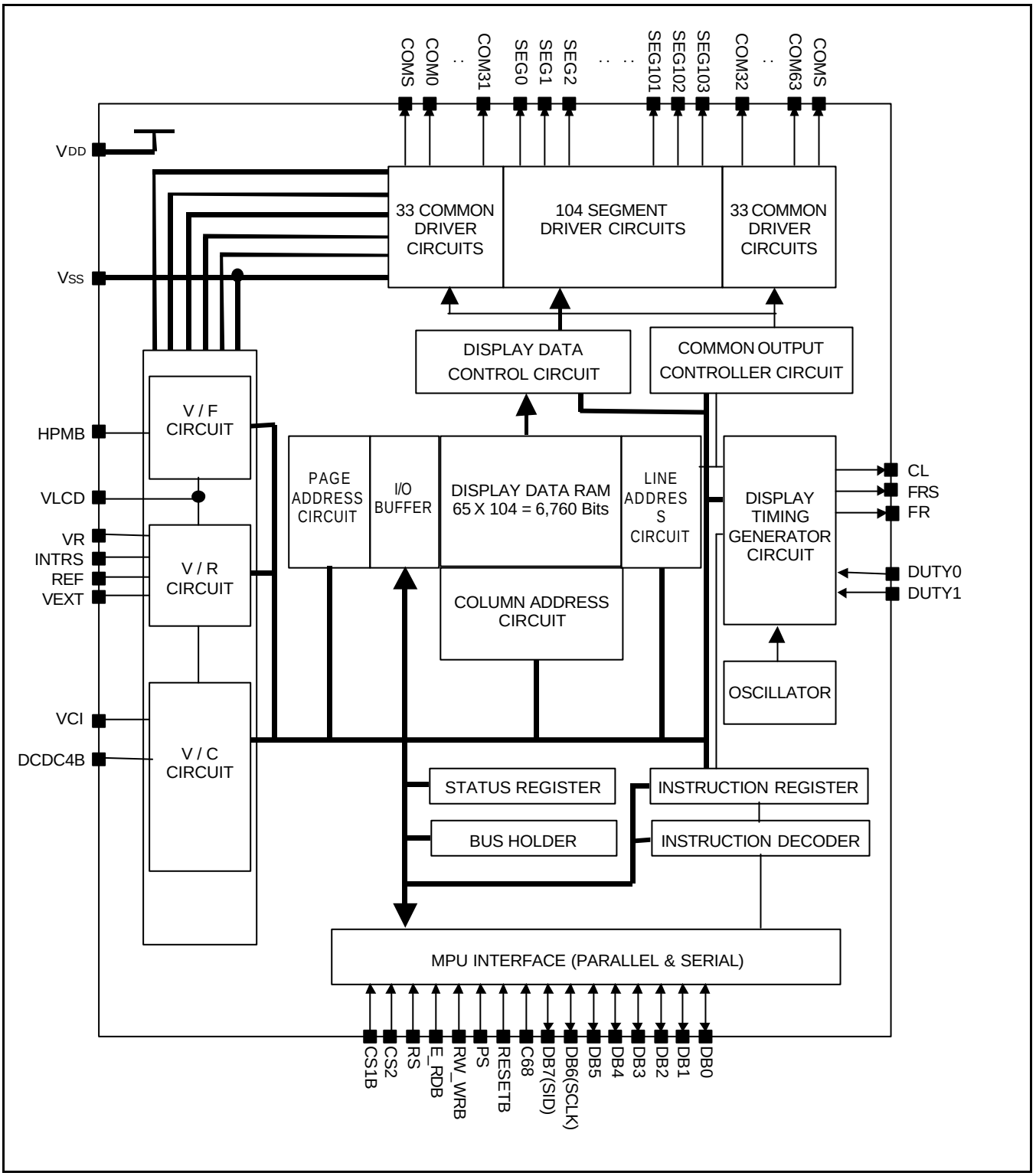


Figure 1. Block Diagram

PAD CONFIGURATION

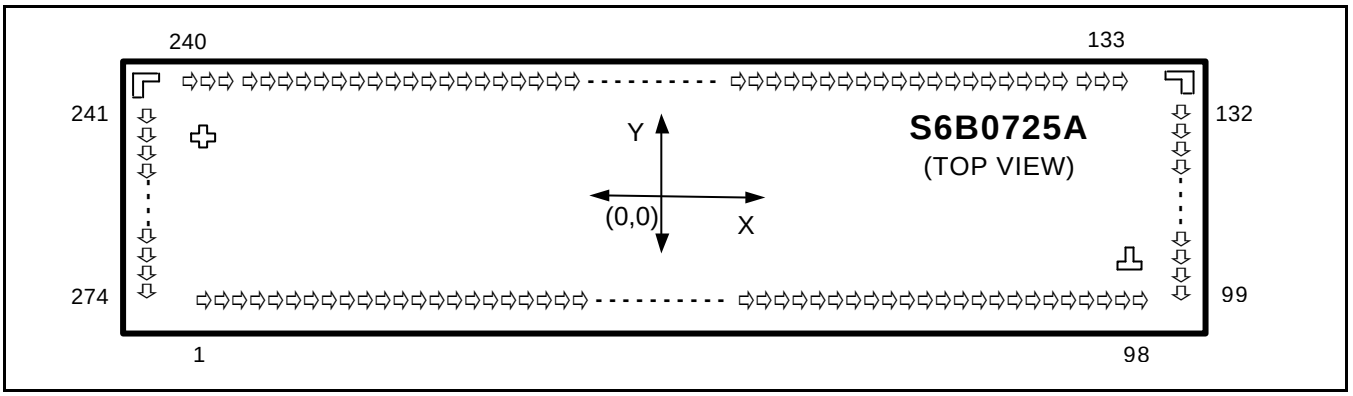
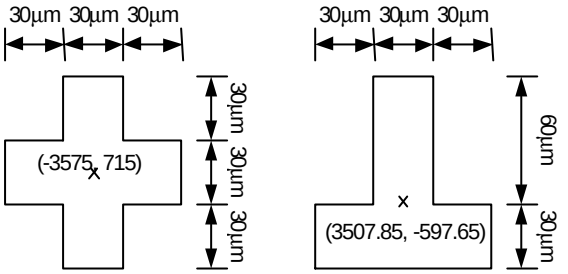


Figure 2. S6B0725A Chip Configuration

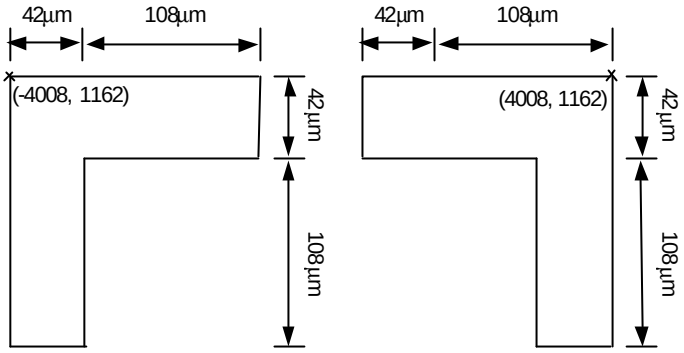
Table 1. S6B0725A Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	8220	2540	µm
Pad pitch	1 to 98	70		
	99 to 100	70		
	100 to 132	60		
	133 to 134	80		
	134 to 135	194		
	135 to 238	68		
	238 to 239	194		
	239 to 240	80		
	241 to 273	60		
	273 to 274	70		
Bumped pad size (Bottom)	1 to 98	42	92	
	99	102	52	
	100 to 132	102	32	
	133 to 134	52	102	
	135 to 238	32	102	
	239 to 240	52	102	
	241 to 273	102	32	
	274	102	52	
Bumped pad height	All pad	14 (Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate(with Gold Bump *)



* When designing COG pattern, ITO pattern must be prohibited on ILB Align Key, DUMMY pads, TEST pads. If ITO pattern is used for routing over these area, it can be happened pattern-short through bumped pattern on these area.

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	DUMMY1	-3390	-1155	51	VCI	110	-1155	101	COM30	3963	-930
2	FRS	-3320	-1155	52	VCI	180	-1155	102	COM29	3963	-870
3	FR	-3250	-1155	53	VCI	250	-1155	103	COM28	3963	-810
4	CL	-3180	-1155	54	VCI	320	-1155	104	COM27	3963	-750
5	TEST1	-3110	-1155	55	VCI	390	-1155	105	COM26	3963	-690
6	VDD	-3040	-1155	56	VCI	460	-1155	106	COM25	3963	-630
7	VDD	-2970	-1155	57	VCI	530	-1155	107	COM24	3963	-570
8	VDD	-2900	-1155	58	VDD	600	-1155	108	COM23	3963	-510
9	VDD	-2830	-1155	59	VEXT	670	-1155	109	COM22	3963	-450
10	VDD	-2760	-1155	60	VSS	740	-1155	110	COM21	3963	-390
11	VDD	-2690	-1155	61	REF	810	-1155	111	COM20	3963	-330
12	VDD	-2620	-1155	62	VDD	880	-1155	112	COM19	3963	-270
13	VDD	-2550	-1155	63	DCDC4B	950	-1155	113	COM18	3963	-210
14	VDD	-2480	-1155	64	VSS	1020	-1155	114	COM17	3963	-150
15	VDD	-2410	-1155	65	HPMB	1090	-1155	115	COM16	3963	-90
16	VDD	-2340	-1155	66	VDD	1160	-1155	116	COM15	3963	-30
17	VDD	-2270	-1155	67	INTRS	1230	-1155	117	COM14	3963	30
18	VDD	-2200	-1155	68	VSS	1300	-1155	118	COM13	3963	90
19	VDD	-2130	-1155	69	VSS	1370	-1155	119	COM12	3963	150
20	DB0	-2060	-1155	70	VSS	1440	-1155	120	COM11	3963	210
21	DB1	-1990	-1155	71	VSS	1510	-1155	121	COM10	3963	270
22	DB2	-1920	-1155	72	VSS	1580	-1155	122	COM9	3963	330
23	DB3	-1850	-1155	73	VSS	1650	-1155	123	COM8	3963	390
24	DB4	-1780	-1155	74	VSS	1720	-1155	124	COM7	3963	450
25	DB5	-1710	-1155	75	VSS	1790	-1155	125	COM6	3963	510
26	DB6	-1640	-1155	76	VSS	1860	-1155	126	COM5	3963	570
27	DB7	-1570	-1155	77	VSS	1930	-1155	127	COM4	3963	630
28	VSS	-1500	-1155	78	VR	2000	-1155	128	COM3	3963	690
29	TEST2	-1430	-1155	79	VSS	2070	-1155	129	COM2	3963	750
30	TEST3	-1360	-1155	80	TESTA0	2140	-1155	130	COM1	3963	810
31	VSS	-1290	-1155	81	TESTB0	2210	-1155	131	COM0	3963	870
32	RS	-1220	-1155	82	VSS	2280	-1155	132	COMS	3963	930
33	VDD	-1150	-1155	83	VLCD	2350	-1155	133	DUMMY4	3776	1117
34	DUTY0	-1080	-1155	84	VLCD	2420	-1155	134	DUMMY5	3696	1117
35	VSS	-1010	-1155	85	VLCD	2490	-1155	135	SEG0	3502	1117
36	DUTY1	-940	-1155	86	VLCD	2560	-1155	136	SEG1	3434	1117
37	VDD	-870	-1155	87	VLCD	2630	-1155	137	SEG2	3366	1117
38	PS	-800	-1155	88	VLCD	2700	-1155	138	SEG3	3298	1117
39	VSS	-730	-1155	89	TESTA1	2770	-1155	139	SEG4	3230	1117
40	C68	-660	-1155	90	TESTB1	2840	-1155	140	SEG5	3162	1117
41	VDD	-590	-1155	91	TESTA2	2910	-1155	141	SEG6	3094	1117
42	E_RDB	-520	-1155	92	TESTB2	2980	-1155	142	SEG7	3026	1117
43	RW_WRB	-450	-1155	93	TESTA3	3050	-1155	143	SEG8	2958	1117
44	VSS	-380	-1155	94	TESTB3	3120	-1155	144	SEG9	2890	1117
45	CS1B	-310	-1155	95	TESTA4	3190	-1155	145	SEG10	2822	1117
46	CS2	-240	-1155	96	TESTB4	3260	-1155	146	SEG11	2754	1117
47	VDD	-170	-1155	97	RESETB	3330	-1155	147	SEG12	2686	1117
48	VCI	-100	-1155	98	DUMMY2	3400	-1155	148	SEG13	2618	1117
49	VCI	-30	-1155	99	DUMMY3	3963	-1060	149	SEG14	2550	1117
50	VCI	40	-1155	100	COM31	3963	-990	150	SEG15	2482	1117

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
151	SEG16	2414	1117	201	SEG66	-986	1117	251	COM42	-3963	330
152	SEG17	2346	1117	202	SEG67	-1054	1117	252	COM43	-3963	270
153	SEG18	2278	1117	203	SEG68	-1122	1117	253	COM44	-3963	210
154	SEG19	2210	1117	204	SEG69	-1190	1117	254	COM45	-3963	150
155	SEG20	2142	1117	205	SEG70	-1258	1117	255	COM46	-3963	90
156	SEG21	2074	1117	206	SEG71	-1326	1117	256	COM47	-3963	30
157	SEG22	2006	1117	207	SEG72	-1394	1117	257	COM48	-3963	-30
158	SEG23	1938	1117	208	SEG73	-1462	1117	258	COM49	-3963	-90
159	SEG24	1870	1117	209	SEG74	-1530	1117	259	COM50	-3963	-150
160	SEG25	1802	1117	210	SEG75	-1598	1117	260	COM51	-3963	-210
161	SEG26	1734	1117	211	SEG76	-1666	1117	261	COM52	-3963	-270
162	SEG27	1666	1117	212	SEG77	-1734	1117	262	COM53	-3963	-330
163	SEG28	1598	1117	213	SEG78	-1802	1117	263	COM54	-3963	-390
164	SEG29	1530	1117	214	SEG79	-1870	1117	264	COM55	-3963	-450
165	SEG30	1462	1117	215	SEG80	-1938	1117	265	COM56	-3963	-510
166	SEG31	1394	1117	216	SEG81	-2006	1117	266	COM57	-3963	-570
167	SEG32	1326	1117	217	SEG82	-2074	1117	267	COM58	-3963	-630
168	SEG33	1258	1117	218	SEG83	-2142	1117	268	COM59	-3963	-690
169	SEG34	1190	1117	219	SEG84	-2210	1117	269	COM60	-3963	-750
170	SEG35	1122	1117	220	SEG85	-2278	1117	270	COM61	-3963	-810
171	SEG36	1054	1117	221	SEG86	-2346	1117	271	COM62	-3963	-870
172	SEG37	986	1117	222	SEG87	-2414	1117	272	COM63	-3963	-930
173	SEG38	918	1117	223	SEG88	-2482	1117	273	COMS	-3963	-990
174	SEG39	850	1117	224	SEG89	-2550	1117	274	DUMMY8	-3963	-1060
175	SEG40	782	1117	225	SEG90	-2618	1117				
176	SEG41	714	1117	226	SEG91	-2686	1117				
177	SEG42	646	1117	227	SEG92	-2754	1117				
178	SEG43	578	1117	228	SEG93	-2822	1117				
179	SEG44	510	1117	229	SEG94	-2890	1117				
180	SEG45	442	1117	230	SEG95	-2958	1117				
181	SEG46	374	1117	231	SEG96	-3026	1117				
182	SEG47	306	1117	232	SEG97	-3094	1117				
183	SEG48	238	1117	233	SEG98	-3162	1117				
184	SEG49	170	1117	234	SEG99	-3230	1117				
185	SEG50	102	1117	235	SEG100	-3298	1117				
186	SEG51	34	1117	236	SEG101	-3366	1117				
187	SEG52	-34	1117	237	SEG102	-3434	1117				
188	SEG53	-102	1117	238	SEG103	-3502	1117				
189	SEG54	-170	1117	239	DUMMY6	-3696	1117				
190	SEG55	-238	1117	240	DUMMY7	-3776	1117				
191	SEG56	-306	1117	241	COM32	-3963	930				
192	SEG57	-374	1117	242	COM33	-3963	870				
193	SEG58	-442	1117	243	COM34	-3963	810				
194	SEG59	-510	1117	244	COM35	-3963	750				
195	SEG60	-578	1117	245	COM36	-3963	690				
196	SEG61	-646	1117	246	COM37	-3963	630				
197	SEG62	-714	1117	247	COM38	-3963	570				
198	SEG63	-782	1117	248	COM39	-3963	510				
199	SEG64	-850	1117	249	COM40	-3963	450				
200	SEG65	-918	1117	250	COM41	-3963	390				

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pins Description

Name	I/O	Description
VDD	Supply	Power supply
VSS	Supply	Ground

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pins Description

Name	I/O	Description
VLCD	O	LCD power supply output pin Connect this pin to V_{SS} through capacitor.(Capacitor is greater than 1μF)
DCDC4B	I	4 times boosting circuit enable input pin – DCDC4B = "H": 3 times boosting – DCDC4B = "L": 4 times boosting
VR	I	VLCD voltage adjustment pin It is valid only when internal voltage regulator resistors are not used (INTRS = "L").
VCI	I	This is the reference voltage for the voltage converter circuit for the LCD driving. Whether internal voltage converter use or not use, this pin should be fixed. The voltage should have the following range: 2.4V ≤ VCI ≤ 3.6V
VEXT	I	This is the external-input reference voltage (V_{REF}) for the internal voltage regulator. It is valid only when external V_{REF} is used (REF = "L"). When using internal V_{REF}, this pin is Open
REF	I	Select the external V_{REF} voltage via VEXT pin – REF = "L": using the external V_{REF} – REF = "H": using the internal V_{REF}

SYSTEM CONTROL

Table 5. System Control Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>CL</td><td>O</td><td colspan="3">Display clock output pin</td></tr>
<tr><td>FRS</td><td>O</td><td colspan="3">Static driver segment output pin
This pin is used together with the FR pin.</td></tr>
<tr><td>FR</td><td>O</td><td colspan="3">Static driver common output pin
This pin is used together with the FRS pin.</td></tr>
<tr><td>INTRS</td><td>I</td><td colspan="3">Internal resistor select pin
This pin selects the resistors for adjusting VLCD voltage level.
– INTRS = “H”: the internal resistors are used
– INTRS = “L”: the external resistors are used
VLCD voltage is controlled by VR pin and external resistive divider.
(* refer to page 28)</td></tr>
<tr><td rowspan="7">DUTY0
DUTY1</td><td rowspan="7">I</td><td colspan="3">The LCD driver duty ratio depends on the following table.</td></tr>
<tr><td>DUTY1</td><td>DUTY0</td><td>Duty ratio</td></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L</td><td>1/55</td></tr>
<tr><td>H</td><td>H</td><td>1/65</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>HPMB</td><td>I</td><td colspan="3">Power control pin of the power supply circuits for LCD driver.
– HPMB = “H”: normal mode
– HPMB = “L”: high power mode</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Chip select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RDB
RW_WRB</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table></td></tr>
<tr><td>*Note: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RDB and RW_WRB must be fixed to either “H” or “L”.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor interface select input pin
– PS = “H”, C68 = "H": 6800-series parallel MPU interface
– PS = “H”, C68 = "L": 8080-series parallel MPU interface
– PS = “L”, C68 = "H": 4 pin-SPI serial MPU interface
– PS = “L”, C68 = "L": 3 pin-SPI serial MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data
* This pin must be fixed to either “H” or “L” in case of 3 pin-SPI serial MPU interface mode</td></tr>
<tr><td rowspan="3">RW_WRB</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><td>C68</td><td>MPU Type</td><td>RW_WRB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = “H”: read
– RW = “L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td></td></tr>
<tr><td></td></tr>
</table>

Table 6. Microprocessor Interface Pins Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RDB</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>E_RDB</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L"),
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>TESTs</td><td>I/O</td><td colspan="4">These are pins for chip test.
They are set to open.</td></tr>
</table>

NOTE: DUMMYs – These pins should be opened (floated).

LCD DRIVER OUTPUTS

Table 7. LCD Driver Output Pins Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG103</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">FR</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>VLCD</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>VLCD</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM63</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and FR signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>FR</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">VSS</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">VLCD</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0725A can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B0725A has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

Table 8. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	H	4 pin-SPI serial MPU mode
				L	3 pin-SPI serial MPU mode

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 9. The type of data transfer is determined by signals at RS, E_RDB and RW_WRB as shown in table 10.

Table 9. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RDB (E)	RW_WRB (RW)	E_RDB (/RD)	RW_WRB (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

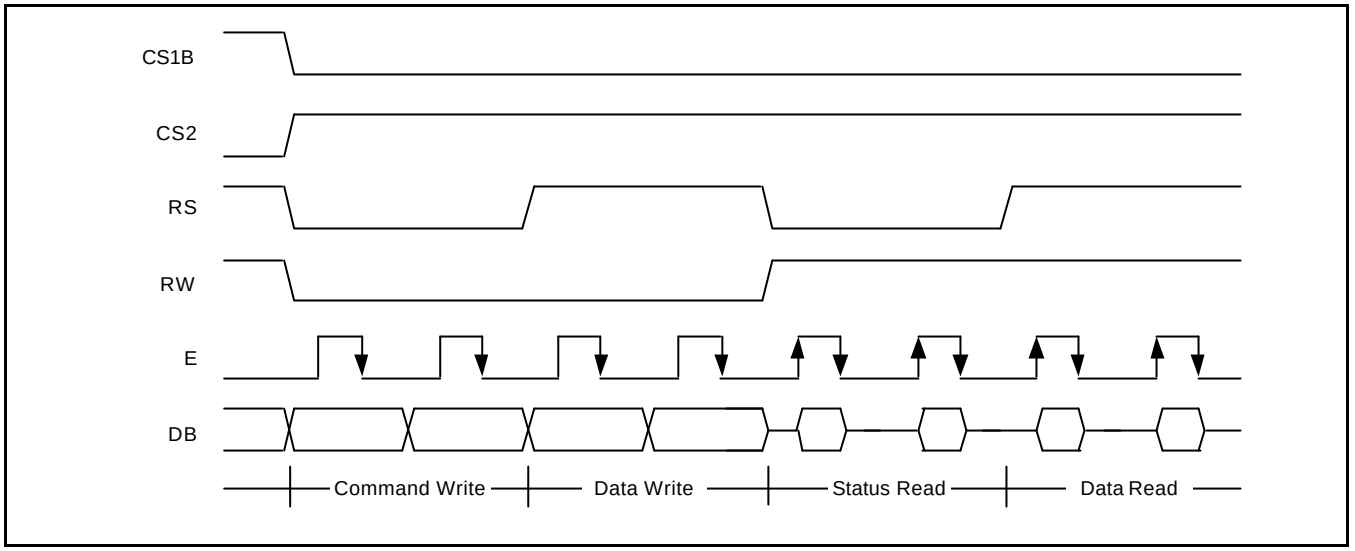


Figure 2-1. 6800-Series MPU Interface protocol (PS="H", C68="H")

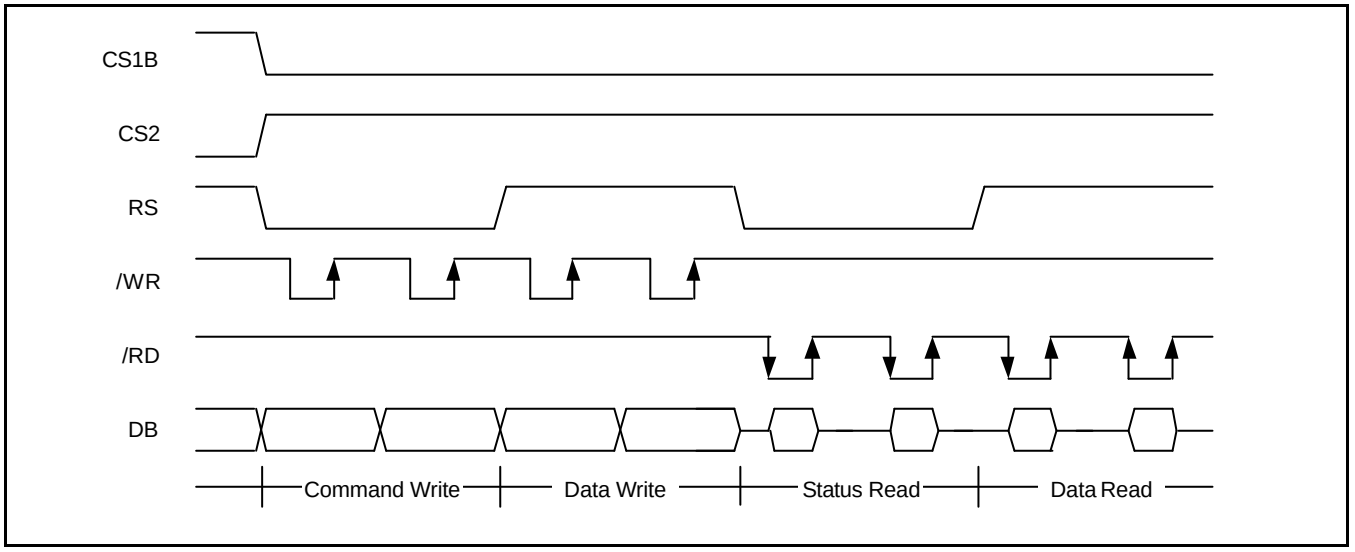


Figure 2-2. 8080-Series MPU Interface Protocol (PS="H", C68="L")

Serial Interface (PS = "L")

When the S6B0725A is active (CS1B=" L", CS2=" H'), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (RS) Pin, based on the setting of C68. When the RS pin is used (PS = " H'), data is display data when RS is high, and command data when RS is low. When RS is not used (C68 = " L"), the LCD Driver will receive command from MPU by default. If messages on the data pin are data rather than command, MPU should send Data Direction command (10000000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sending, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.
Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

The serial interface type is selected by setting C68 as shown in table 11.

Table 11. Parallel / Serial Interface Mode

Serial Mode	PS	C68	Chip Select	Register Select	Serial Data / Clock input
4 pin SPI serial mode	L	H	CS1B, CS2	RS pin	DB7 / DB6
3 pin SPI serial mode	L	L	CS1B, CS2	Software	DB7 / DB6

4 Pin SPI Serial Interface (PS = "L", C68 = "H")

In 4-pin serial interface mode, RS pin is used for indicating whether serial data input is display or instruction data. Data is display data when RS is high and instruction data when RS is low.

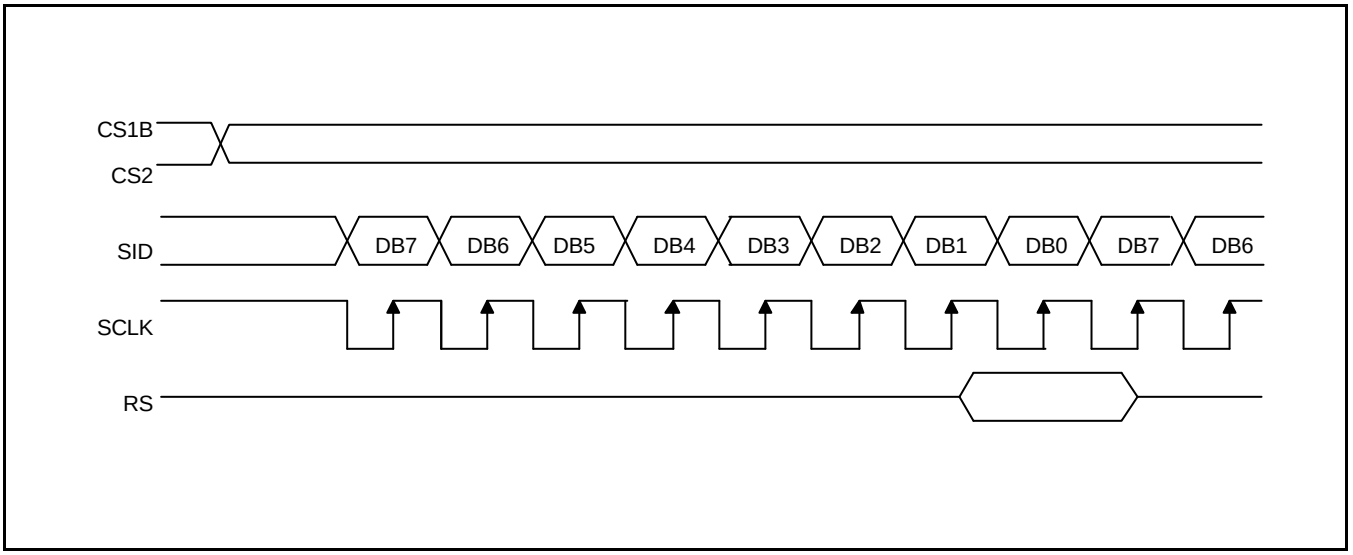


Figure 3. 4 Pin SPI serial Interface Timing (RS used)

3 Pin-SPI Interface (PS = "L", C68 = "L")

In 3-Pin SPI Interface mode, the pre-defined instruction called Display Data Length, is used to indicate whether serial data input is display or instruction data instead of RS pin. The data is handled as instruction data until the Display Data Length instruction is issued. This Display Data Length instruction consists of two bytes instruction. The first byte instruction enables the next instruction to be valid, and the data of the second byte indicates that a specified number of display data bytes (1 to 256) are to be transmitted. The next byte after the display data string is handled as instruction data. For details, refers to figure 4.

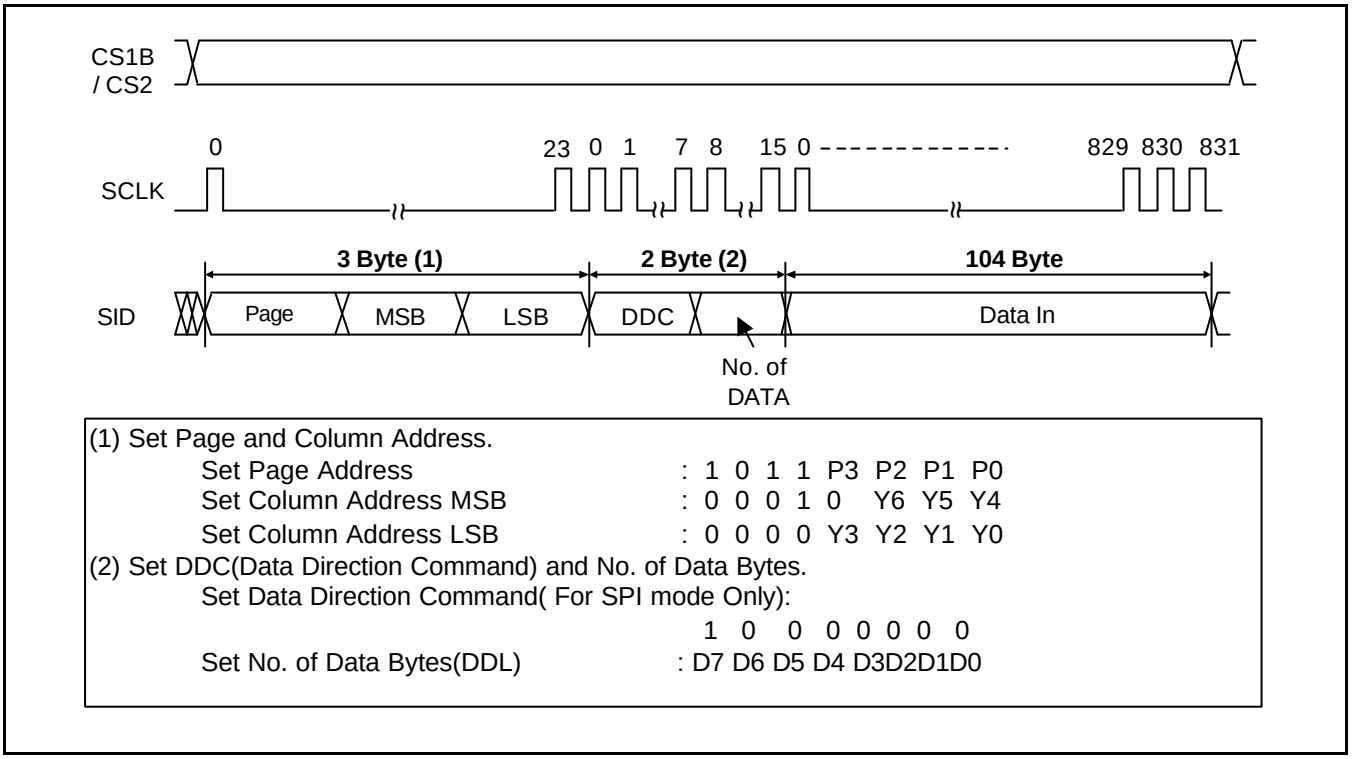


Figure 4. 3 Pin SPI Timing (RS is not used)

This command is used in 3-Pin SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data. New data will be transferred serially with most significant bit first.

*NOTES:

- In spite of transmission of data, if CS1B will be disable, state terminates abnormally. Next state is initialized.
- The number of writing display data = DDL register value + 1

Busy Flag

The busy flag indicates whether the S6B0725A is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0725A uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 5. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 6. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

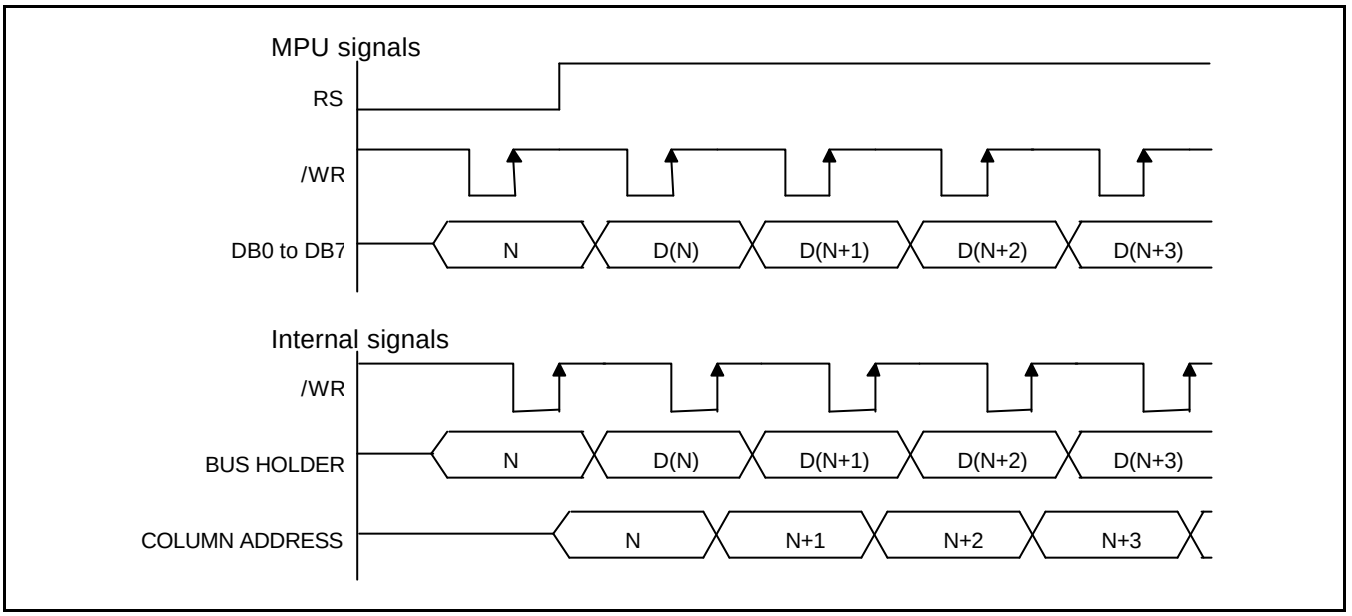


Figure 5. Write Timing

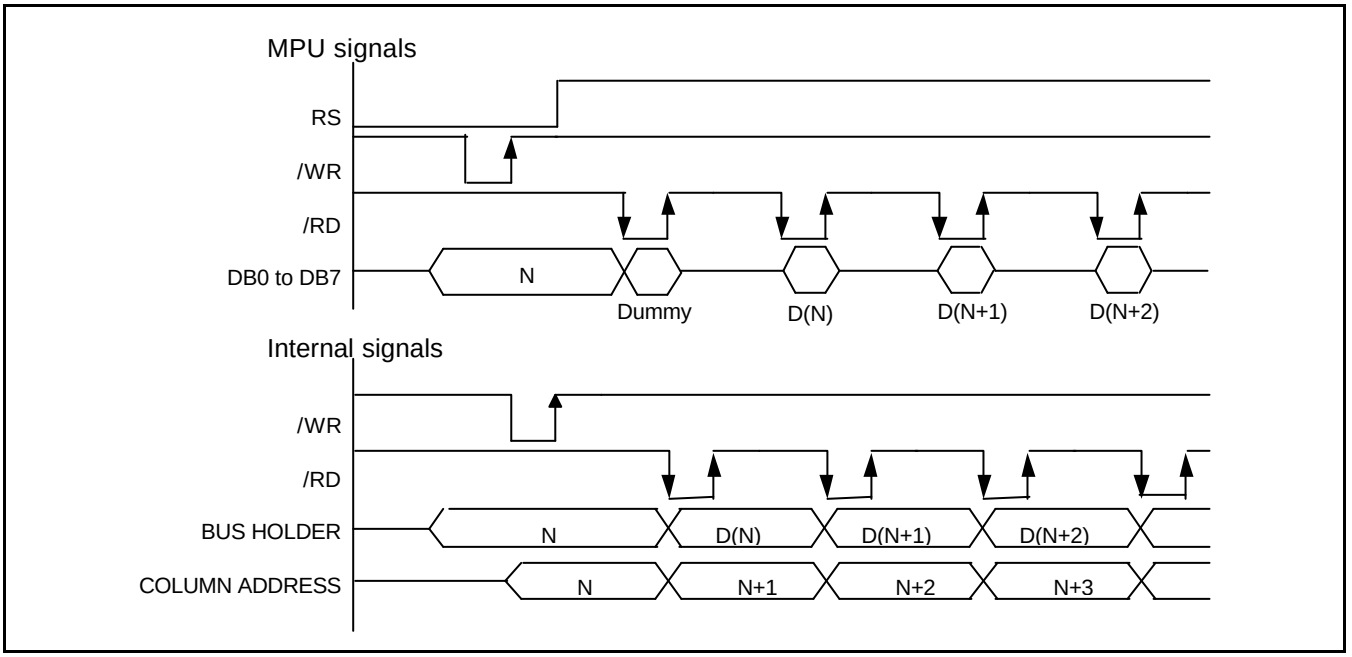


Figure 6. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 104-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 7. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

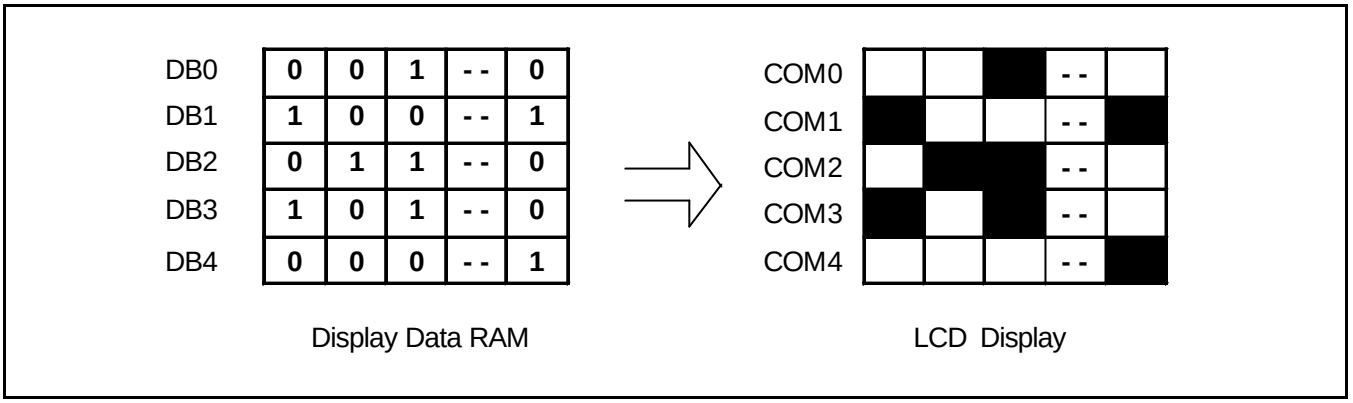


Figure 7. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a page address to Display Data RAM shown in figure 9. It incorporates 4-bit page address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 9. It incorporates 6-bit line address register changed by only the Initial Display Line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 104-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU cannot access line address of icons.

Column Address Circuit

Column address circuit has a 7-bit preset counter that provides column address to the Display Data RAM as shown in figure 9. When Set Column Address MSB / LSB instruction is issued, 7-bit [Y6:Y0] is updated. And, since this address is increased by 1 each a Read or Write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 67H. It is unlocked if a column address is set again by set Column Address MSB/LSB instruction. And the column address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 8.

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	... ...	SEG 100	SEG 101	SEG 102	SEG 103
Column address [Y7:Y0]	00H	01H	02H	03H	... ...	64H	65H	66H	67H
Display data	1	0	1	0		1	1	0	0
LCD panel display (ADC = 0)	■		■		... ...	■	■		
LCD panel display (ADC = 1)			■	■	... ...		■		■

Figure 8. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

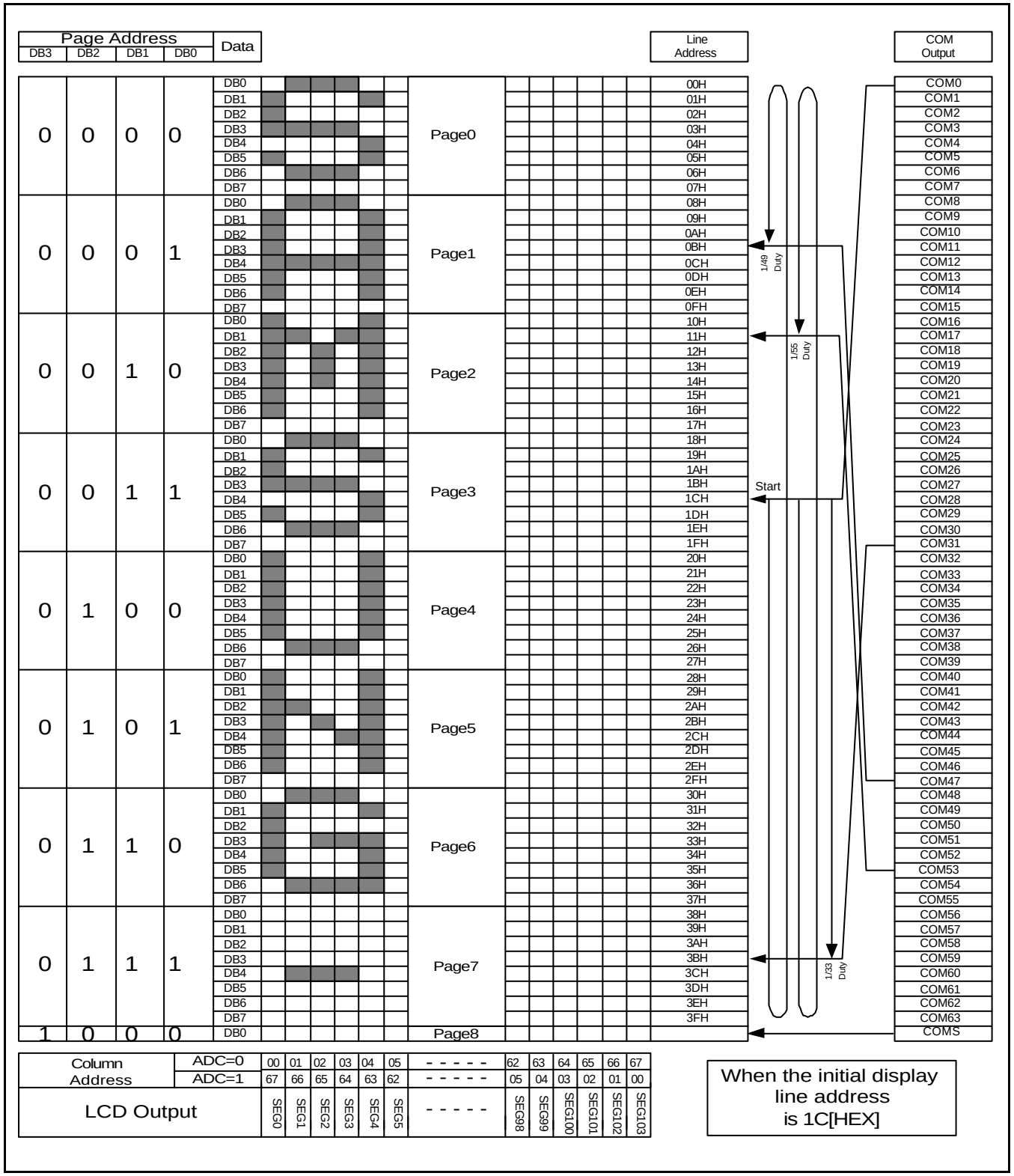


Figure 9. Display Data RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 104-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, FR is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 10.

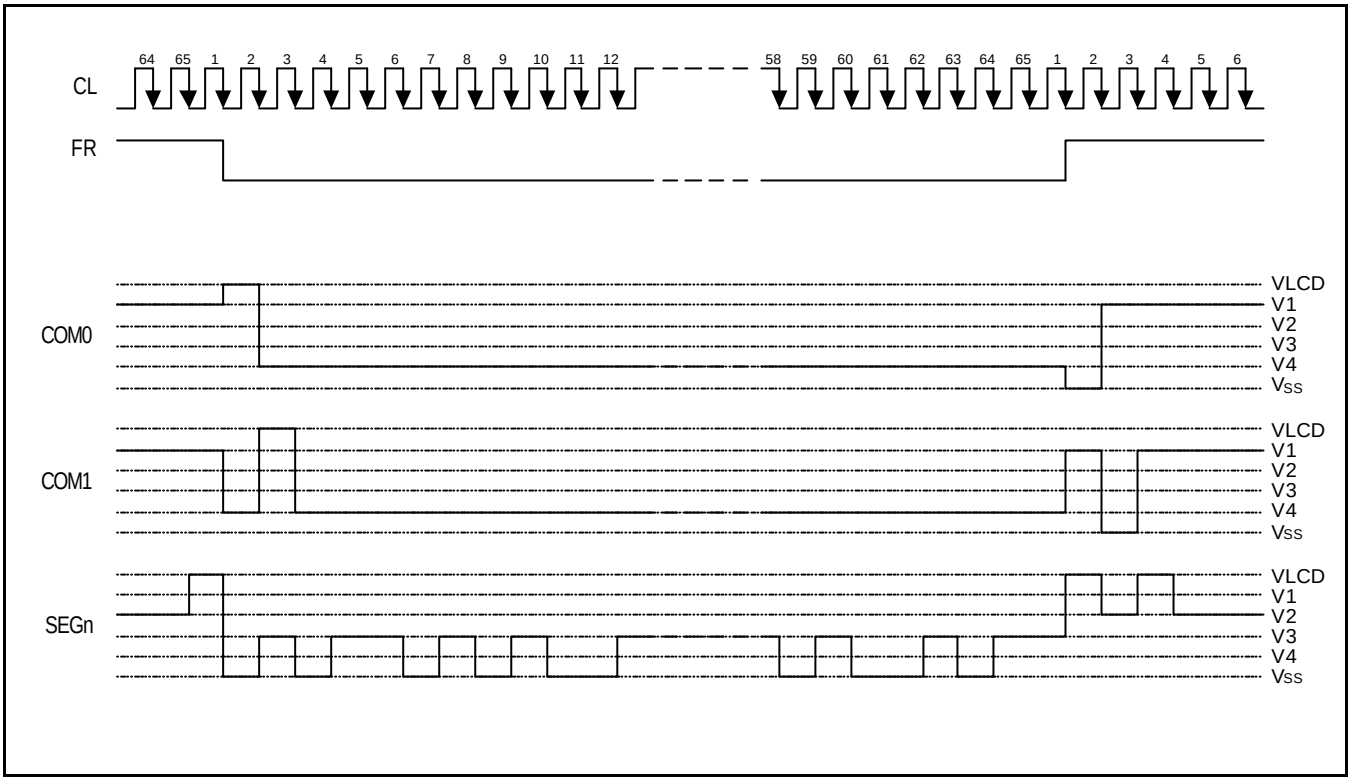


Figure 10. 2-frame AC Driving Waveform (Duty Ratio = 1/65)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 12. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins							
		COM [0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM [48:63]	COMS
1/33	0	COM[0:15]	*NC					COM[16:31]	COMS
	1	COM[31:16]	*NC					COM[15:0]	
1/49	0	COM[0:23]		*NC			COM[24:47]		COMS
	1	COM[47:24]		*NC			COM[23:0]		
1/55	0	COM[0:26]			*NC	COM[27:53]			COMS
	1	COM[53:27]			*NC	COM[26:0]			
1/65	0	COM[0:63]							COMS
	1	COM[63:0]							

*NC: No Connection

LCD DRIVER CIRCUITS

This driver circuit is configured by 66-channel (including 2 COMS channels) common driver and 104-channel segment driver. This LCD panel driver voltage depends on the combination of display data and FR signal.

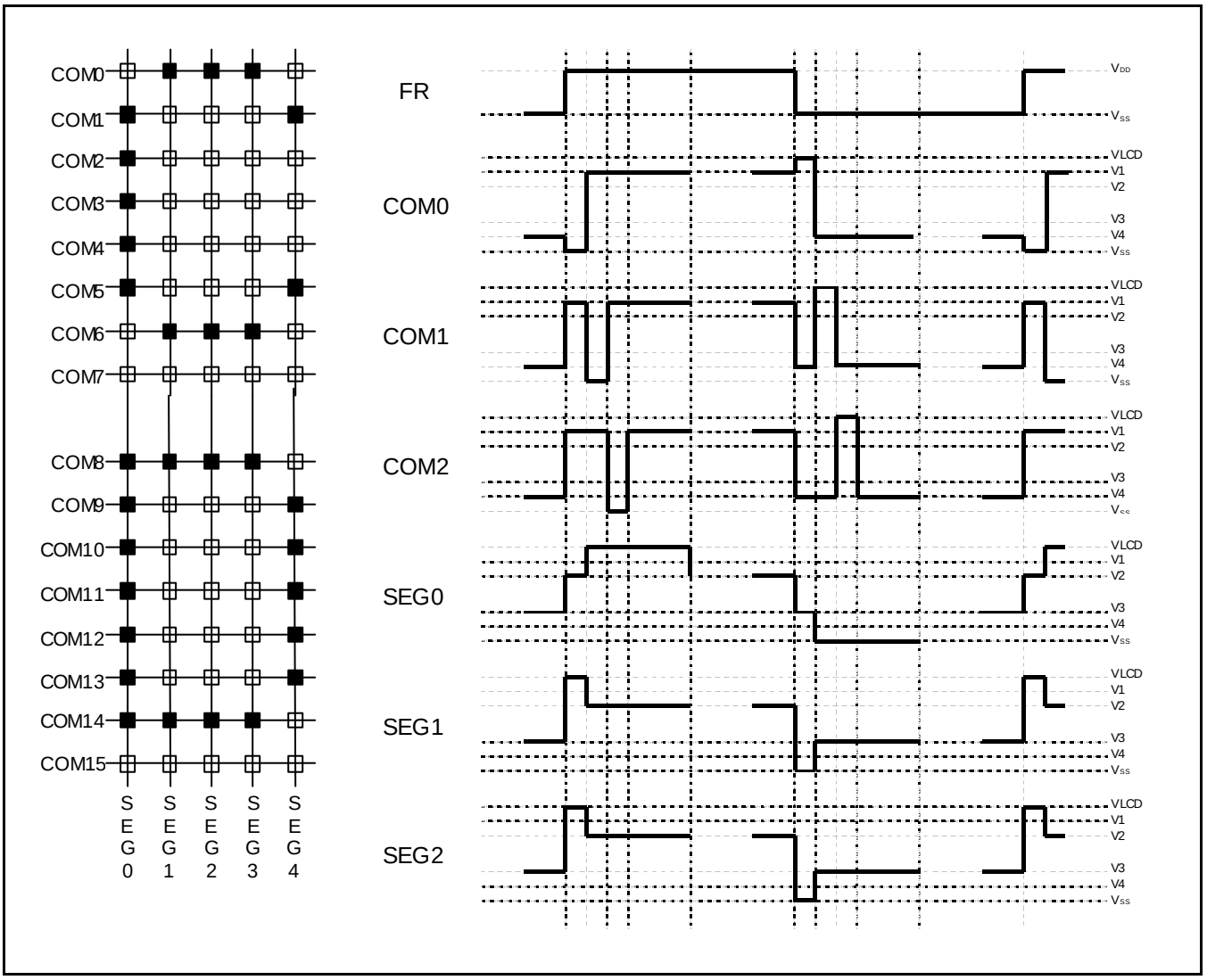


Figure 11. Segment and Common Timing

POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description".

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and VSS to 3 or 4 times toward positive side.

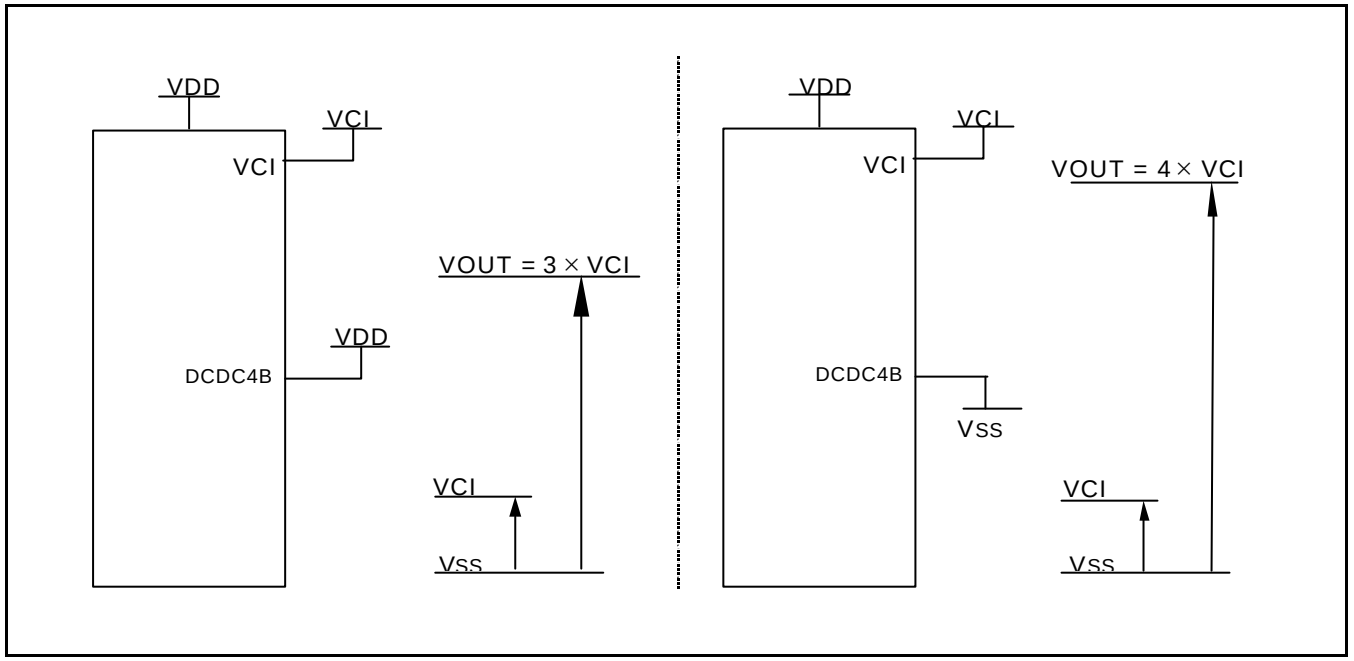


Figure 12. Three Times Boosting Circuit **Figure 13. Four Times Boosting Circuit**

* The VCI voltage range must be set so that the VOUT (Voltage converter output) does not exceed the absolute maximum rating value

Voltage Regulator Circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, VLCD, by adjusting resistors, Ra and Rb, within the range of |VLCD| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 14, it is necessary to be applied internally.

For the Eq. 1, we determine VLCD by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in table 13.

$$V_{LCD} = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 13. V_{REF} Voltage at Ta = 25 °C

REF	Temp. coefficient	V_{REF} [V]
H	-0.05% / °C	2.1
L	External input	VEXT

Table 14. Electronic Contrast Control Register (64 Steps)

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)	VLCD	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

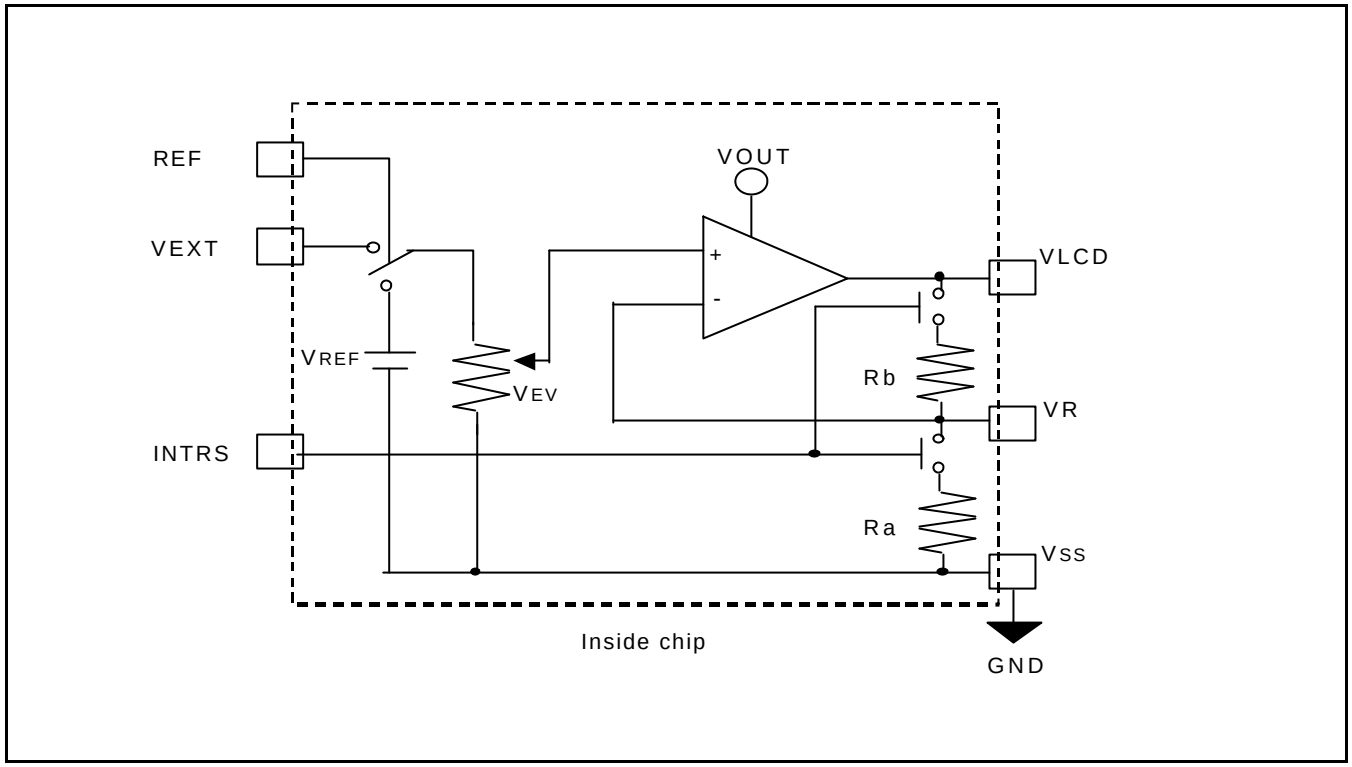


Figure 14. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between VLCD and VR. We determine VLCD by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 15. Internal Rb / Ra ratio depending on 3-bit data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	3.0	3.5	4.0	4.5	5.0	5.5	Not available	Not available

The following figure shows VLCD voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

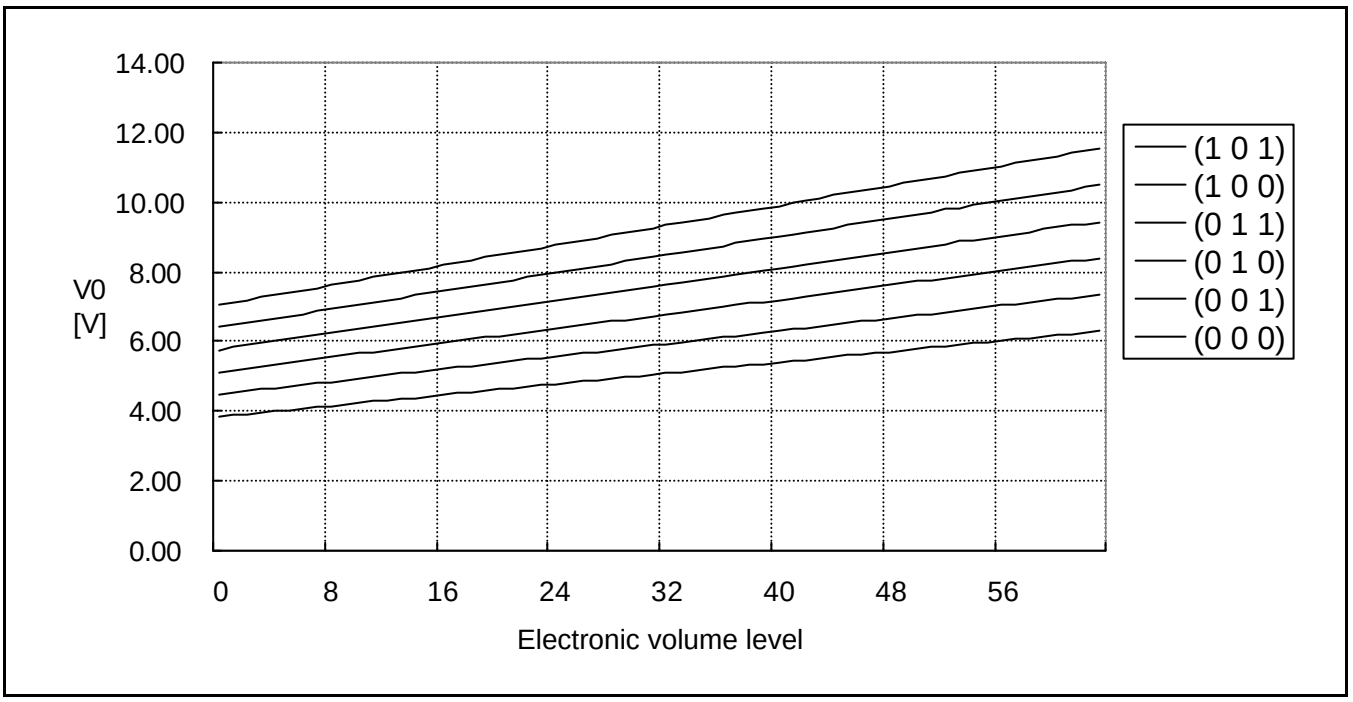


Figure 15. Electronic Volume Level

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between VLCD and VR.

Example: For the following requirements

1. LCD driver voltage, VLCD = 6V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$6 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (\textbf{Eq. 3})}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 \cong 1.698 \quad [V] \text{ ------ (\textbf{Eq. 4})}$$

From requirement 3.

$$\frac{6}{Ra + Rb} = 1 \ [uA] \quad \text{------ (\textbf{Eq. 5})}$$

From equations Eq. 3, 4 and 5

$Ra \cong 1.698$ [MΩ]

$Rb \cong 4.302$ [MΩ]

The following table shows the range of VLCD depending on the above requirements.

Table 16. VLCD Depending on Electronic Volume Level

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
VLCD	4.53	.....	6.00	.....	7.42

Voltage Follower Circuits

VLCD voltage is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 17. The Relationship between V1 to V4 Level and Duty Ratio

Duty ratio	DUTY1	DUTY0	LCD bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) VLCD	(3/5) VLCD	(2/5) VLCD	(1/5) VLCD
			1/6	(5/6) VLCD	(4/6) VLCD	(2/6) VLCD	(1/6) VLCD
1/49	L	H	1/6	(5/6) VLCD	(4/6) VLCD	(2/6) VLCD	(1/6) VLCD
			1/8	(7/8) VLCD	(6/8) VLCD	(2/8) VLCD	(1/8) VLCD
1/55	H	L	1/6	(5/6) VLCD	(4/6) VLCD	(2/6) VLCD	(1/6) VLCD
			1/8	(7/8) VLCD	(6/8) VLCD	(2/8) VLCD	(1/8) VLCD
1/65	H	H	1/7	(6/7) VLCD	(5/7) VLCD	(2/7) VLCD	(1/7) VLCD
			1/9	(8/9) VLCD	(7/9) VLCD	(2/9) VLCD	(1/9) VLCD

High Power Mode

The power supply circuit equipped in the S6B0725A for LCD drive has very low power consumption (in normal mode: HPMB = "H"). If use for LCD panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the HPMB pin to "L" (high power mode) can improve the quality of the display.

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", the initialized driver has following states.

Display ON / OFF: OFF
Entire display ON / OFF: OFF (normal)
ADC select: OFF (normal)
Reverse display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
Serial interface internal register data clear
LCD bias ratio: 1/9 (1/65 duty), 1/8 (1/55 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
On-chip oscillator OFF
Power save release
Read-modify-write: OFF
SHL select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (0, 1, 1)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

When RESET instruction is issued, the initialized driver has following states.

Read-modify-write: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (0, 1, 1)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

While RESETB is "L" or Reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don' t care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	×	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into DDRAM
Read display data	1	1	Read data								Read data from DDRAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG0→SEG103) When ADC = 1: reverse direction (SEG103→SEG0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/ entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM0→COM63) When SHL = 1: reverse direction (COM63→COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Set Data Direction & Display Data Length (DDL)	x	x	1	0	0	0	0	0	0	0	2-byte Instruction to specify the number of data bytes (SPI Mode)
	x	x	D7	D6	D5	D4	D3	D2	D1	D0	
Power save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON

Table 18. Instruction Table (Continued)

× : Don' t care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
NOP	0	0	1	1	1	0	0	0	1	1	*Non-Operation command*
Test instruction_1	0	0	1	1	1	1	×	×	×	×	*Don' t use this instruction*
Test instruction_2	0	0	1	0	0	1	×	×	×	×	*Don' t use this instruction*

DISPLAY ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

INITIAL DISPLAY LINE

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

SET PAGE ADDRESS

Sets the page address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the display RAM to write or read display data. Changing the page address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

SET COLUMN ADDRESS

Sets the column address of display RAM from the microprocessor into the column address register. Along with the column address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	x	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	1	1	0	102
1	1	0	0	1	1	1	103

READ STATUS

Indicates the internal status of the S6B0725A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON / OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG103 → SEG0), 1: normal direction (SEG0 → SEG103)
ON / OFF	Indicates display ON / OFF status. 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset

WRITE DISPLAY DATA

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

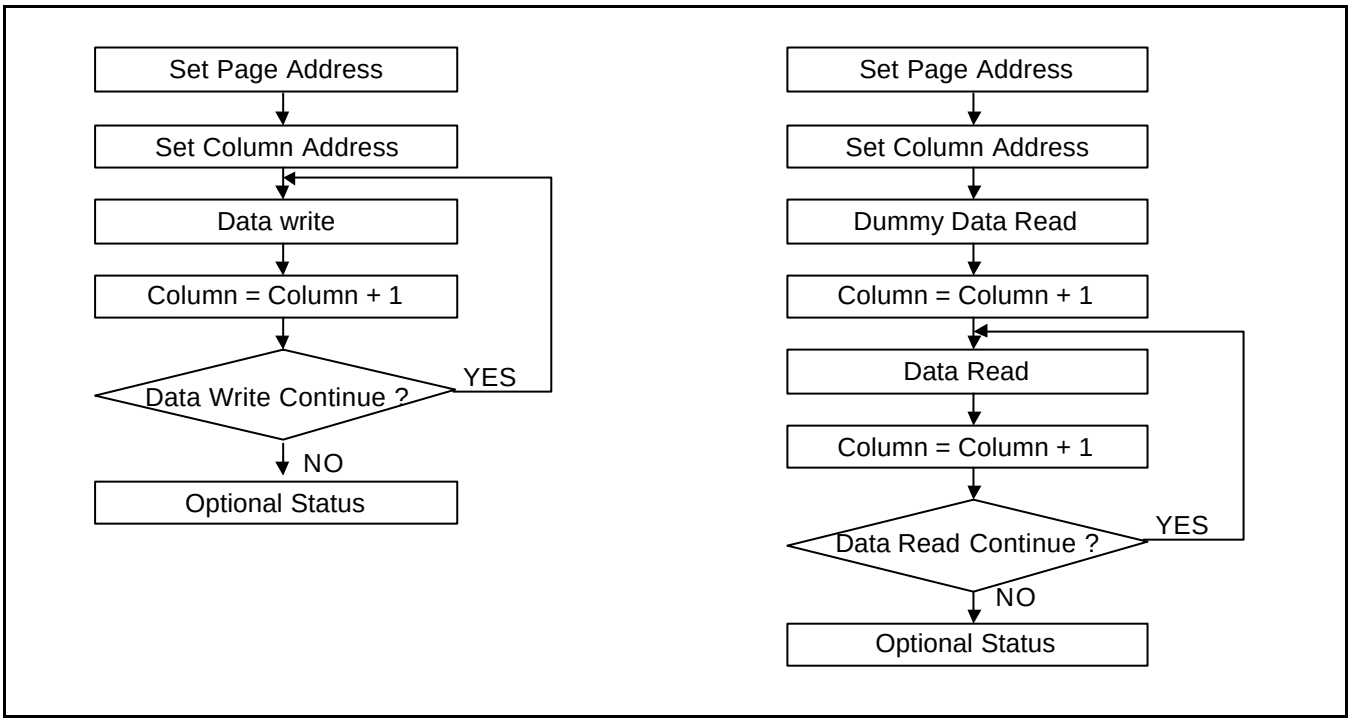


Figure 16. Sequence for Writing Display Data **Figure 17. Sequence for Reading Display Data**

Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

ADC SELECT (SEGMENT DRIVER DIRECTION SELECT)

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG103)
ADC = 1: reverse direction (SEG103 → SEG0)

REVERSE DISPLAY ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

ENTIRE DISPLAY ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display On/Off instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

SELECT LCD BIAS

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY1	DUTY0	LCD bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

SET MODIFY-READ

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

RESET MODIFY-READ

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

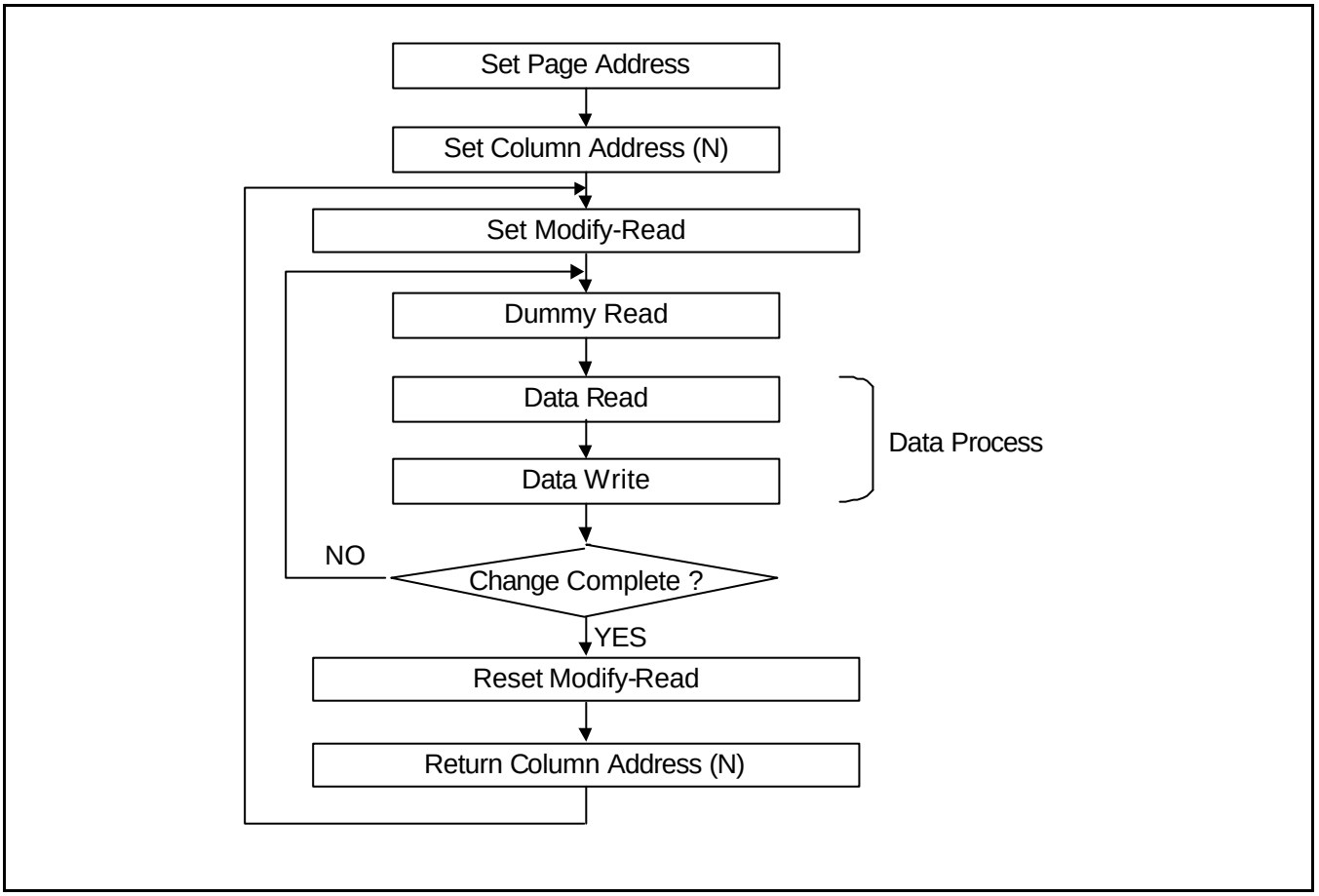


Figure 18. Sequence for Cursor Display

RESET

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL SELECT (COMMON OUTPUT MODE SELECT)

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don' t care

SHL = 0: normal direction (COM0 → COM63)
SHL = 1: reverse direction (COM63 → COM0)

POWER CONTROL

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

REGULATOR RESISTOR SELECT

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the **Table 15**.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5 (default)
1	0	0	5.0
1	0	1	5.5
1	1	0	Not available
1	1	1	Not available

REFERENCE VOLTAGE SELECT

Consists of 2-byte instruction. The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62		
1	1	1	1	1	1	63	Maximum	High

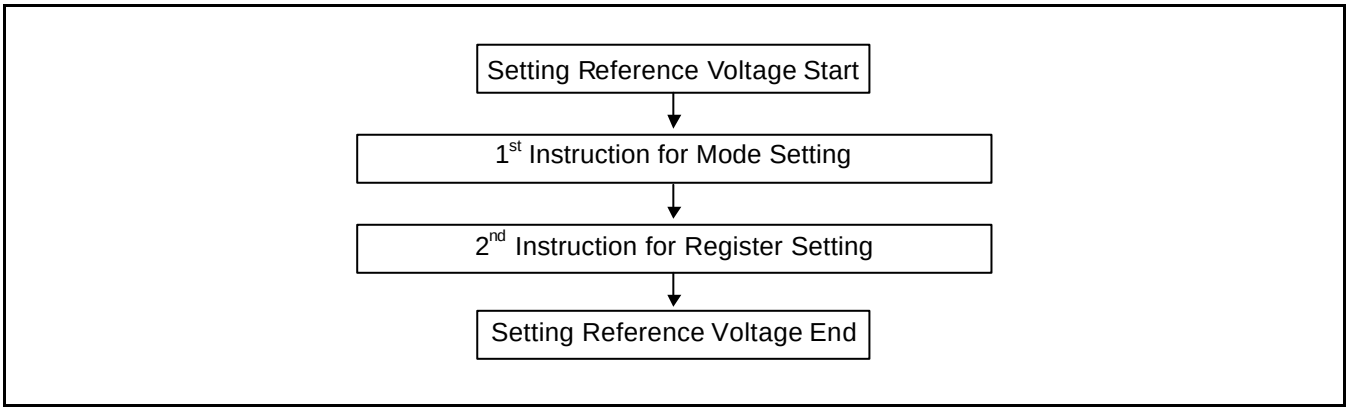


Figure 19. Sequence for Setting the Reference Voltage

SET STATIC INDICATOR STATE

Consists of two bytes instruction. The first byte instruction (Set Static Indicator Mode) enables the second byte instruction (Set Static Indicator Register) to be valid. The first byte sets the static indicator on/off. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

SET DATA DIRECTION & DISPLAY DATA LENGTH (3-PIN SPI MODE)

Consists of two bytes instruction.
This command is used in 3-Pin SPI mode only (PS = " L" and C68 = " L"). It will be two continuous commands, the first byte control the data direction (write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When RS is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

The 1st Instruction: Set Data Direction (Only Write Mode)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	0	0	0	0	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOP

Non-Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

TEST INSTRUCTION (TEST INSTRUCTION_1 & TEST INSTRUCTION_2)

These are the instruction for IC chip testing. Please do not use it. If the test instruction is used by accident, it can be cleared by applying " 0" signal to the RESETB input pin or the reset instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×
0	0	1	0	0	1	×	×	×	×

POWER SAVE (COMPOUND INSRTUCTION)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B0725A enters the power save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one mode of sleep and standby mode. When Static Indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power save mode is released by the entire display OFF instruction.

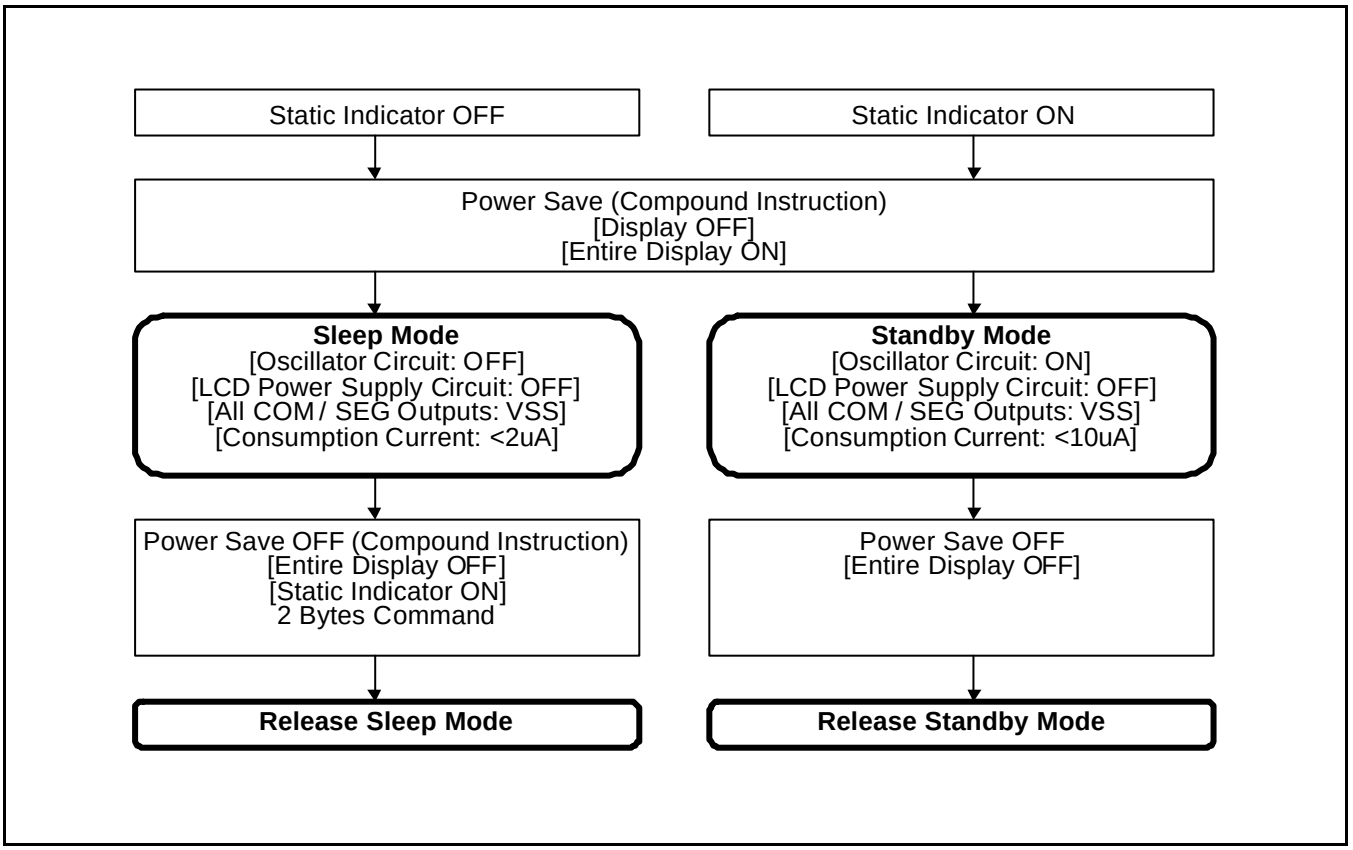


Figure 20. Power Save (Compound Instruction)

– Sleep Mode

This stops all operations in the LCD display system, and as long as there are no access from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

a. The oscillator circuit and the LCD power supply circuit are halted.
b. All liquid crystal drive circuits are halted, and the segment and common outputs go to the V_{SS} level.

– Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive.
The internal modes are in the following states during standby mode.

a. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
b. The duty drive system liquid crystal drive circuits are halted and the segment and common outputs go to the V_{SS} level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.

REFERENTIAL INSTRUCTION SETUP FLOW (1)

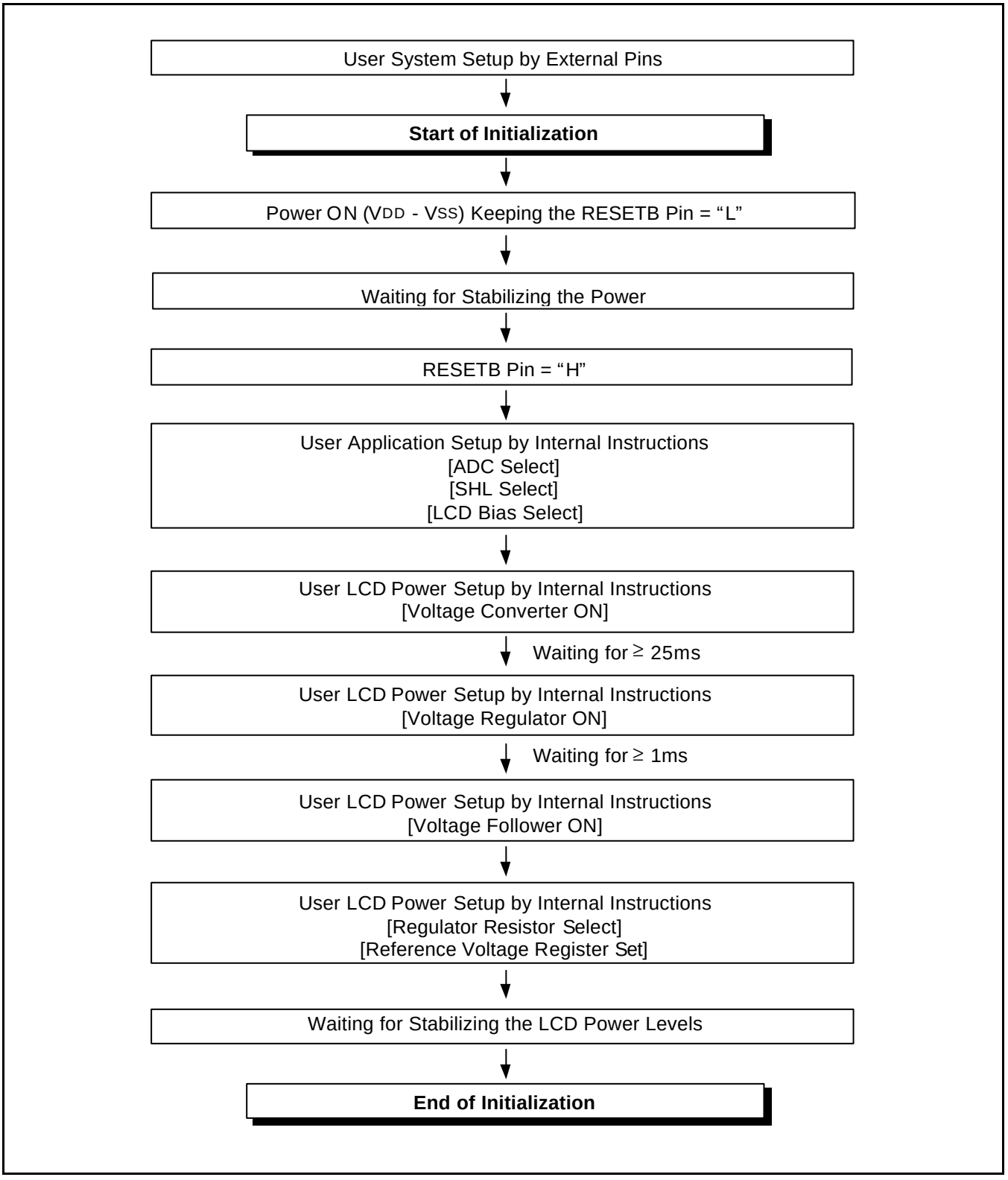


Figure 21. Initializing with the Built-in Power Supply Circuits

REFERENTIAL INSTRUCTION SETUP FLOW (2)

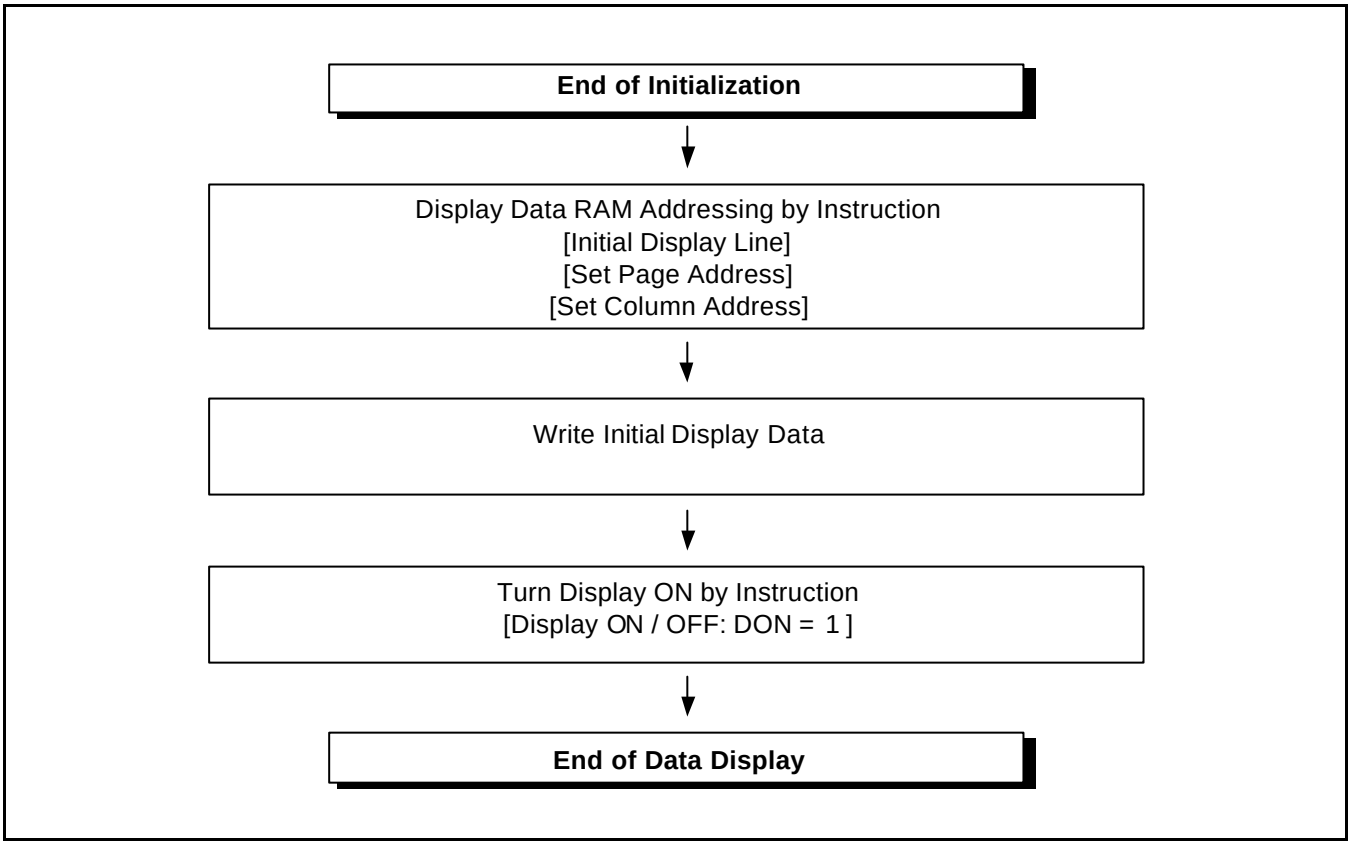


Figure 22. Data Displaying

REFERENTIAL INSTRUCTION SETUP FLOW (3)

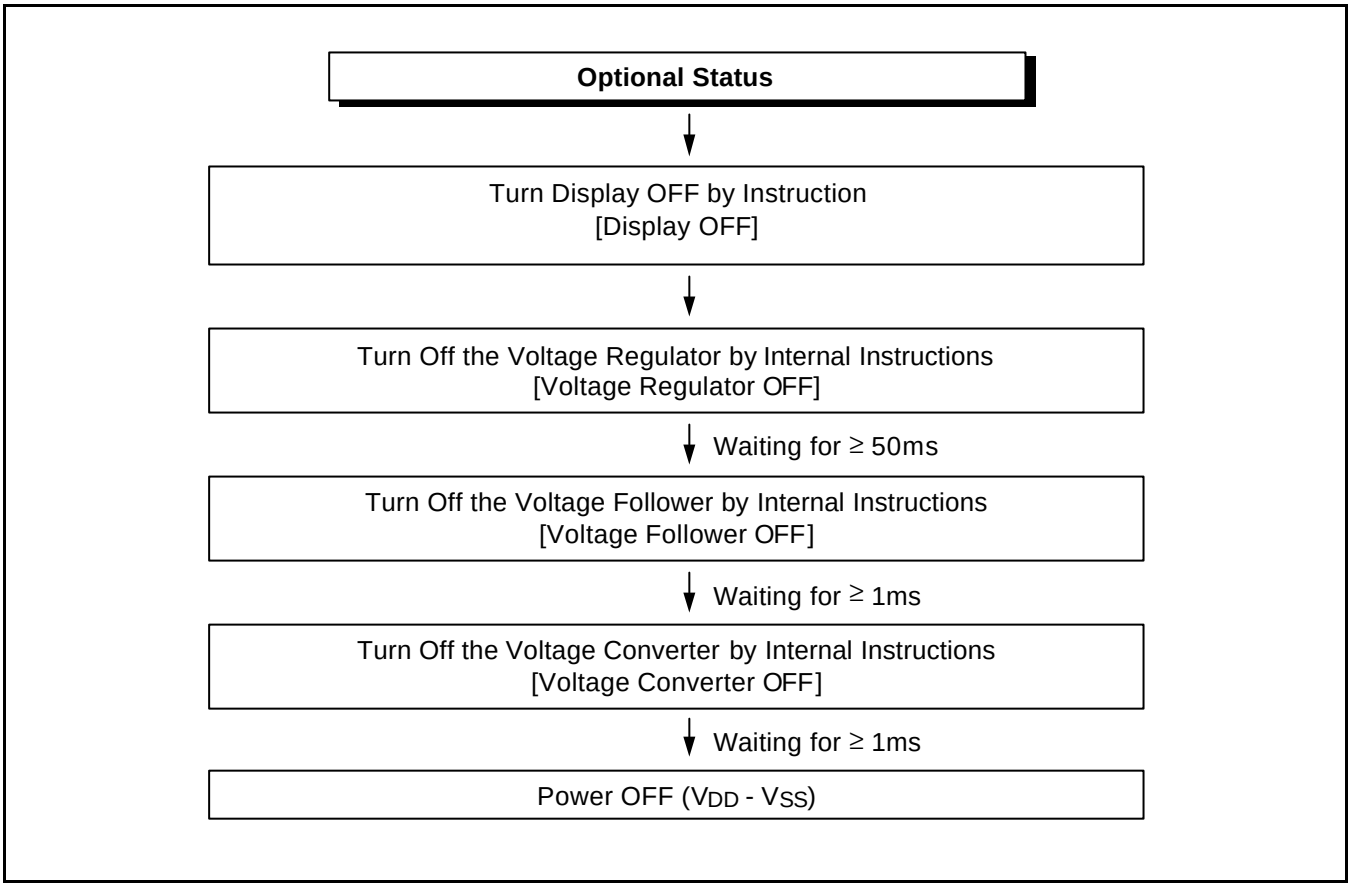


Figure 23. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 to +7.0	V
	V_{LCD}	- 0.3 to +13.0	V
Input voltage range	V_{IN}	- 0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 to +85	°C
Storage temperature range	T_{STR}	- 55 to +125	°C

Notes:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0V.
2. Voltages VLCD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		2.4	-	3.6	V	VDD *1
LCD power voltage (2)		VLCD		4.5	-	9.0	V	VLCD *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	Ta = 25°C Duty ratio = 1/65	32.7	43.6	54.5	KHz	CL *8
	External	f_{CL}		4.09	5.45	6.81		
Voltage converter Input voltage		VCI	× 3	2.4	-	3.6	V	VCI
			× 4	2.4	-	3.0		
Reference voltage		V_{REF}	Ta = 25°C - 0.05%/°C	2.04	2.1	2.16	V	*9

Dynamic Current Consumption when the Built-in Power Circuit is ON (At Operate Mode)

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, (VCI = V_{DD}, 3 times boosting) V0 – V_{SS} = 7.64V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	120	-	µA	*11
		V_{DD} = 3.0V, (VCI = V_{DD}, 3 times boosting) V0 – V_{SS} = 7.64V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	140	-	µA	*11
		V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – V_{SS} = 8.40V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	180	-	µA	*11
		V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – V_{SS} = 8.40V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	200	-	µA	*11

Current Consumption during Power Save Mode

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	During sleep	-	-	2	µA	
Standby mode current	I_{DDS2}	During standby	-	-	10	µA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{2 \times 8 \times 65}$
1/55	On-chip oscillator circuit is used	$\frac{f_{OSC}}{9}$	$\frac{f_{OSC}}{2 \times 9 \times 55}$
1/49	On-chip oscillator circuit is used	$\frac{f_{OSC}}{10}$	$\frac{f_{OSC}}{2 \times 10 \times 49}$
1/33	On-chip oscillator circuit is used	$\frac{f_{OSC}}{15}$	$\frac{f_{OSC}}{2 \times 15 \times 33}$

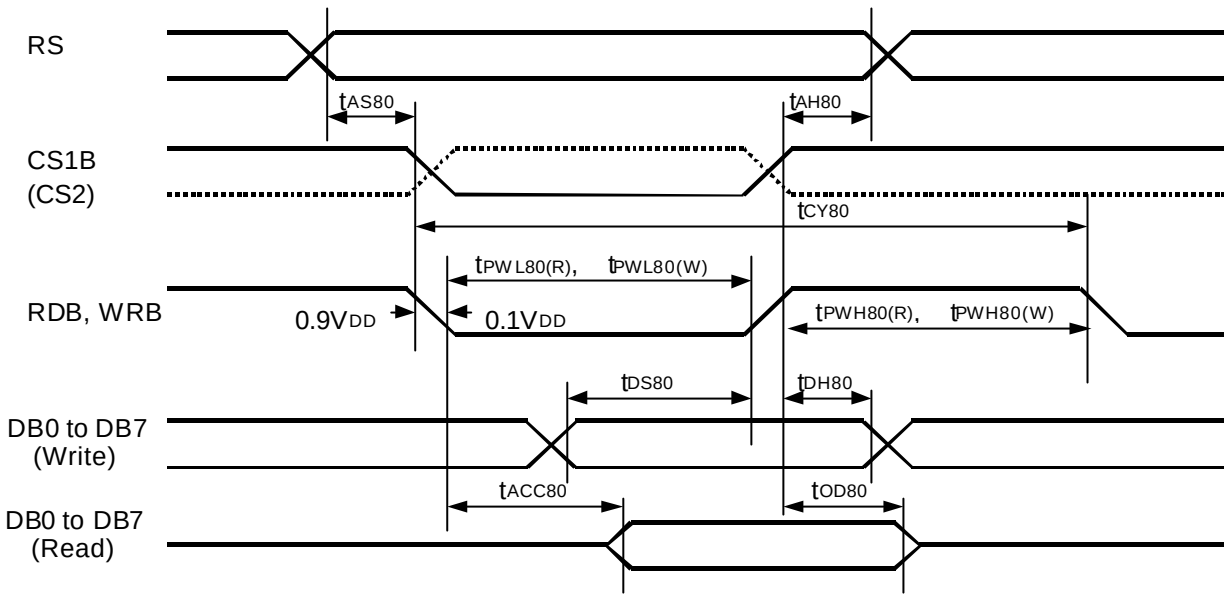
(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: LCD AC signal frequency)

[* Remark Solves]

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RDB, RW_WRB, RESETB, C68, PS, INTRS, HPMB pins.
*4. DB0 to DB7, FR, FRS, CL pins.
*5. CS1B, CS2, RS, DB[7:0], E_RDB, RW_WRB, RESETB, C68, PS, INTRS, HPMB pins.
*6. Applies when the DB[7:0], FR, FRS and CL pins are in high impedance.
*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON = ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8. See table 21 for the relationship between oscillation frequency and frame frequency.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust VLCD.
*10,11. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and WRB(RDB) is low.

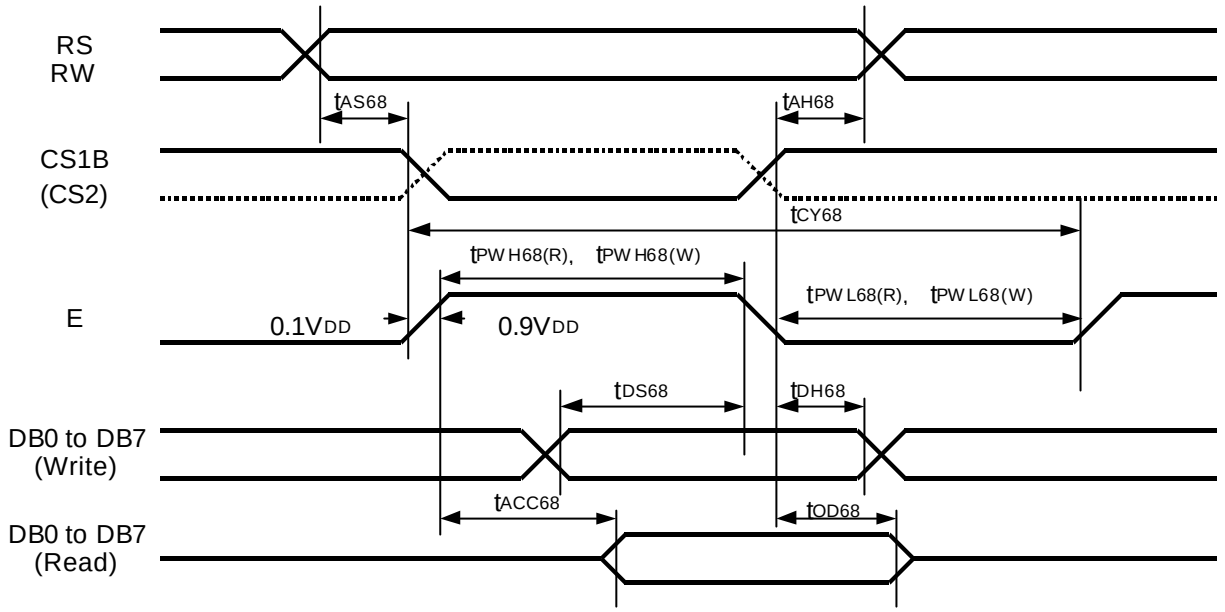
Figure 24. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time	RS	t_{CY80}	300	-	-	ns	
Pulse width (WRB)	RW_WRB	$t_{PWL80\ (W)}$ $t_{PWH80\ (W)}$	60 60	-	-	ns	
Pulse width (RDB)	E_RDB	$t_{PWL80\ (R)}$ $t_{PWH80\ (R)}$	60 60	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	140 100	ns	C_L = 100 pF

Note: 1. The input signal rising time and falling time (tr,tf) is specified at 15ns or less.
(tr + tf) < (t_{CY80} - $t_{PWL80\ (W)}$ - $t_{PWH80\ (W)}$) for write, (tr + tf) < (t_{CY80} - $t_{PWL80\ (R)}$ - $t_{PWH80\ (R)}$) for read

Read / Write Characteristics (6800-series Microprocessor)



** $t_{PWH68(W)}$ and $t_{PWH68(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and E is high.

Figure 25. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS RW	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time		RS	t_{CY68}	300	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	40 15	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	140 100	ns	C_L = 100 pF
Enable pulse width	Read Write	E_RDB	$t_{PWH68(R)}$ $t_{PWL68(R)}$ $t_{PWH68(W)}$ $t_{PWL68(W)}$	120 120 60 60	-	-	ns	

Note: 1. The input signal rising time and falling time (tr,tf) is specified at 15ns or less.
(tr + tf) < (t_{CY68} – $t_{PWH68\,(W)}$ – $t_{PWH68\,(W)}$) for write, (tr + tf) < (t_{CY80} – $t_{PWH68\,(R)}$ – $t_{PWL68\,(R)}$) for read

Serial Interface Characteristics

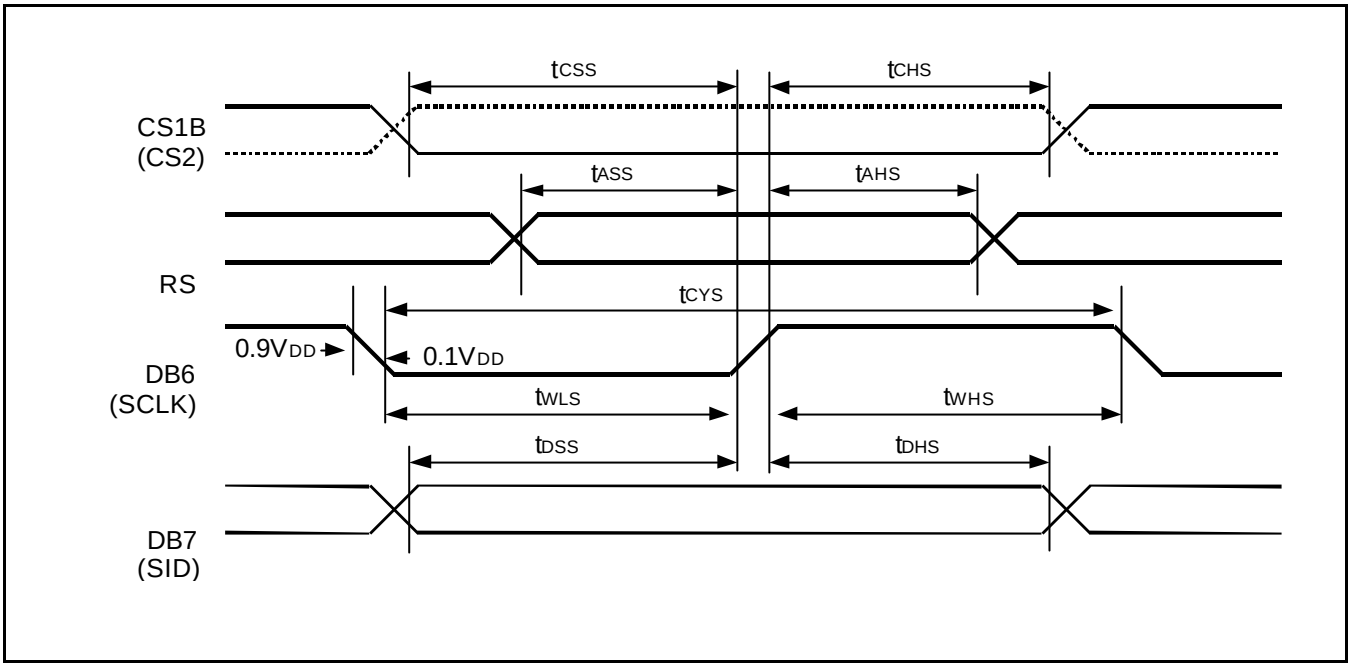


Figure 26. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	250 100 100	- - -	- - -	ns	
Address setup time Address hold time	RS	tASS tAHS	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	100 100	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	150 150	- -	- -	ns	

Note: 1. The input signal rising time and falling time (tr,tf) is specified at 15ns or less.

Reset Input Timing

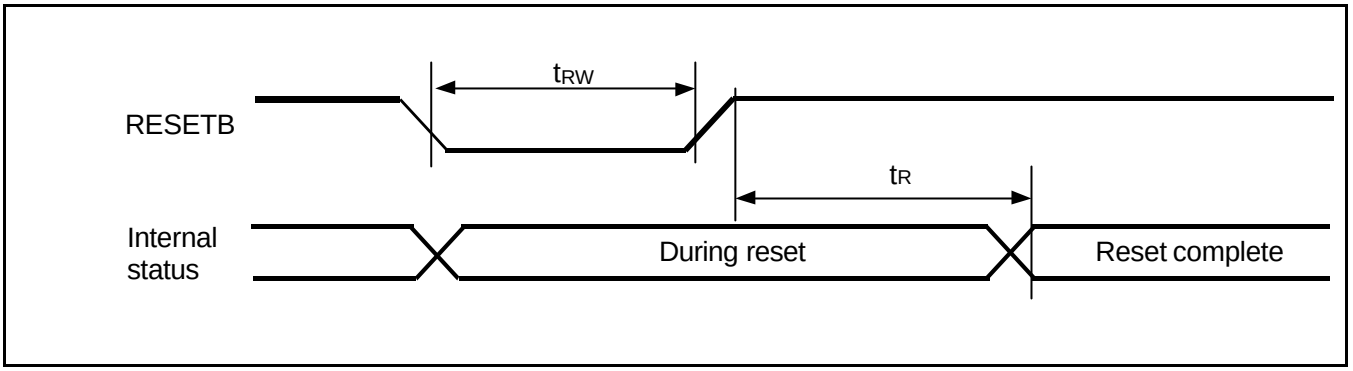


Figure 27. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	1.0	-	-	µs	
Reset time	-	t_R	-	-	1.0	µs	

Display Control Output Timing

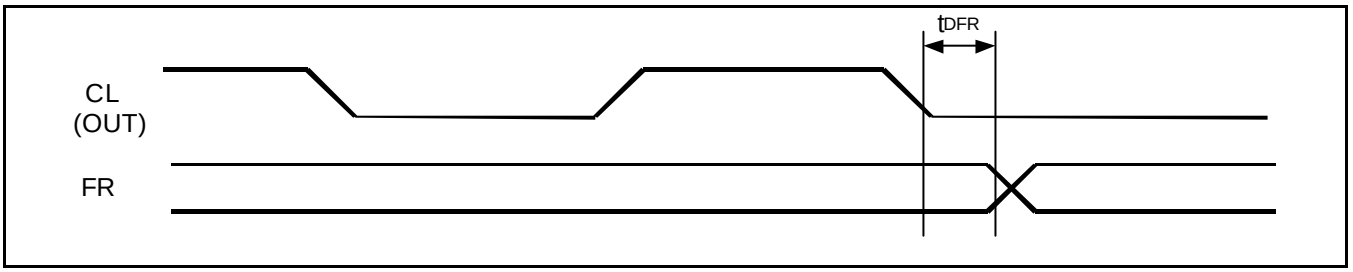


Figure 28. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	C_L = 50 pF

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", C68 = "H")

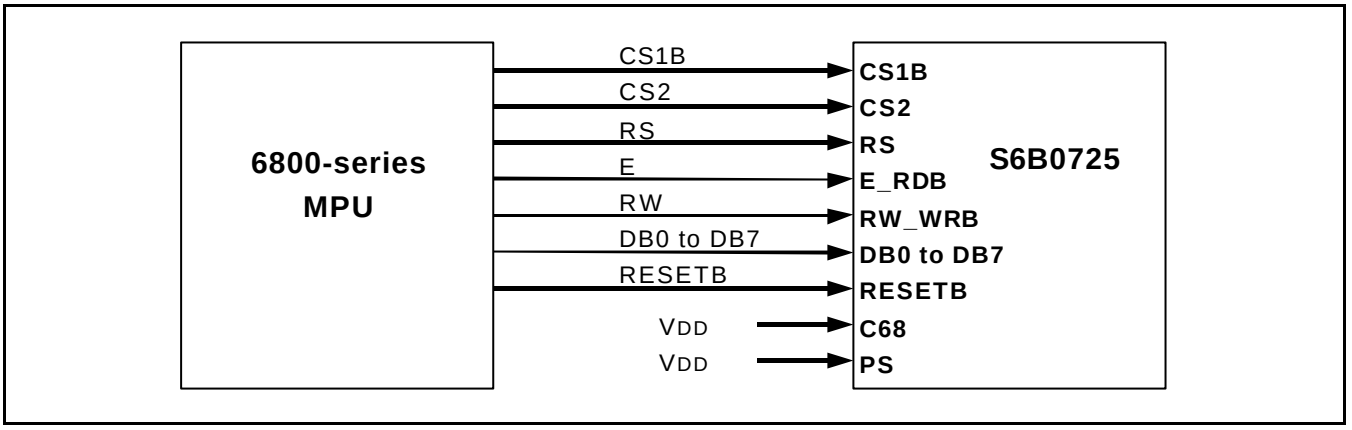


Figure 29. Interfacing with 6800-series

In Case of Interfacing with 8080-series (PS = "H", C68 = "L")

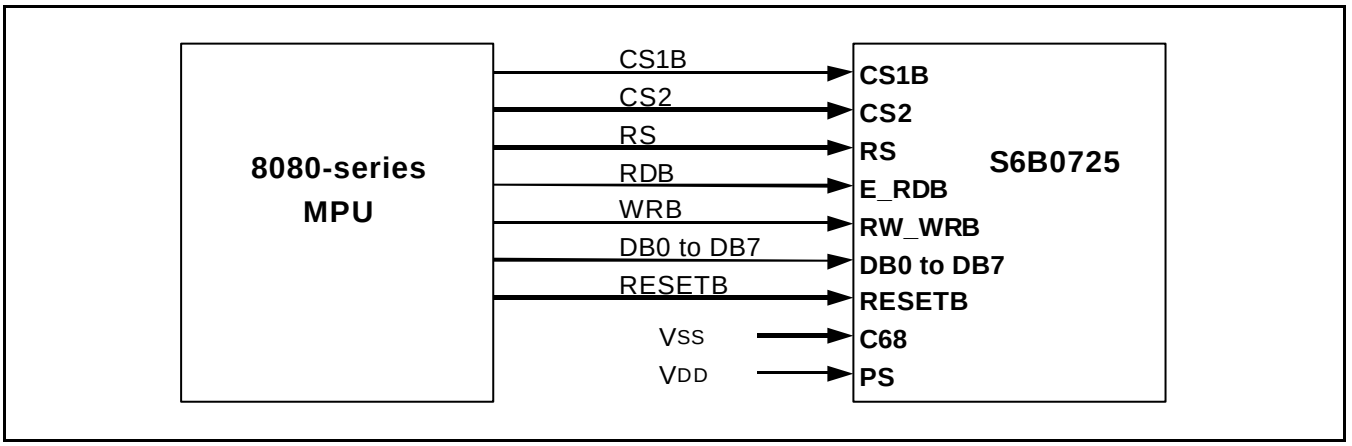


Figure 30. Interfacing with 8080-series

In Case of Serial Interface with RS Pin (PS = "L", C68 = "H ")

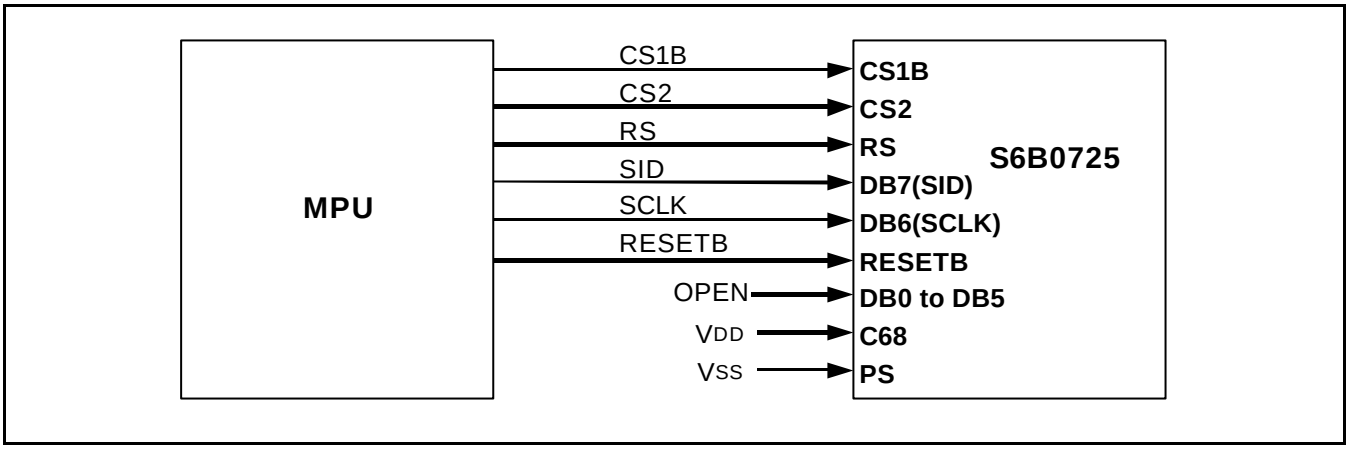


Figure 31. 4 Pin Serial Interface

In Case of Serial Interface with Software Command (PS = "L", C68 = "L ")

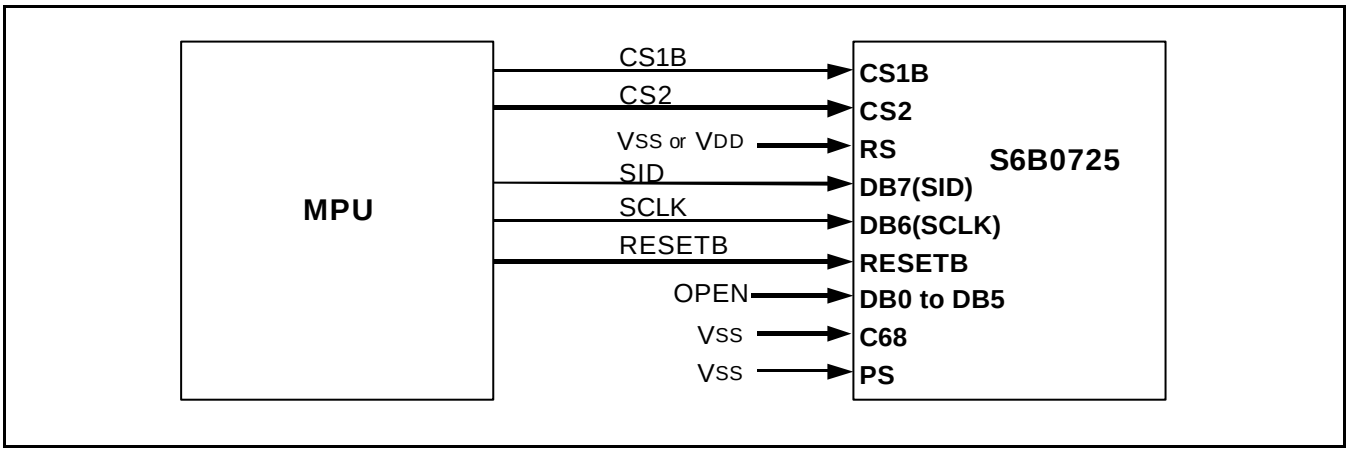


Figure 32. 3 Pin SPI Serial Interface

CONNECTIONS BETWEEN S6B0725A AND LCD PANEL

Single Chip Structure (1/65 Duty Configurations)

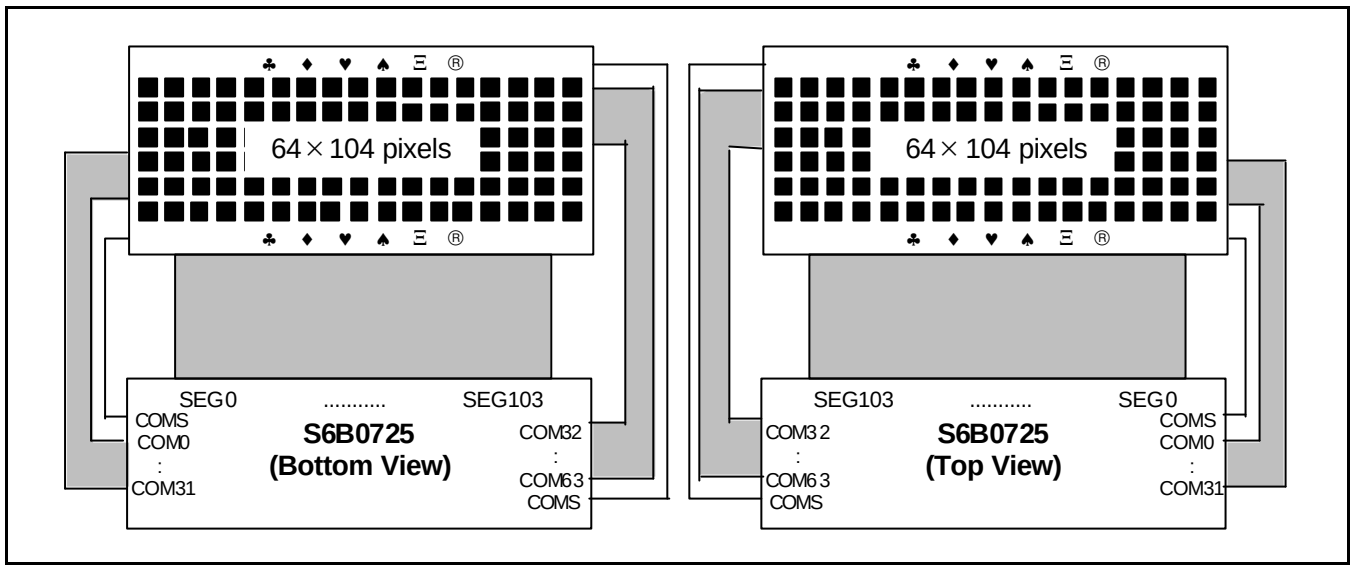


Figure 33. SHL = 1, ADC = 0

Figure 34. SHL = 1, ADC = 1

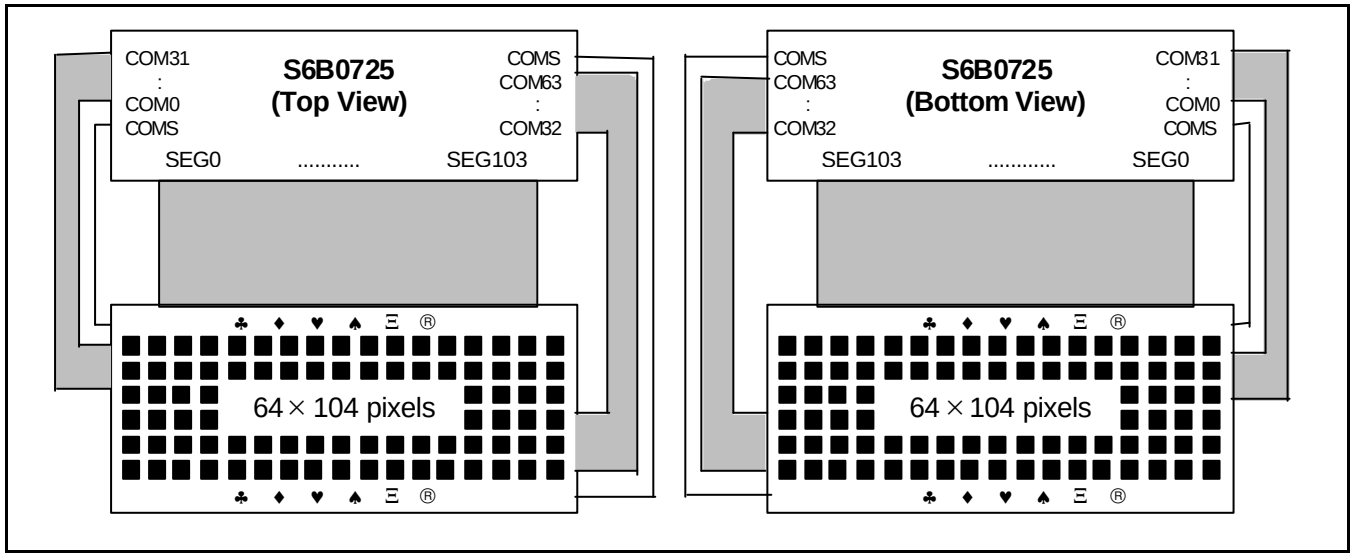


Figure 35. SHL = 0, ADC = 0

Figure 36. SHL = 0, ADC = 1

Single Chip Structure (1/55 Duty Configurations)

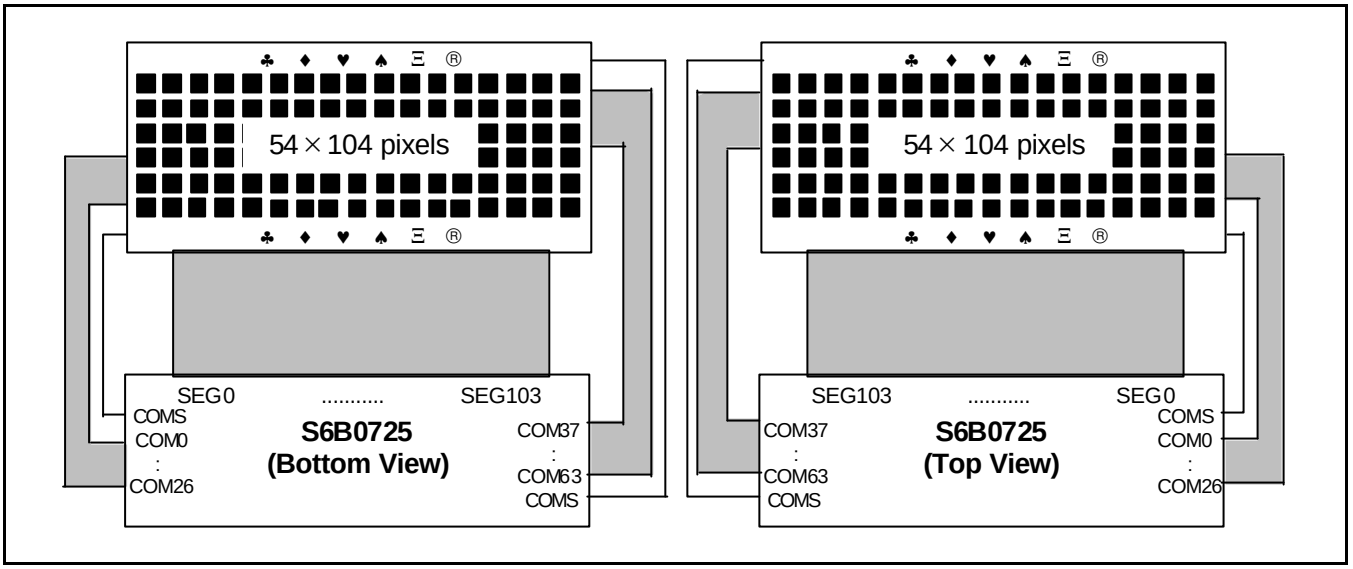


Figure 37. SHL = 1, ADC = 0

Figure 38. SHL = 1, ADC = 1

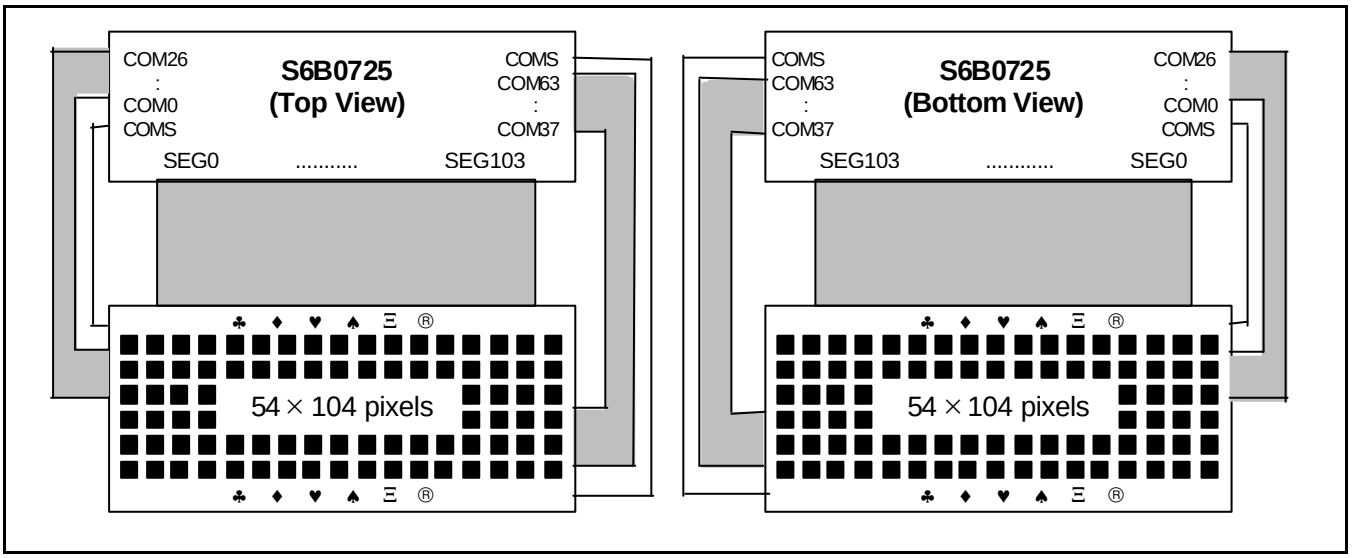


Figure 39. SHL = 0, ADC = 0

Figure 40. SHL = 0, ADC = 1

Single Chip Structure (1/49 Duty Configurations)

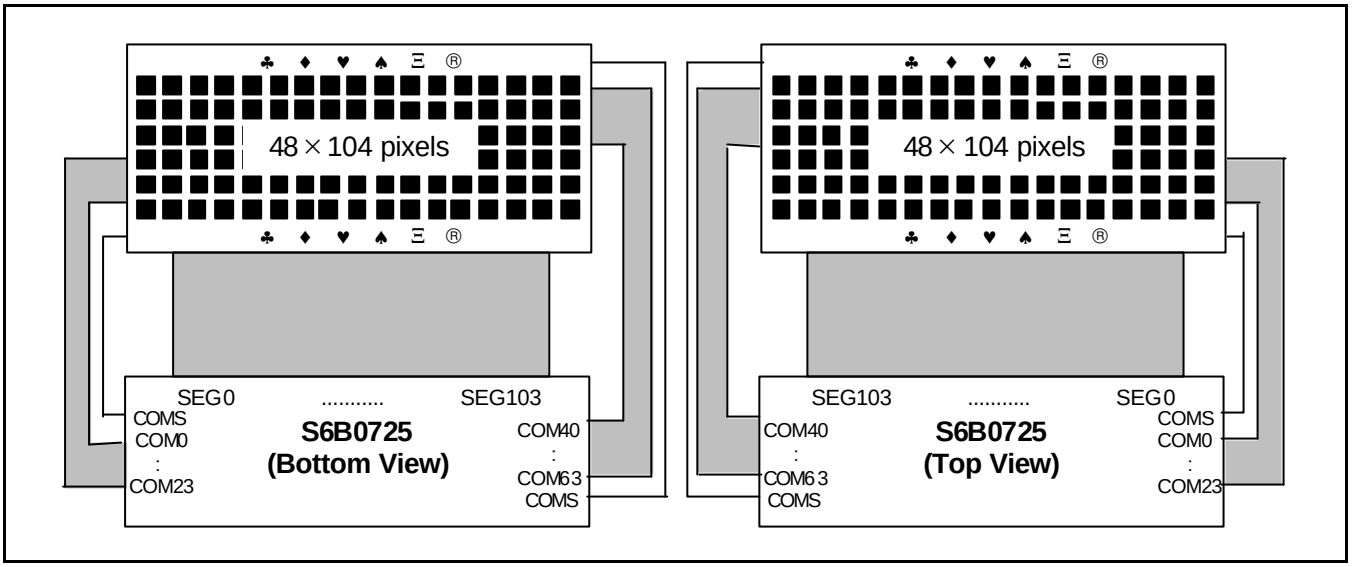


Figure 41. SHL = 1, ADC = 0

Figure 42. SHL = 1, ADC = 1

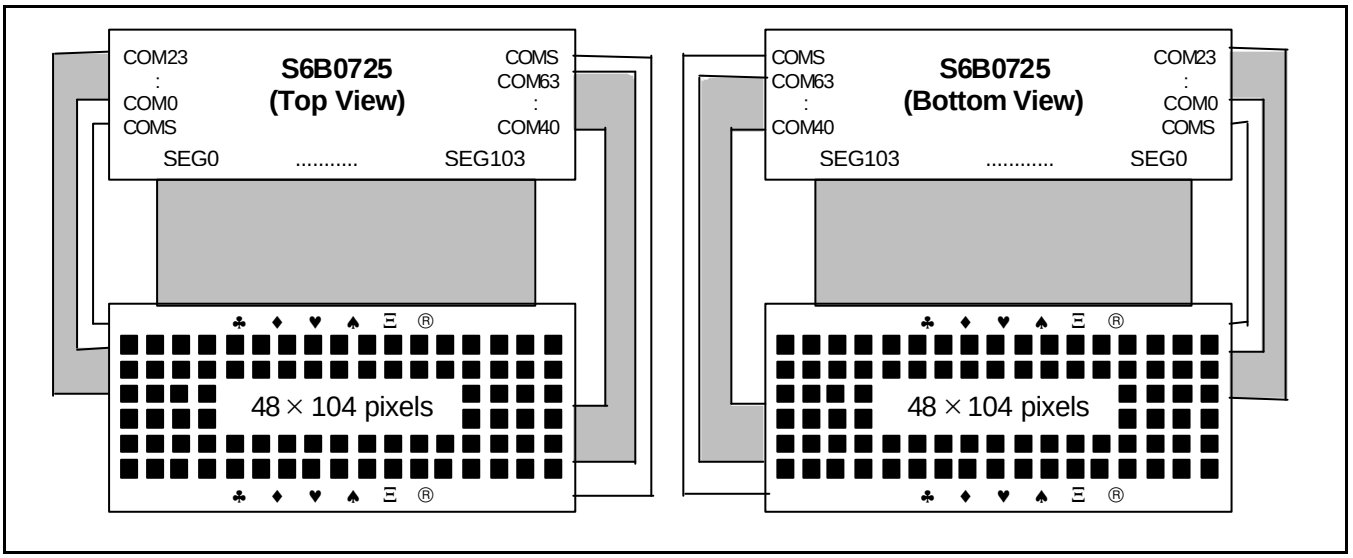


Figure 43. SHL = 0, ADC = 0

Figure 44. SHL = 0, ADC = 1

Single Chip Structure (1/33 Duty Configurations)

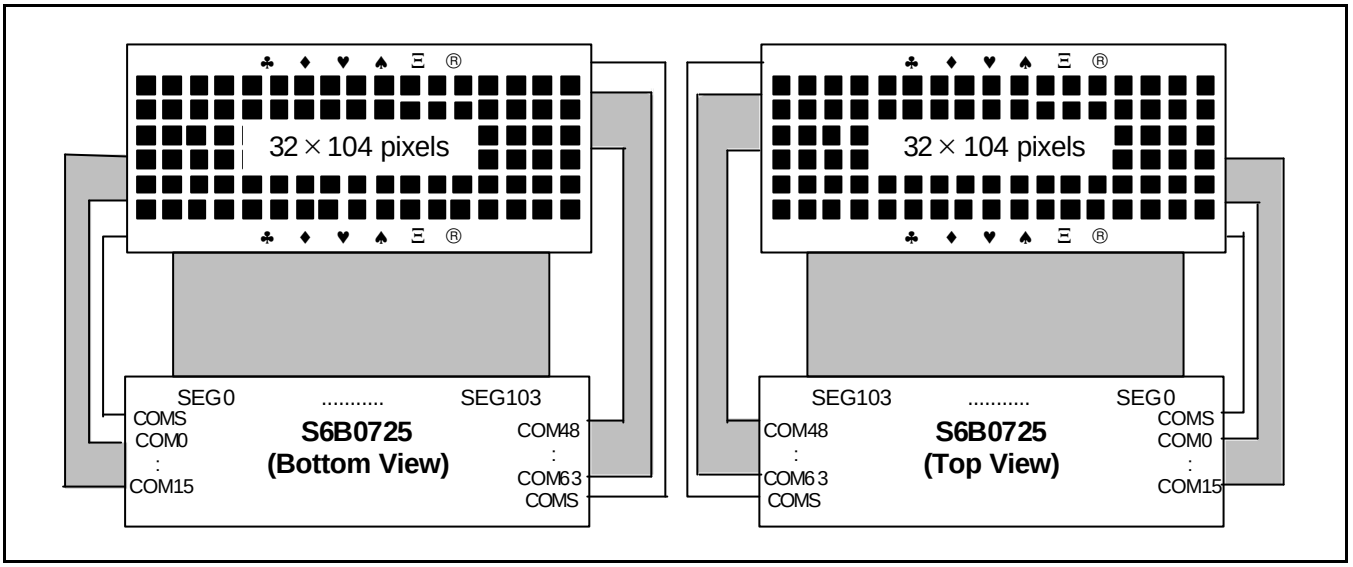


Figure 45. SHL = 1, ADC = 0

Figure 46. SHL = 1, ADC = 1

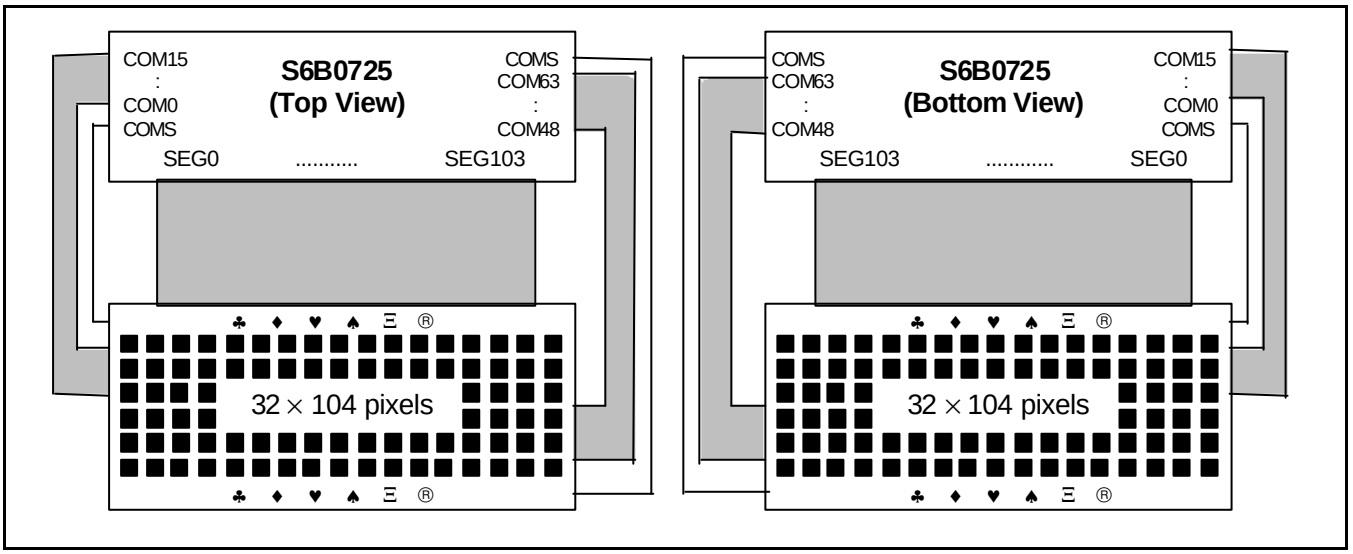


Figure 47. SHL = 0, ADC = 0

Figure 48. SHL = 0, ADC = 1

S6B0725A Application Circuit for Serial Mode

■ **4 Pin SPI Serial Interface**

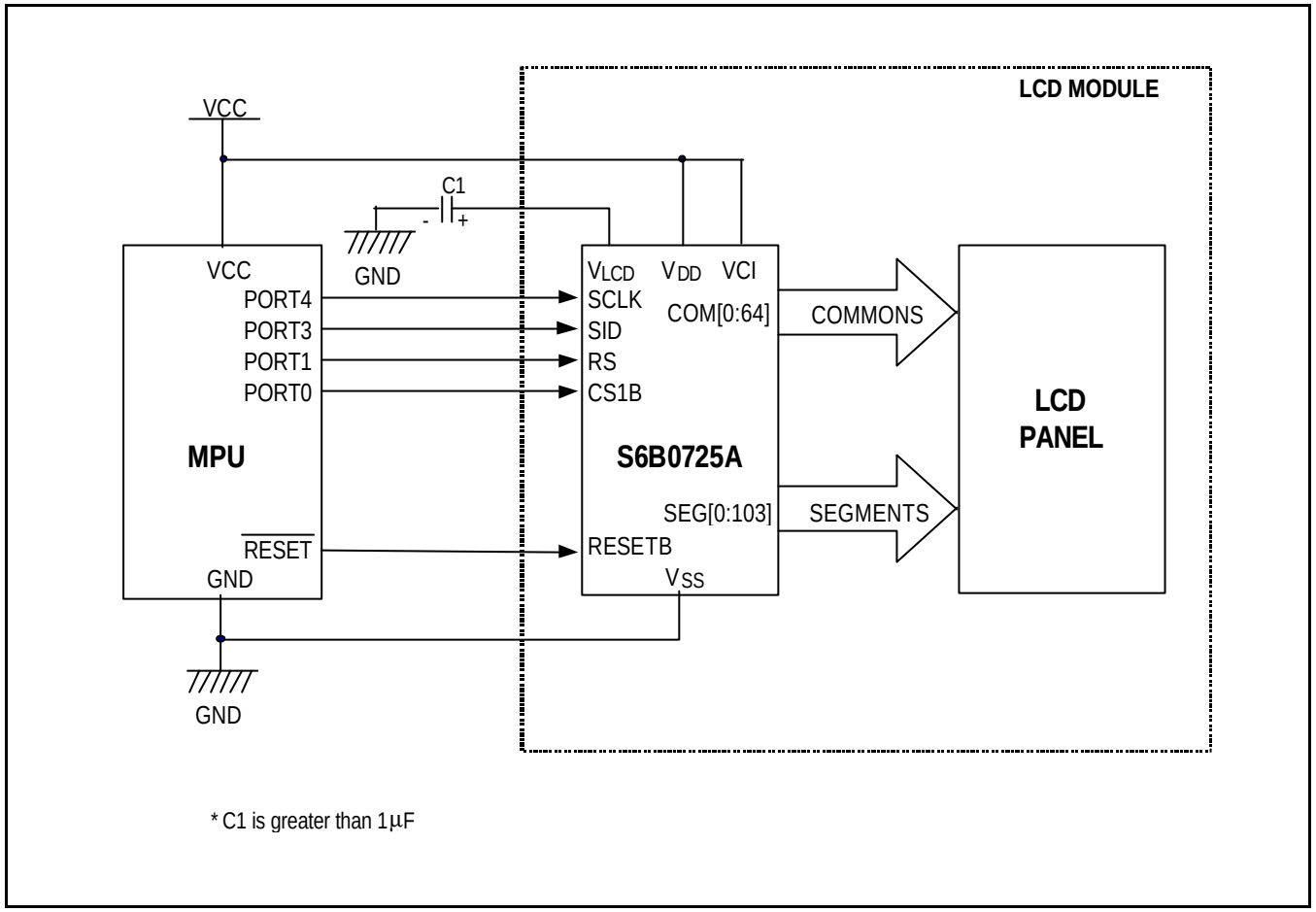


Figure 49. S6B0725A Application Circuit for 4 Pin SPI Serial Interface