Preliminary | COM'L

PAL24R10-10 Series

10 ns 28-pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 10 ns maximum propagation delay
- f_{MAX} = 55.5 MHz
- 8 ns maximum from clock input to data output
- Center V_{CC} and GND pins provide clean signals
- 28-pin version of popular architectures: 24L10, 24R10, 24R8, 24R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Register preload for testability
- Easy design with PALASM® software
- Programmable on standard PAL® device programmers
- 28-pin SKINNYDIP® and PLCC packages save space

GENERAL DESCRIPTION

The PAL24R10-10 Series (PAL24L10-10, PAL24R10-10, PAL24R8-10, PAL24R4-10) is a high-speed 28-pin version of the standard PAL16R8 and PAL20R8 Series. With a 10-ns maximum propagation delay time, the PAL24R10-10 Series provides high speed in a 28-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL24R10-10 Series adds two more inputs and two output or I/O pins to the standard 20R8 Series to take advantage of all the pins in the 28-pin PLCC package.

The family utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count. Power and ground have been placed on the center pins of the device, a configuration that minimizes ground bounce.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL24L10-10	16	8 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL24R10-10	14	10 reg.	8	reg.	pin
PAL24R8-10	14	8 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL24R4-10	14	4 reg. 6 comb.	8 7	reg. I/O	pin prog.

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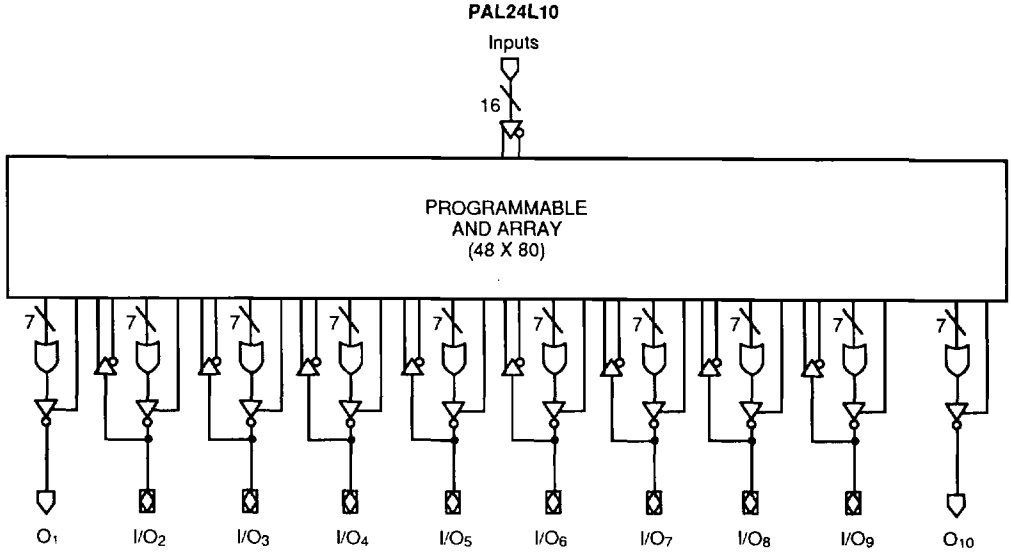
BLOCK DIAGRAMS

PAL24L10



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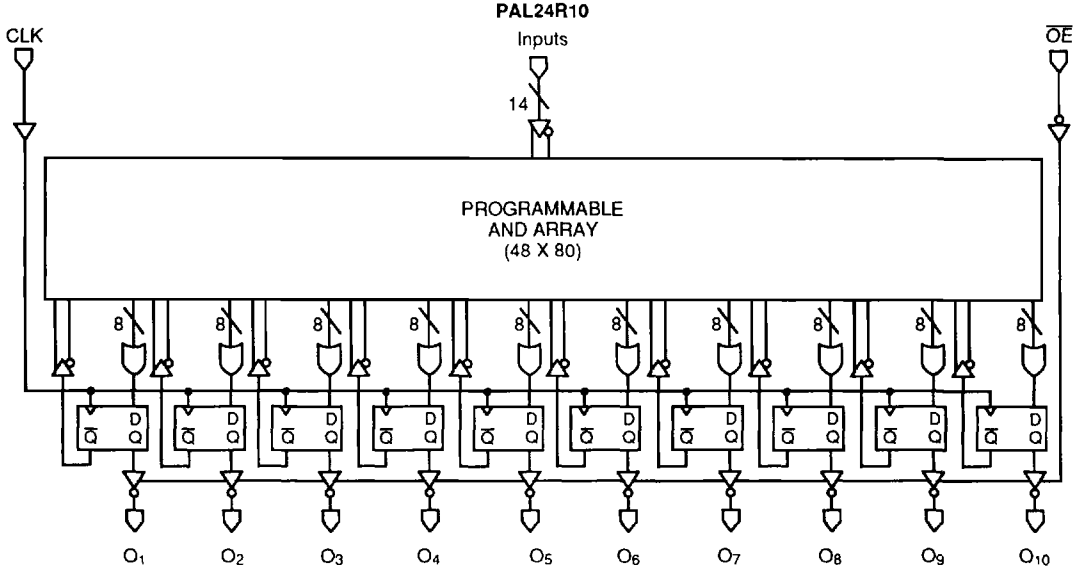
PAL24R10



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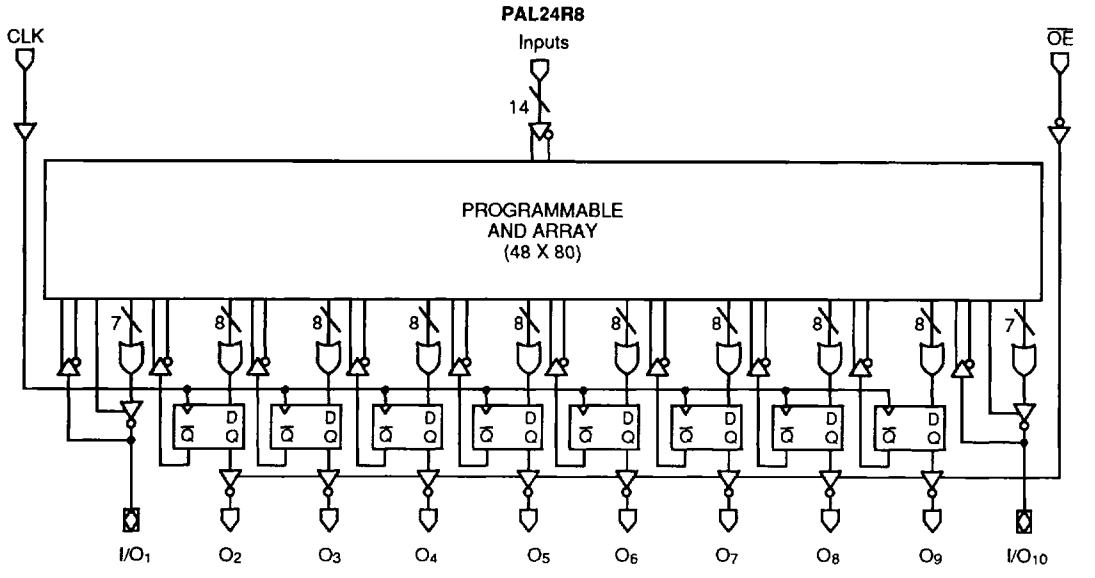
BLOCK DIAGRAMS



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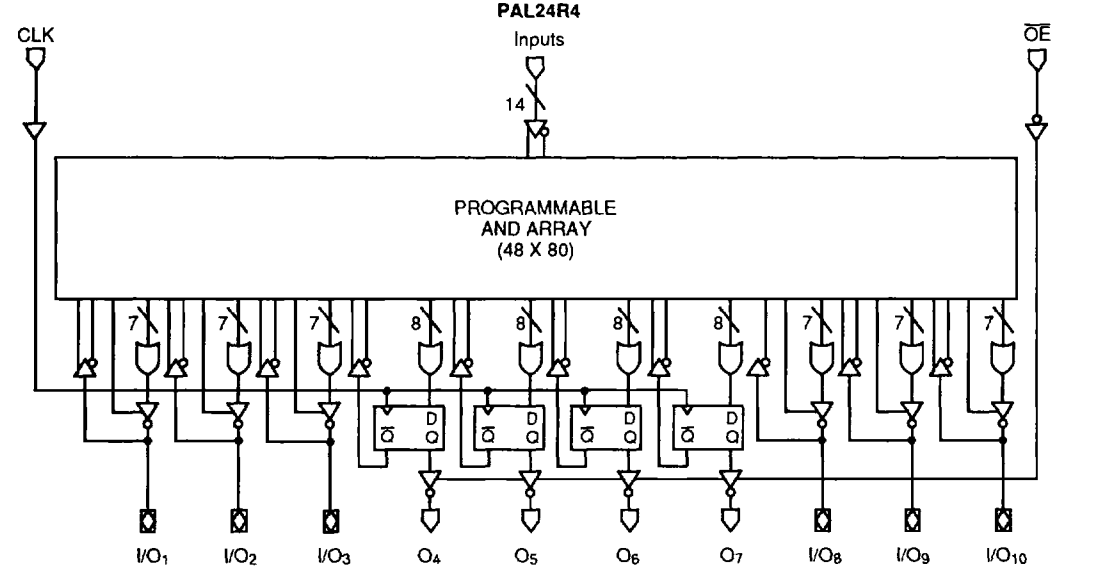

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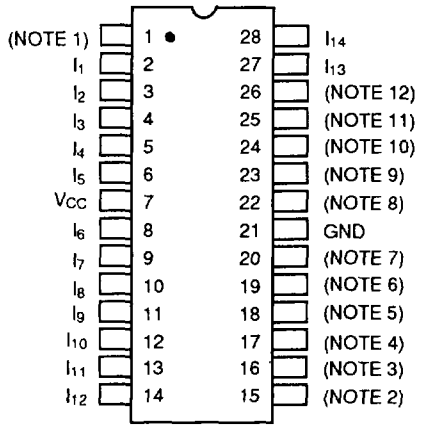
CONNECTION DIAGRAMS
Top View

SKINNYDIP



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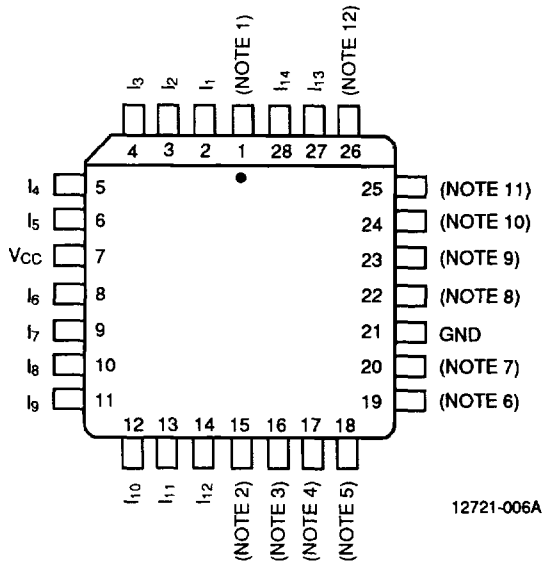
PLCC



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Note	24L10	24R10	24R8	24R4
1	I_0	CLK	CLK	CLK
2	I_{15}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	I/O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	O_7
10	I/O_8	O_8	O_8	I/O_8
11	I/O_9	O_9	O_9	I/O_9
12	O_{10}	O_{10}	I/O_{10}	I/O_{10}

Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

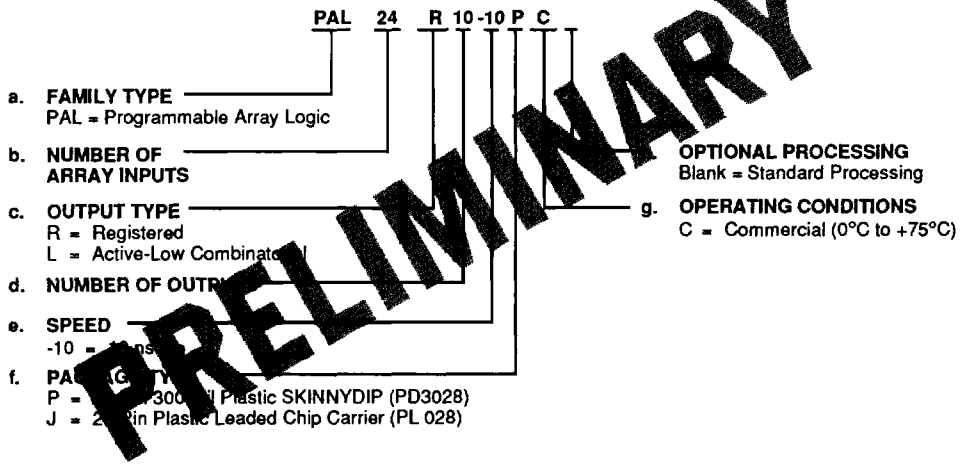
2

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Number of Array Inputs**
c. **Output Type**
d. **Number of Outputs**
e. **Speed**
f. **Package Type**
g. **Operating Conditions**
h. **Optional Processing**



Valid Combinations	
PAL24L10-10	PC, JC
PAL24R10-10	
PAL24R8-10	
PAL24R4-10	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Standard 28-pin PAL Family

The standard bipolar 28-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have fourteen dedicated input lines, and each combinatorial output is an I/O pin. The PAL24L10-10 has sixteen dedicated input lines, and eight of the ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL24R10-10 Series will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL24R10-10 Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL24R10-10 Series design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is unprogrammed.

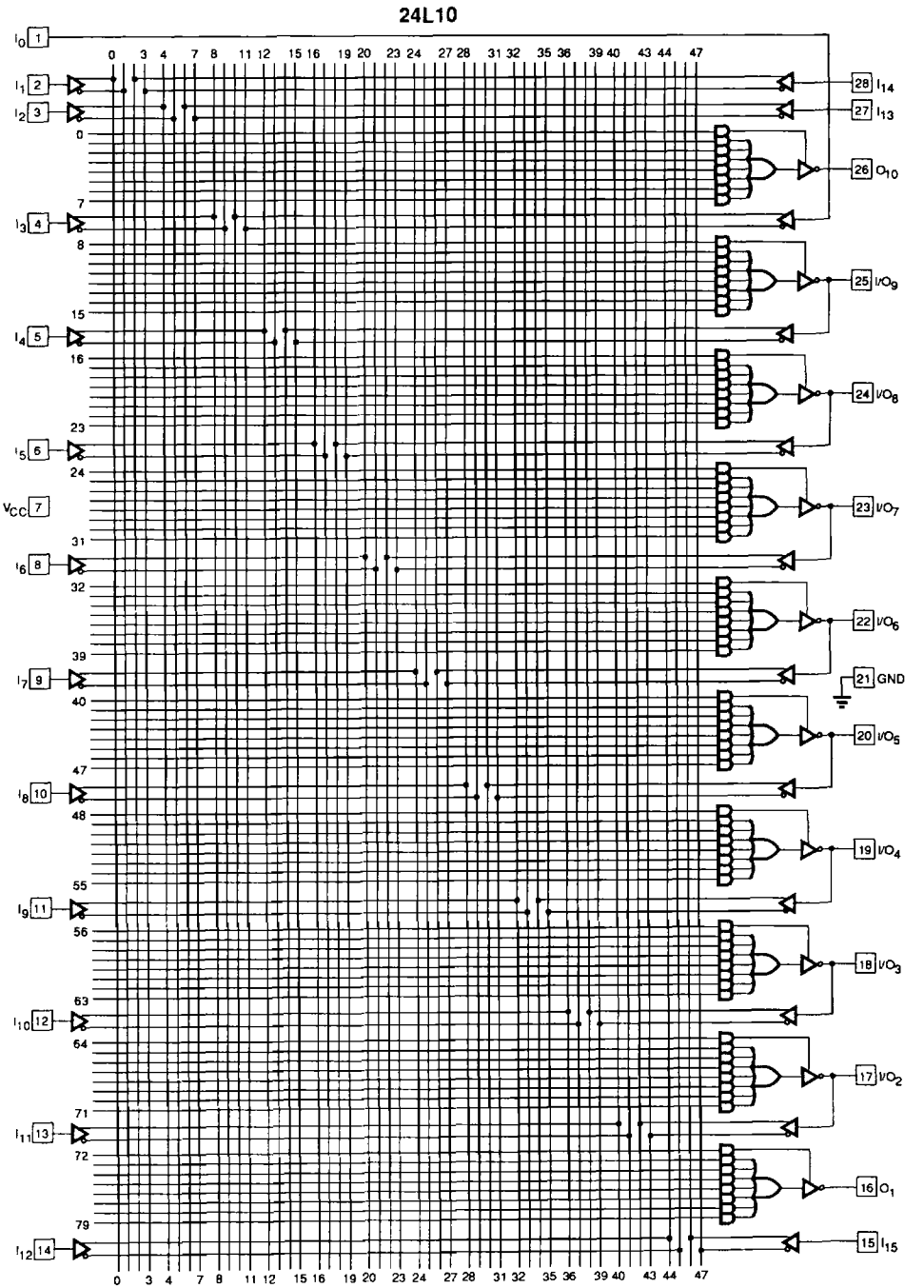
Quality and Testability

The PAL24R10-10 Series offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL24R10-10 Series is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.

LOGIC DIAGRAM



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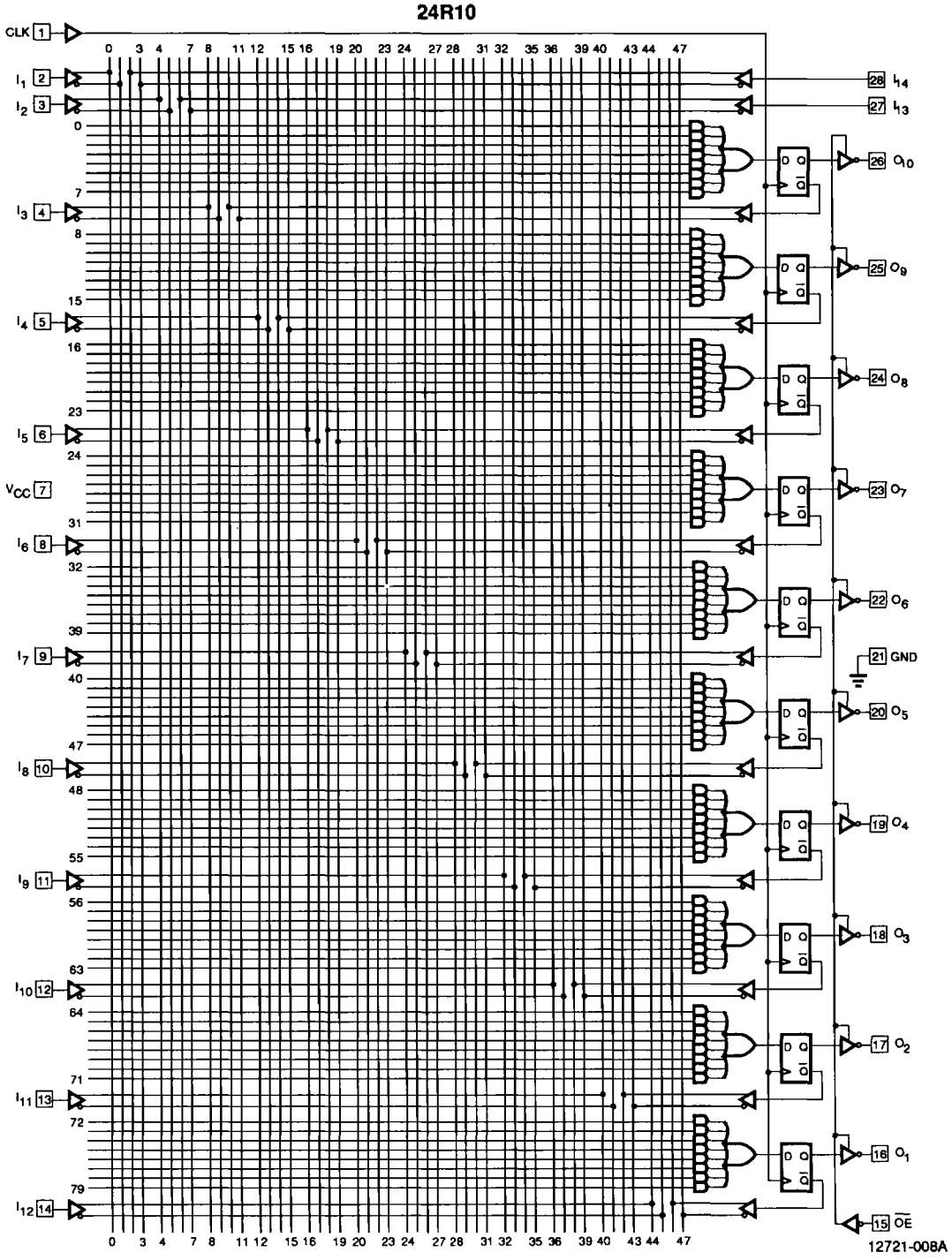
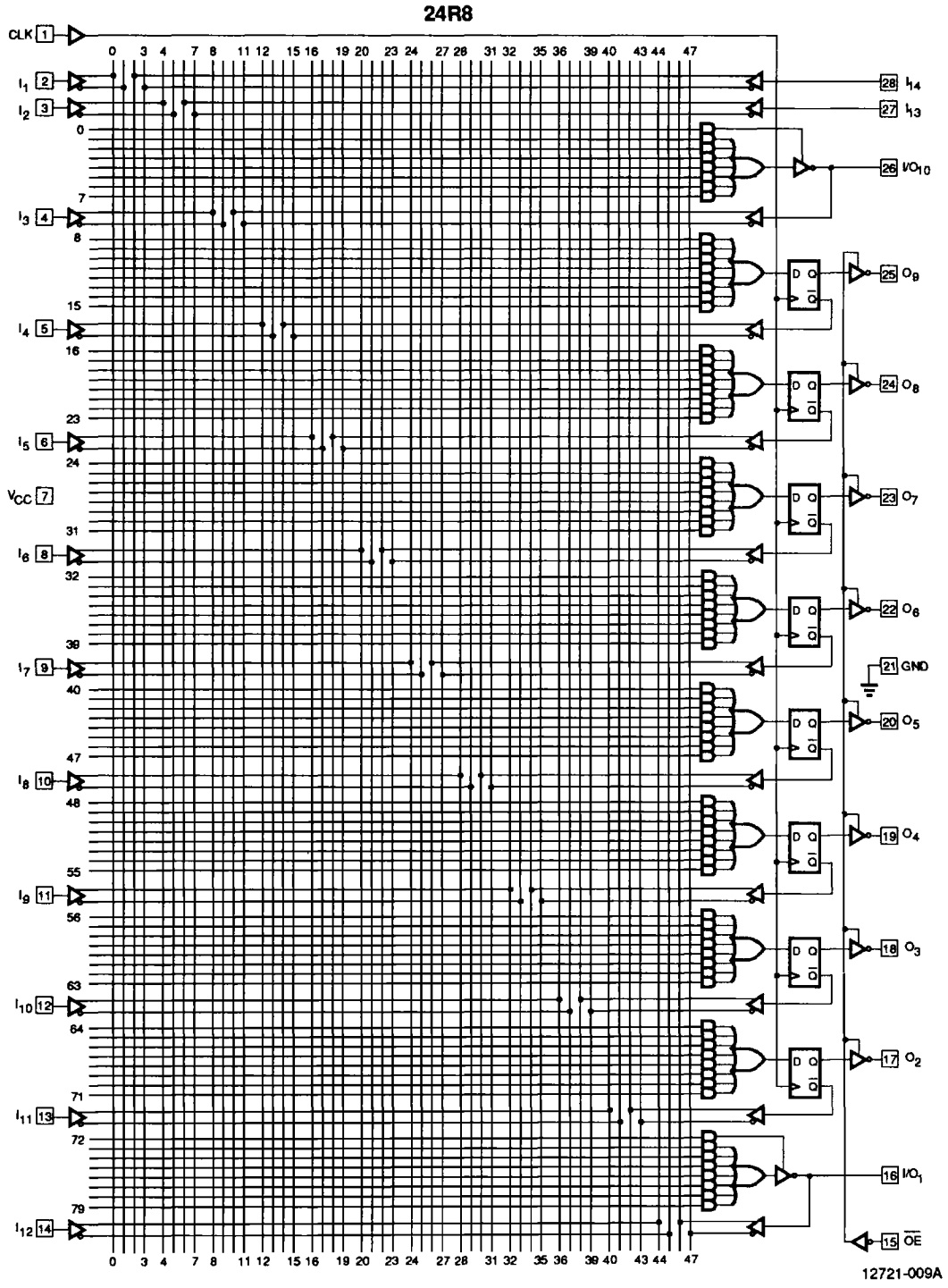
LOGIC DIAGRAM



LOGIC DIAGRAM



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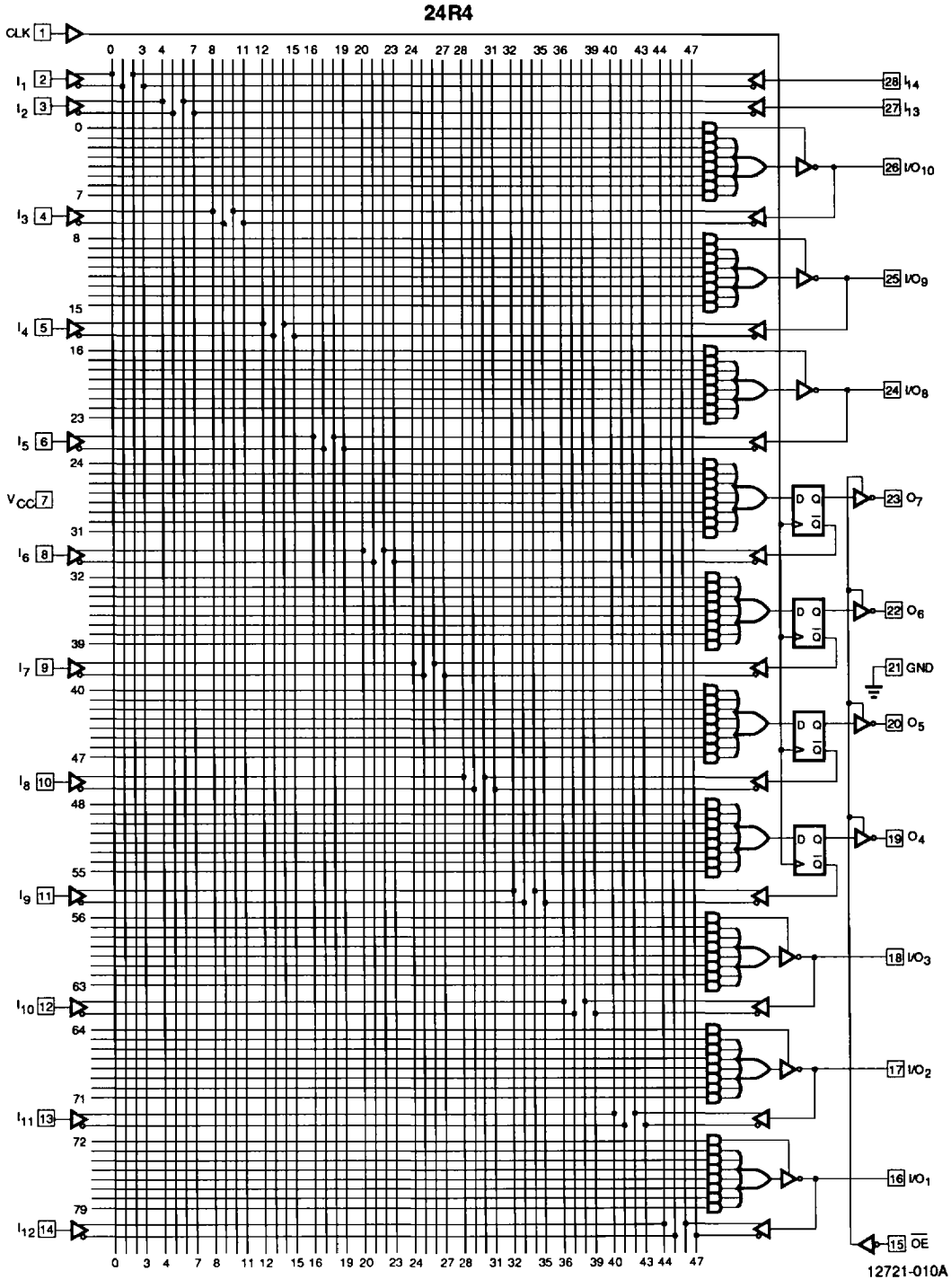
LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = [illegible] V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	[illegible] V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

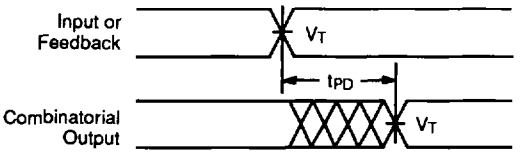
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			24L10, 24R8 24R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock				10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	8	ns
t_{CF}	Clock to Feedback (Note 4)					7	ns
t_{WL}	Clock Width	LOW		24R10, 24R8	7		ns
t_{WH}		HIGH		24R4	7		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		55.5		MHz
		Internal Feedback	$1/(t_S + t_{CF})$		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		71.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			24L10, 24R8 24R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

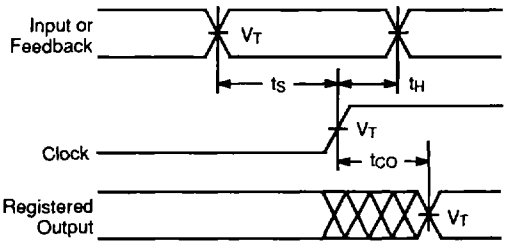
2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. *Calculated from measured f_{MAX} internal.*
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

SWITCHING WAVEFORMS



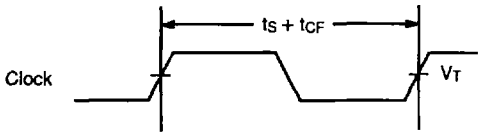
12015-010A

Combinatorial Output



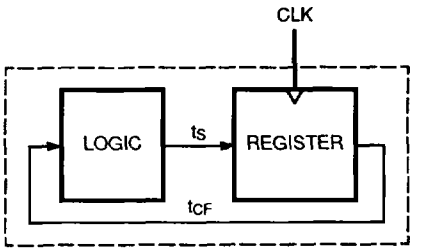
12015-012A

Registered Output

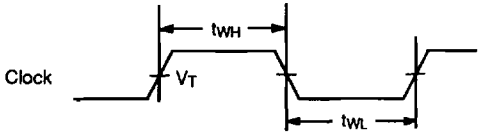


12149-025A

Clock to Feedback (f_{MAX} Internal)
See Path at Right

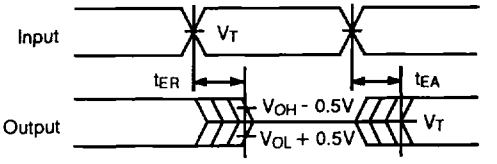


12015-021A



12015-011A

Clock Width



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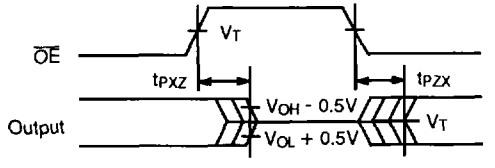
Input to Output Disable/Enable



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$\overline{OE}$ to Output Disable/Enable

Notes:

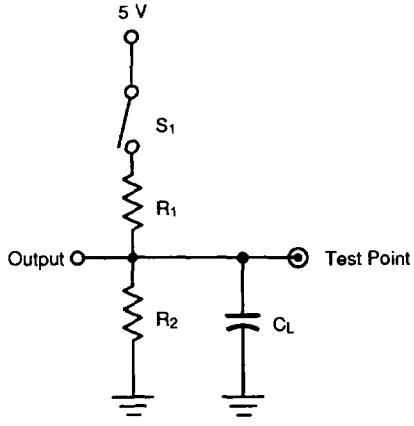
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

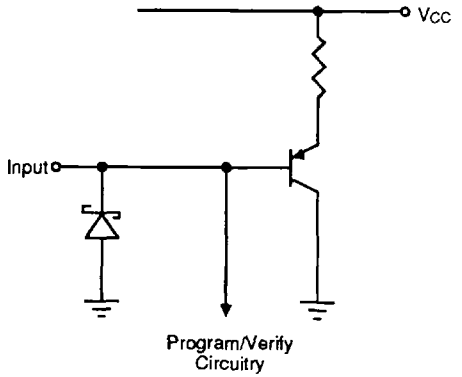


12350-019A

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5 V L → Z: V_{OL} + 0.5 V

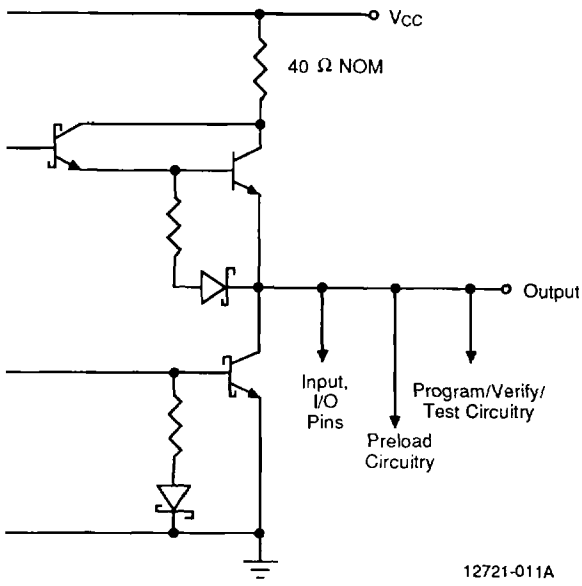
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



12350-020B

Typical Output



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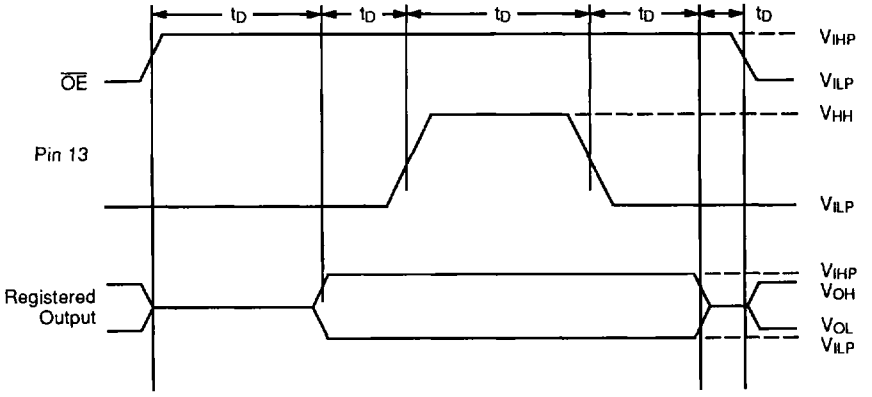
OUTPUT REGISTER PRELOAD

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Raise V_{CC} to V_{CCH}.
2. Set $\overline{OE}$ to V_{IHP} to disable output registers.
3. Apply either V_{IHP} or V_{ILP} to all registered outputs. Use V_{IHP} to preload a HIGH in the flip-flop; use V_{ILP} to preload a LOW in the flip-flop. Leave combinatorial outputs floating.
4. Pulse pin 13 to V_{HH}, then back to V_{ILP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower $\overline{OE}$ to V_{ILP} to enable the output registers.
7. Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	19.5	20	20.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
V_{CCH}	Power supply during preload	4.5	5.0	5.5	V
t_D	Delay time	100	200	1000	ns



10294-004B

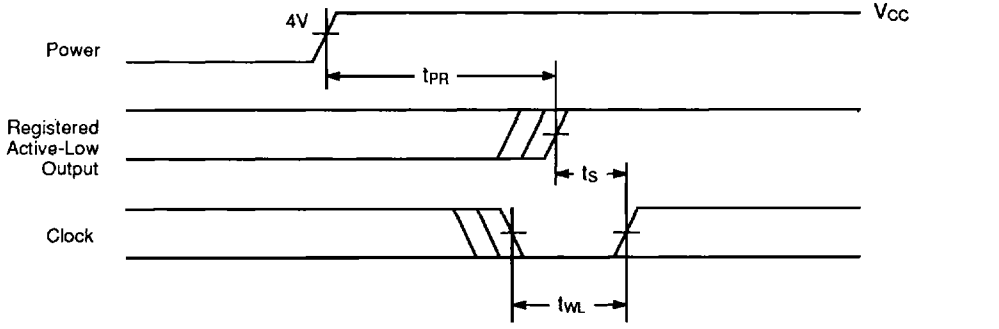
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



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Power-Up Reset Waveform