

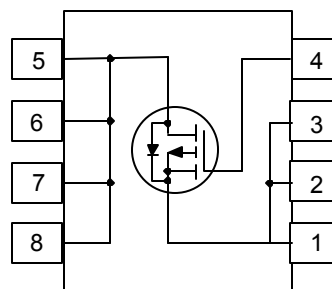
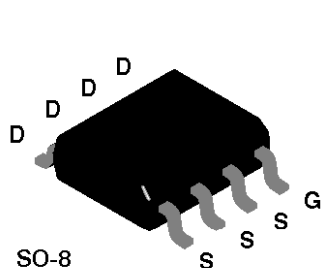
NDS9407 Single P-Channel Enhancement Mode Field Effect Transistor

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.0A, -60V. $R_{DS(ON)} = 0.15\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} = 0.24\Omega @ V_{GS} = -4.5V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS9407	Units
V_{DSS}	Drain-Source Voltage	-60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	± 3.0	A
	- Continuous $T_A = 70^\circ\text{C}$	± 2.4	
	- Pulsed $T_A = 25^\circ\text{C}$	± 12	
P_D	Maximum Power Dissipation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60			V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$			-1	μA	
			$T_A = 55^\circ\text{C}$			-10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$		-1	-2.3	V	
			$T_A = 125^\circ\text{C}$	-0.8	-1.8		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -3.0\text{ A}$		0.08	0.15	Ω	
			$T_A = 125^\circ\text{C}$		0.13		0.3
			$V_{GS} = -4.5\text{ V}, I_D = -1.6\text{ A}$		0.135		0.24
			$T_A = 125^\circ\text{C}$		0.2	0.48	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-12			A	
g_{FS}	Forward Transconductance	$V_{DS} = -15\text{ V}, I_D = -3.0\text{ A}$		6.8		S	
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1400		pF	
C_{oss}	Output Capacitance			290		pF	
C_{rss}	Reverse Transfer Capacitance			80		pF	
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -25\text{ V}, I_D = -1\text{ A},$ $V_{GEN} = -10\text{ V}, R_{GEN} = 6\ \Omega$		12	30	ns	
t_r	Turn - On Rise Time			12	40	ns	
$t_{D(off)}$	Turn - Off Delay Time			55	100	ns	
t_f	Turn - Off Fall Time			22	45	ns	
Q_g	Total Gate Charge	$V_{DS} = -30\text{ V},$ $I_D = -3.0\text{ A}, V_{GS} = -10\text{ V}$		37	50	nC	
Q_{gs}	Gate-Source Charge			4		nC	
Q_{gd}	Gate-Drain Charge			10		nC	

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -2.5 A (Note 2)		-0.9	-1.2	V

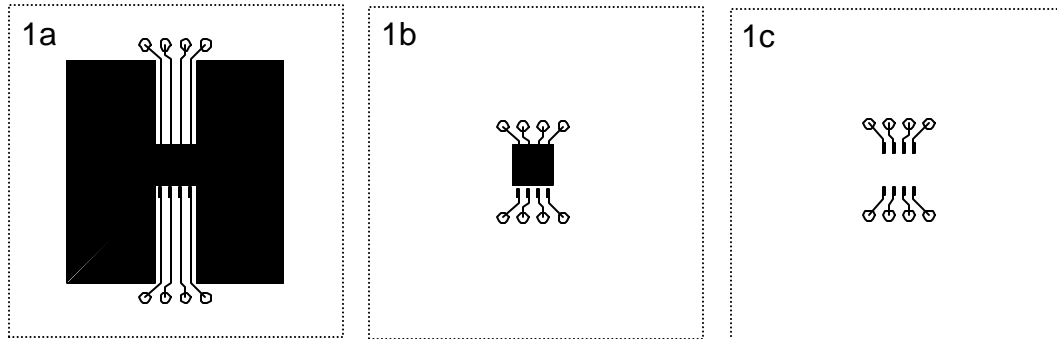
Notes:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

$$PD(t) = \frac{T_c - T_a}{R_{\theta J}(t)} = \frac{T_c - T_a}{R_{\theta J} + R_{\theta C}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_c$$

Typical R_{θJA} using the board layouts shown below on 4.5"x5" FR-4 PCB in still air environment

- 50°C/W when mounted on a 1 in² pad of 2oz copper.
- 105°C/W when mounted on a 0.04 in² pad of 2oz copper.
- 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

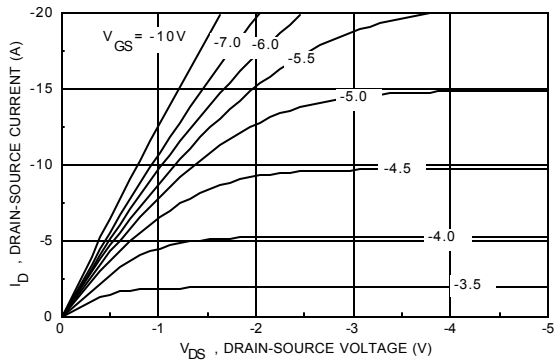


Figure 1. On-Region Characteristics.

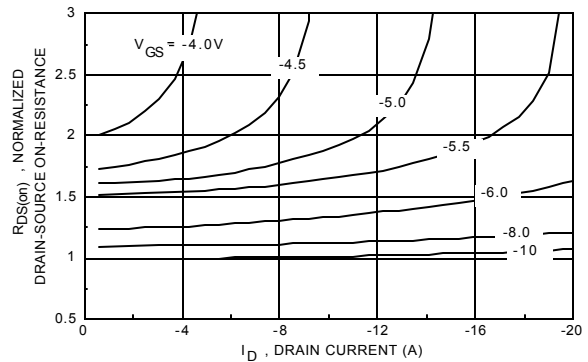


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

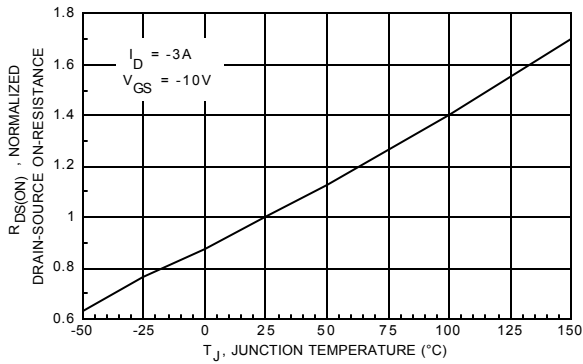


Figure 3. On-Resistance Variation with Temperature.

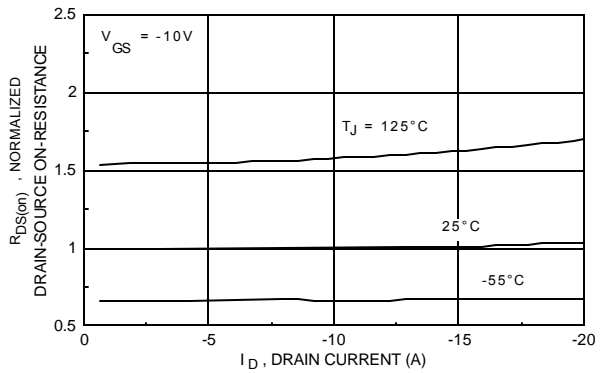


Figure 4. On-Resistance Variation with Drain Current and Temperature.

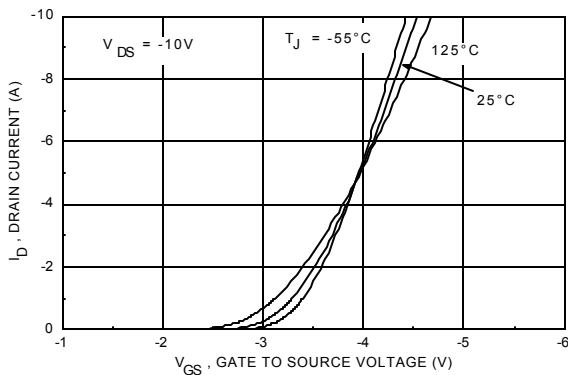


Figure 5. Transfer Characteristics.

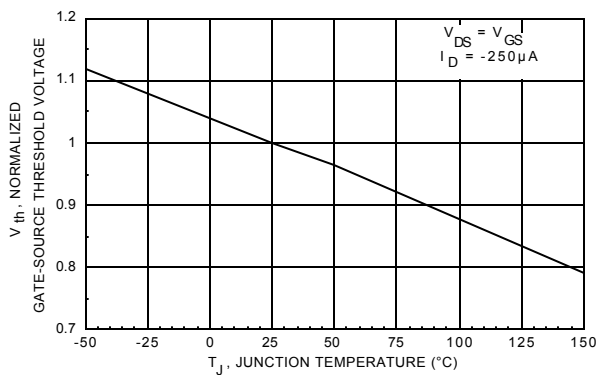


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

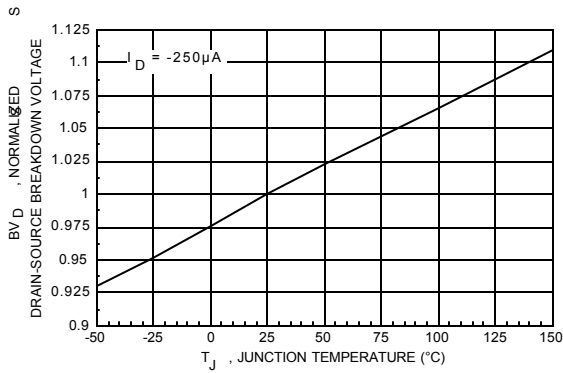


Figure 7. Breakdown Voltage Variation with Temperature.

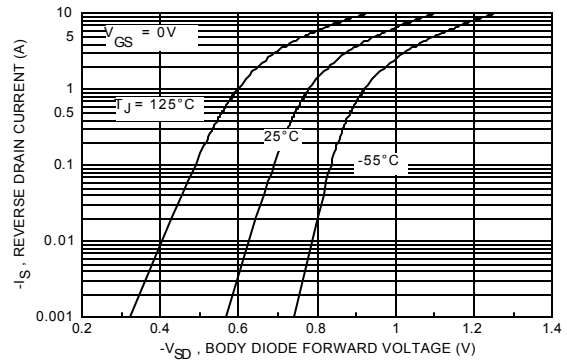


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

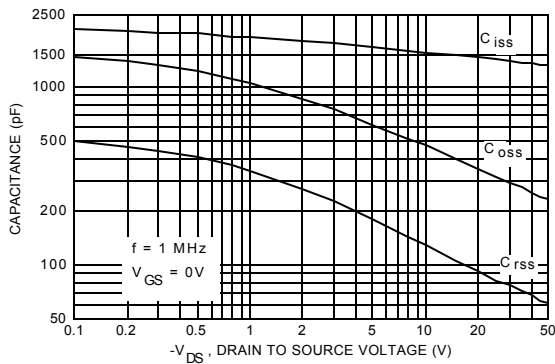


Figure 9. Capacitance Characteristics.

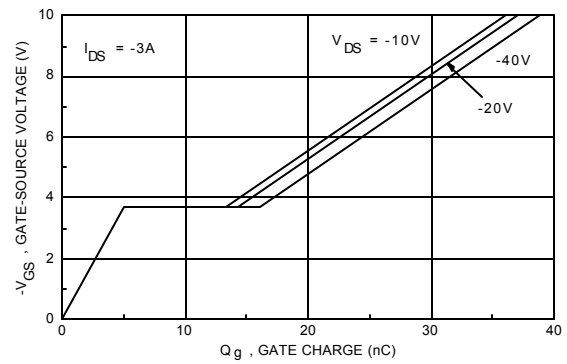


Figure 10. Gate Charge Characteristics.

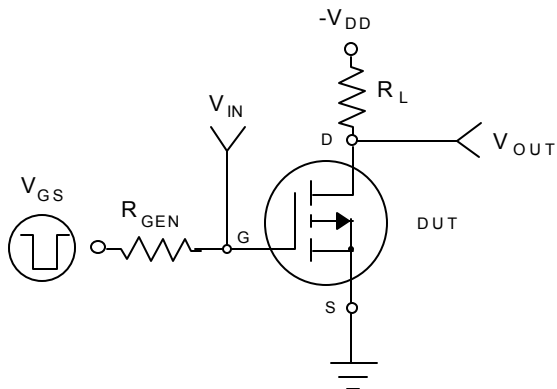


Figure 11. Switching Test Circuit

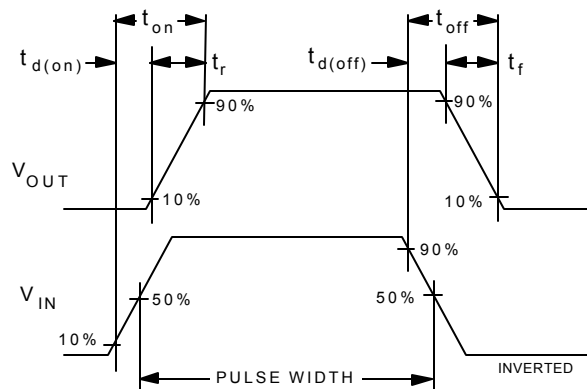


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

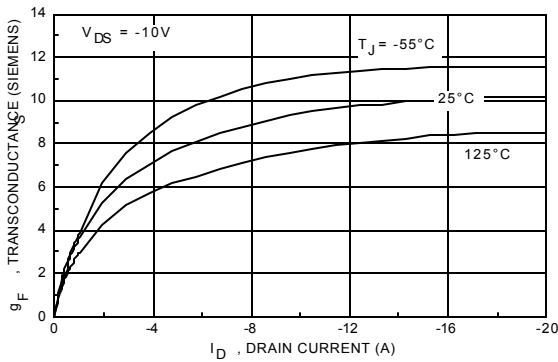


Figure 13. Transconductance Variation with Drain Current and Temperature

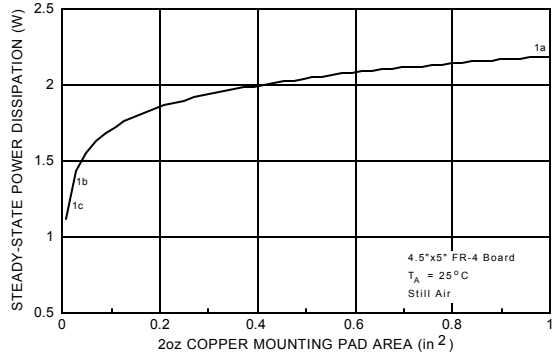


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

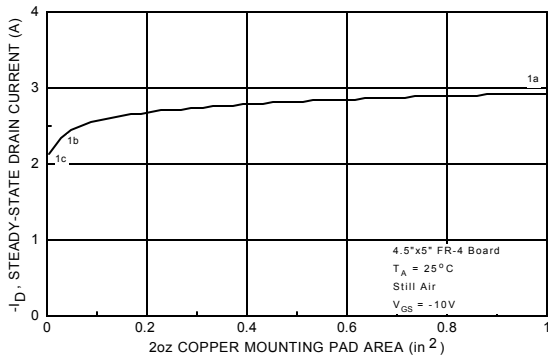


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

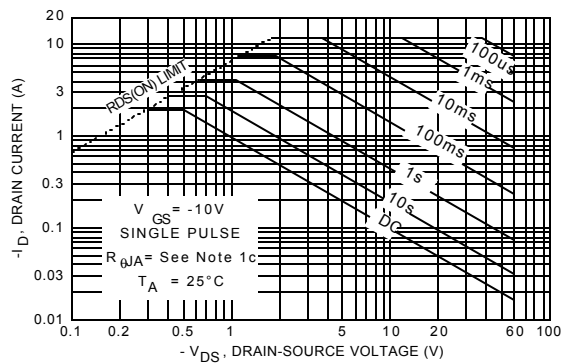


Figure 16. Maximum Safe Operating Area

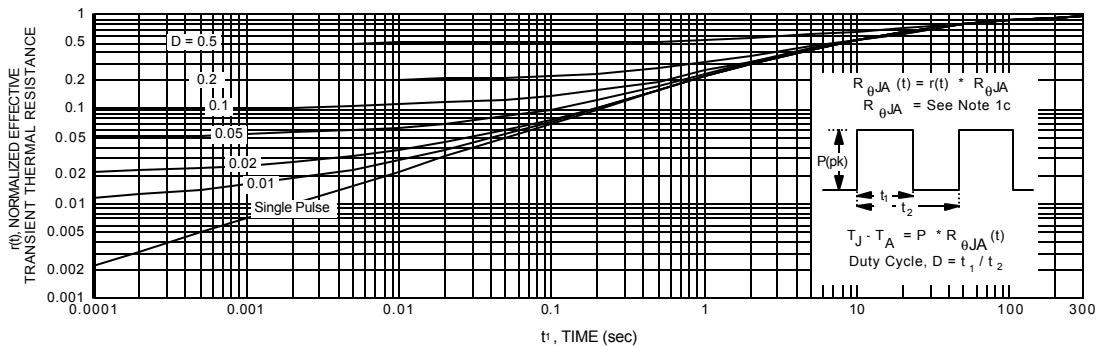


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions



SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

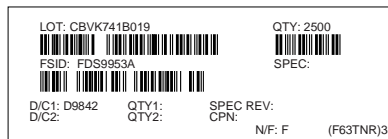
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample

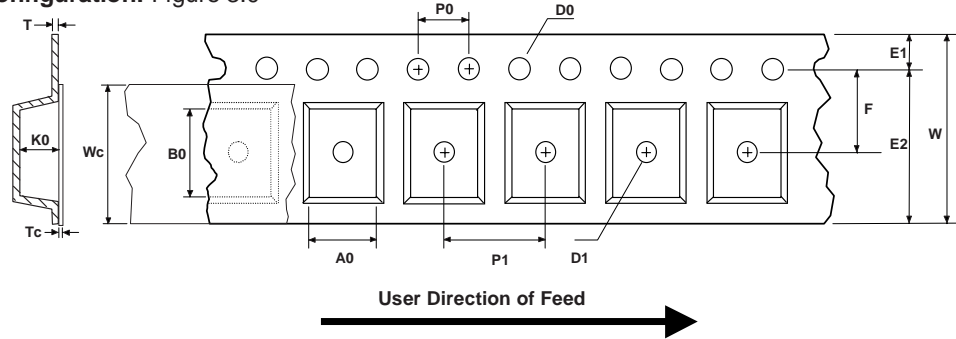


SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



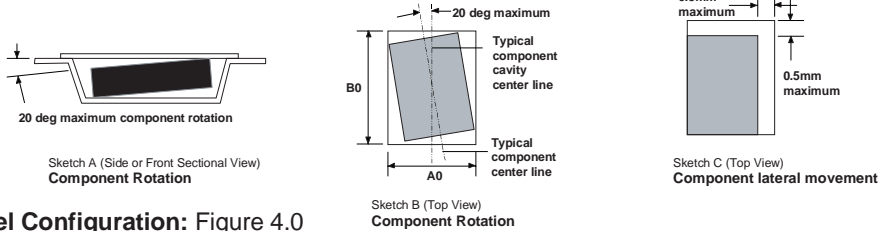
SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

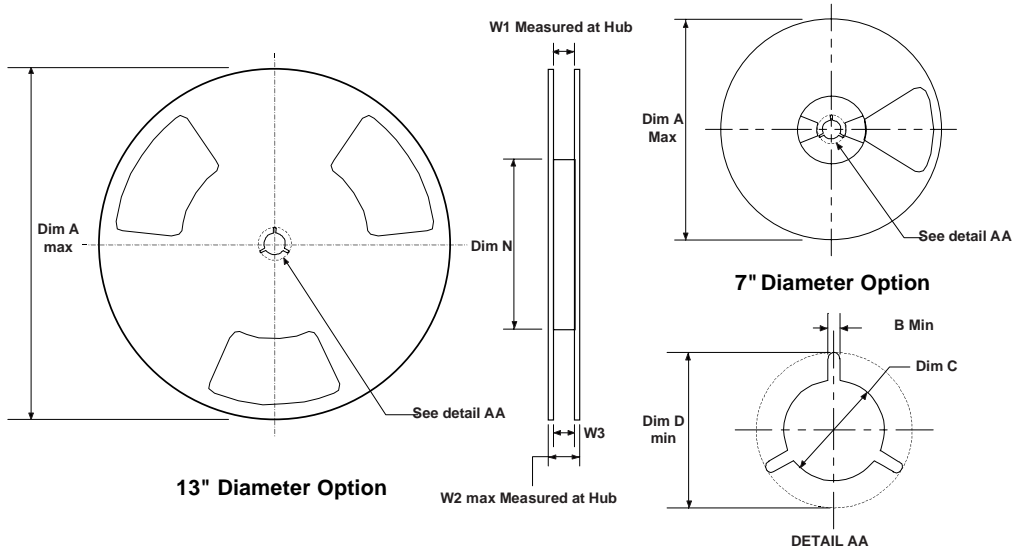


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

- STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

- THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH
- MAXIMUM LEAD 0.024 [0.609]

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FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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