LV0229XA

Monolithic Linear IC

Front Monitor OE-IC for Optical Pickups

ON Semiconductor®

http://onsemi.com

Overview

The LV0229XA is a front monitor optoelectronic IC for optical pickups that has a built-in photo diode compatible with three waveforms. LV0229XA is small size and type CSP packages.

Functions

- Pin photodiode compatible with three wavelengths incorporated.
- Gain adjustment (-5dB to +5dB in 256 steps) through serial communication.
- Amplifier to amplify differential output.

Features

- Photodiode compatible with three wavelengths incorporated, high-speed process employed.
- Compact, thin CSP package employed.
- Use AR coated glass for three-wavelength (One side).

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}		6	V
Allowable power dissipation	Pd	substrate *1, Ta = 75°C	105	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +100	°C

*1: Glass epoxy both-side substrate 55mm × 45mm × 1mm, Copper foil area (head: about 85% tail: about 70%)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

LV0229XA

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V_{CC}		4.5	5	5.5	V
Output load capacitance	Co		12	20	33	pF
Output load resistance	Zo		3			kΩ

Electrical and Optical Characteristics at Ta = 25°C, V_{CC} = 5V, R_L = 6kΩ, C_L = 20pF

Parameter	Symbol	Conditions	IV Gain	Ratings			Unit
				min	typ	max	
Current dissipation	I_{CC}			9	14	19	mA
Sleep current	Islp				0.2	0.5	mA
Output voltage when shielded	Vc	At shielding		1.85	2	2.15	V
Output offset voltage	Vofs	At shielding, voltage between VOP-VON		-30	0	30	mV
Temperature dependence of offset voltage *1	Vofs	Ta = -10 to +75°C		-60	0	60	μV/°C
Optical output voltage *1 Voltage between VOP-VON	VLC	λ = 780nm, G = 0dB	Low	1.93	2.41	2.90	mV/μW
	VH1C		Middle	4.58	5.73	6.87	
	VH2C		High	10.86	13.58	16.29	
	VLD	λ = 650nm, G = 0dB	Low	2.03	2.54	3.05	
	VH1D		Middle	4.82	6.02	7.23	
	VH2D		High	11.42	14.28	17.13	
	VLB	λ = 405nm, G = 0dB	Low	1.27	1.59	1.90	
	VH1B		Middle	3.01	3.76	4.52	
	VH2B		High	7.14	8.92	10.71	
Light output voltage adjustment range *1	G	G = 0dB reference, absolute value of adjustment width		4.5	5	5.5	dB
Output saturation voltage *1	VoD	Voltage between VOP-VON		2000			mV
Frequency characteristics *1, *2	FcC	-3dB (1MHz reference), λ = 780nm Light input = 40μW (DC) + 20μW (AC)		40	60		MHz
	FcD1	-3dB (1MHz reference), λ = 650nm Light input = 40μW (DC) + 20μW (AC)	Low Middle	60	85		
	FcD2	-3dB (1MHz reference), λ = 650nm Light input = 40μW (DC) + 20μW (AC)	High	50	70		
	FcB1	-3dB (1MHz reference), λ = 405nm Light input = 40μW (DC) + 20μW (AC)	Low Middle	60	85		
	FcB2	-3dB (1MHz reference), λ = 405nm Light input = 40μW (DC) + 20μW (AC)	High	50	70		
Settling time *1	Tset				10	15	ns
Response time *1	Tr, Tf	Vo = 0.9Vp-p, output level 10 to 90% fc = 10MHz, duty = 50%			4	10	ns
Linearity *1	Lin	At output voltage 0.5V and 1.0V (Between VOP-VON)		-1	0	1	%
Light-output voltage temperature dependence Voltage between VOP-VON *1, *3	TC	λ = 780nm, 25°C reference		4	7	10	%
	TD	λ = 650nm, 25°C reference		-3	0	3	%
	TB	λ = 405nm, 25°C reference		-4	-1	2	%

Item with *1 mark indicate the design reference value.

Item with *2 mark indicate the frequency characteristics when VOP and VON are applied individually.

      The frequency characteristics are for the output voltage adjustment range is -5 to +5dB.

Item with *3 mark indicates the temperature dependence for the case of High / Middle / Low gain and for the case when the temperature is 25 to 75°C for the output voltage adjustment range of -5 to +5dB.
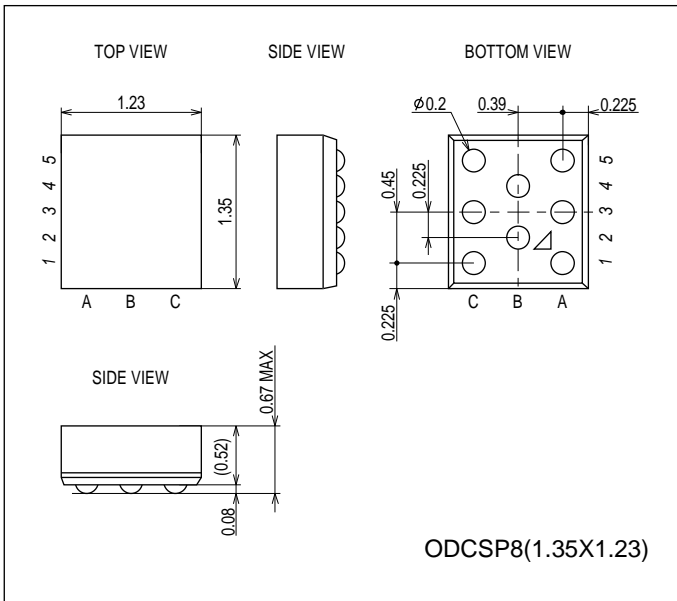

[Expression of output voltage]

      Vn = (sensitivity / 1.78) × 5221 / (5221 - 14 × GCAstep) × light intensity (μW)

Package Dimensions

unit : mm (typ)

3446

TOP VIEW   SIDE VIEW   BOTTOM VIEW

ODCSP8(1.35X1.23)

Pin Assignment

TOP VIEW
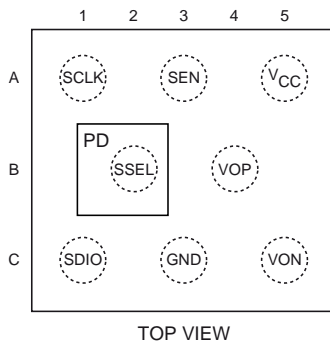
Pin No.	Pin name	Function
A1	SCLK	Serial communication Clock pin
A3	SEN	Serial communication Enable pin
A5	V_{CC}	Power supply voltage pin
B2	SSEL	Register selection pin
		SSEL = Low : Address 00 to 0Fh used
		SSEL = High : Address 10 to 1Fh used
		SSEL = Open : Address 70 to 7Fh used
B4	VOP	Positive side output pin
C1	SDIO	Serial communication Data pin
C3	GND	GND pin
C5	VON	Negative side output pin

PD assignment

1.35

0.615

0.26

Center of chip

Center of PD

PD Size
0.4 × 0.4

1.23

*PD size for reference to be used for design

0.675

(Unit : mm)
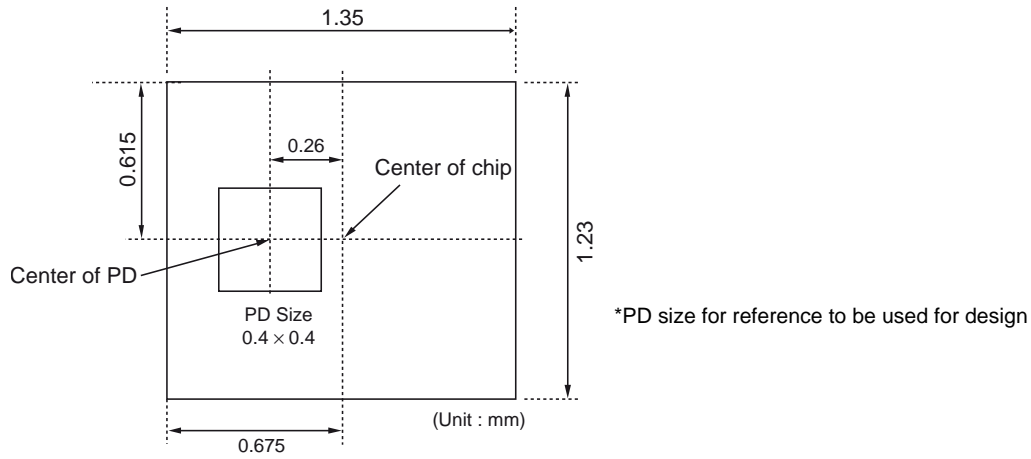
Block diagram and Test circuit diagram

Control

V_{CC}

SEN SCLK SDIO SSEL

Serial

V_{CC}

0.1μF

High
Middle
Low

Vref

Bias
Regulator

−
+
Vref

−
+
Vref

+

−

Vo+

Vo−

20pF

20pF

6kΩ

GND
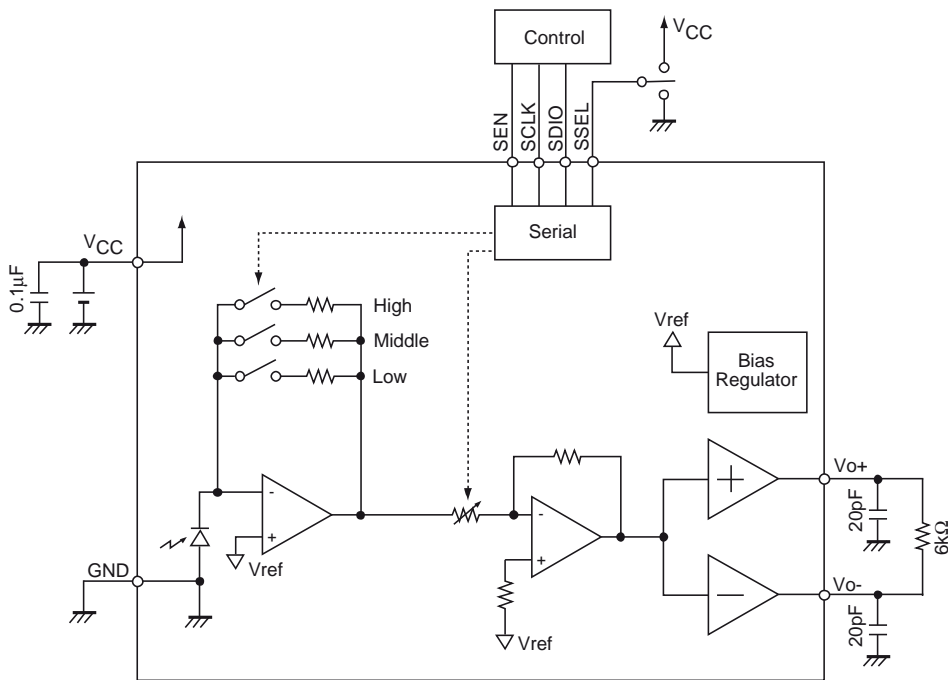
* Please place decoupling capacitors within 3mm from pin

Resister table

Enable selection of the register group from the SSEL pin.

SSEL = Low

	Address	7	6	5	4	3	2	1	0
Name	00h	**POWER**		**IV GAIN SEL**					
Default		00		00		0	0	0	0
Value		11: Power on 00/01/10: Sleep		00/01: High 10: Middle 11: Low					
Name	01h	**GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	0Eh	**TEST1 (*1)**							

SSEL = High

	Address	7	6	5	4	3	2	1	0
Name	10h	**POWER**		**IV GAIN SEL**					
Default		00		00		0	0	0	0
Value		11: Power on 00/01/10: Sleep		00/01: High 10: Middle 11: Low					
Name	11h	**GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	1Eh	**TEST1 (*1)**							

SSEL = Open

	Address	7	6	5	4	3	2	1	0
Name	70h	**POWER**		**IV GAIN SEL**					
Default		00		00		0	0	0	0
Value		11: Power on 00/01/10: Sleep		00/01: High 10: Middle 11: Low					
Name	71h	**GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	7Eh	**TEST1 (*1)**							

*1 TEST1 are either the time when power is applied or "00000000" is set. Do not attempt to change "00000000" during operation.
"00000000" is returned when reading is made.

*2 No problem in terms of operation occurs even when writing is made to the address 02h to 0Dh & 0Fh, 12h to 1Dh & 1Fh and 72h to 7Dh & 7Fh.
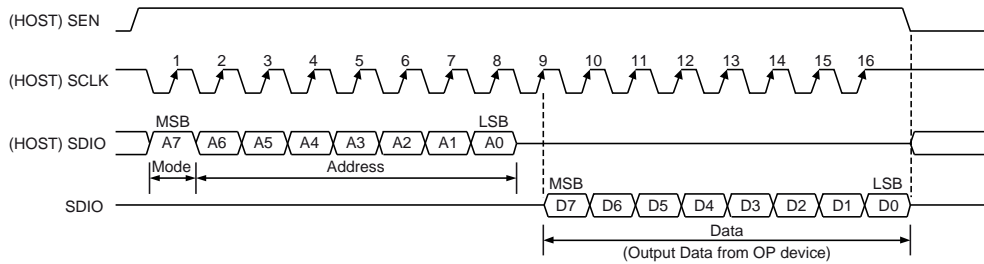"00000000" is returned when this address is read.

*3 When I performed address reading except the register group set by an SSEL terminal, I keep Hi-Z without paying a value.

## Serial protocol

WRITE timing chart
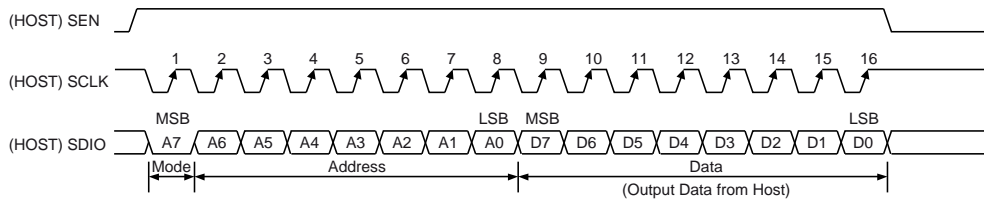
READ timing chart

SDIO pin load / C_L = 20pF. The table below shows the design reference value.

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency Write	f_{SCL}	0		10	MHz
SCL clock frequency Read	f_{SCL}	0		4	MHz
SDIO data setup time	t_{DSU}	50			ns
SDIO data hold time	t_{DHO}	50			ns
SDIO output delay	t_{DDLY}		10	80	ns
SEN "H" period	t_{ENH}	1.6			µs
SEN "L" period	t_{ENL}	200			ns
SCL rise time after SEN rise	t_{STA}	60			ns
SEN fall time after final SCL rise	t_{STO}	100			ns
Serial input "H" voltage	V_IH	2.4		V_{CC}	V
Serial input "L" voltage	V_IL			0.6	V
SDIO output "H" voltage	V_OH	2.5	2.9	3.3	V
SDIO output "L" voltage	V_OL	0	0.3	0.8	V

WRITE
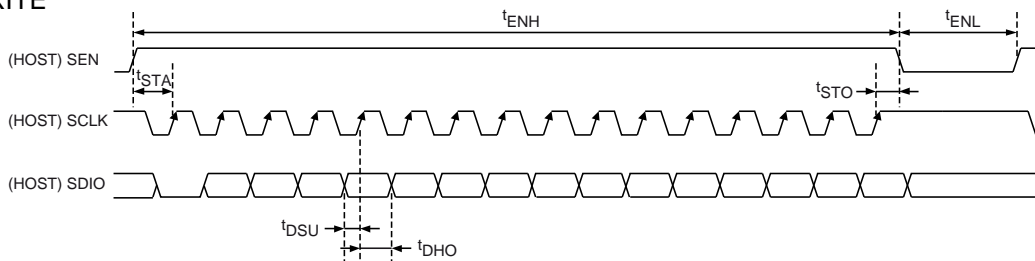
READ
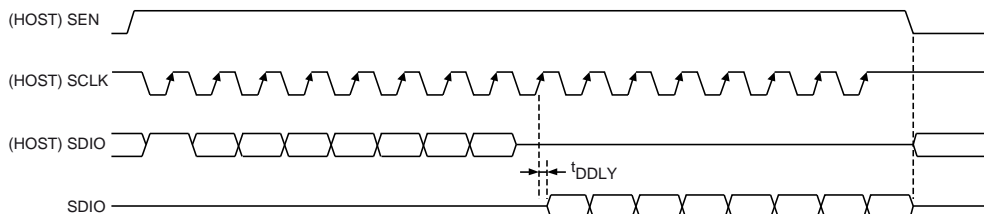
Pin	Type	Equivalent circuit diagram
SDIO	Input Output	
VOP VON	Output	
SCLK SEN	Input	
SSEL	Input	