

HAT1021R

Silicon P Channel Power MOS FET
High Speed Power Switching

HITACHI

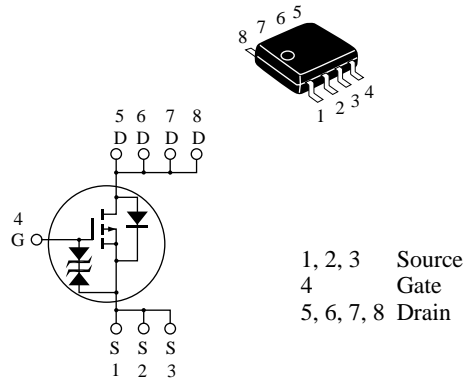
ADE-208-475D (Z)
5th. Edition
Feb. 1999

Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



HAT1021R

Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|--|---------------------------------|-------------|------|
| Drain to source voltage | V_{DSS} | - 20 | V |
| Gate to source voltage | V_{GSS} | ± 10 | V |
| Drain current | I_D | - 5.5 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note1} | - 44 | A |
| Body-drain diode reverse drain current | I_{DR} | - 5.5 | A |
| Channel dissipation | P_{ch} ^{Note2} | 2.5 | W |
| Channel temperature | T_{ch} | 150 | °C |
| Storage temperature | T_{stg} | -55 to +150 | °C |

Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$

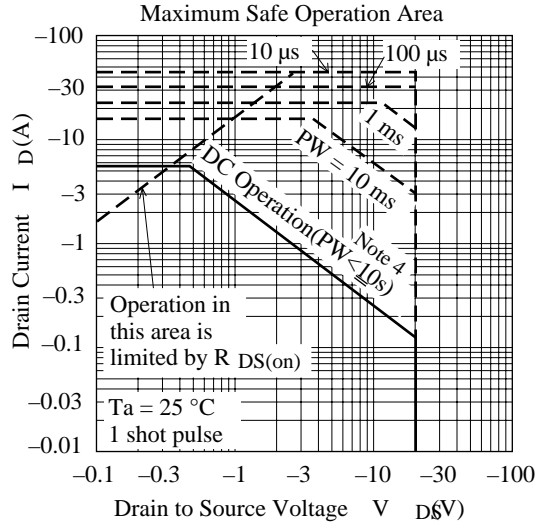
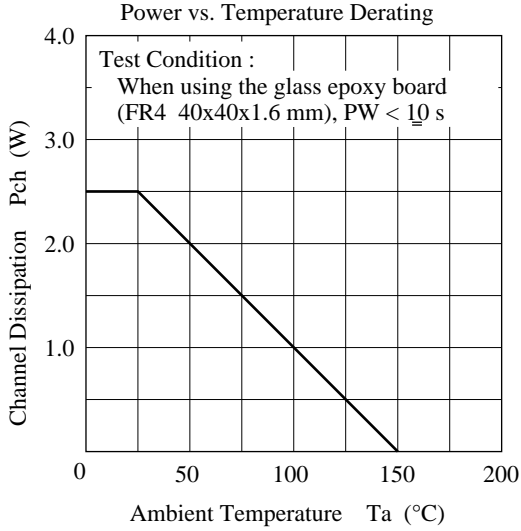
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics (Ta = 25°C)

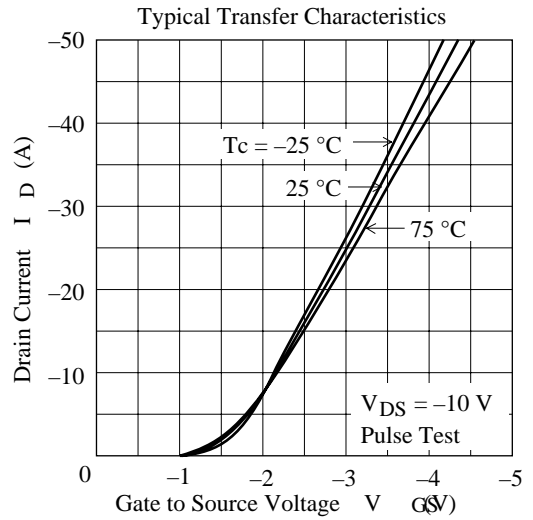
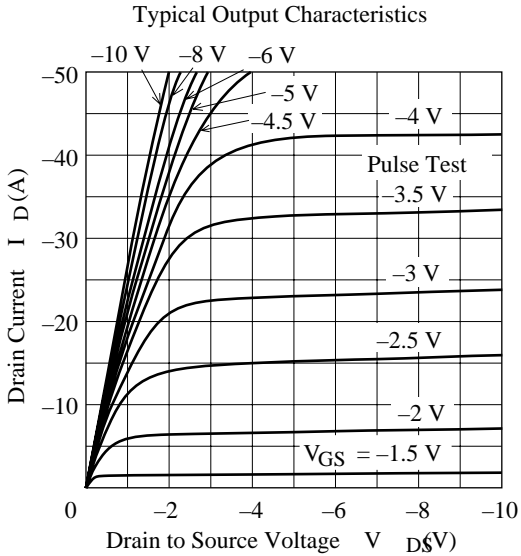
| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|---------------|-------|-------|-------|------|--|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | - 20 | — | — | V | $I_D = -10\text{ mA}$, $V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ± 10 | — | — | V | $I_G = \pm 100\ \mu A$, $V_{DS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 10 | μA | $V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | - 10 | μA | $V_{DS} = -20\text{ V}$, $V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | - 0.5 | — | - 1.5 | V | $V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.048 | 0.060 | Ω | $I_D = -3\text{ A}$, $V_{GS} = -4\text{ V}$ ^{Note3} |
| | $R_{DS(on)}$ | — | 0.065 | 0.085 | Ω | $I_D = -3\text{ A}$, $V_{GS} = -2.5\text{ V}$ ^{Note3} |
| Forward transfer admittance | $ y_{fs} $ | 6 | 9.5 | — | S | $I_D = -3\text{ A}$, $V_{DS} = -10\text{ V}$ ^{Note3} |
| Input capacitance | C_{iss} | — | 1200 | — | pF | $V_{DS} = -10\text{ V}$ |
| Output capacitance | C_{oss} | — | 630 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | C_{rss} | — | 200 | — | pF | $f = 1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 20 | — | ns | $V_{GS} = -4\text{ V}$, $I_D = -3\text{ A}$ |
| Rise time | t_r | — | 120 | — | ns | $V_{DD} \cong -10\text{ V}$ |
| Turn-off delay time | $t_{d(off)}$ | — | 175 | — | ns | |
| Fall time | t_f | — | 140 | — | ns | |
| Body-drain diode forward voltage | V_{DF} | — | - 0.9 | - 1.4 | V | $I_F = -5.5\text{ A}$, $V_{GS} = 0$ ^{Note3} |
| Body-drain diode reverse recovery time | t_{rr} | — | 65 | — | ns | $I_F = -5.5\text{ A}$, $V_{GS} = 0$ $diF/dt = 20\text{ A}/\mu s$ |

Note: 3. Pulse test

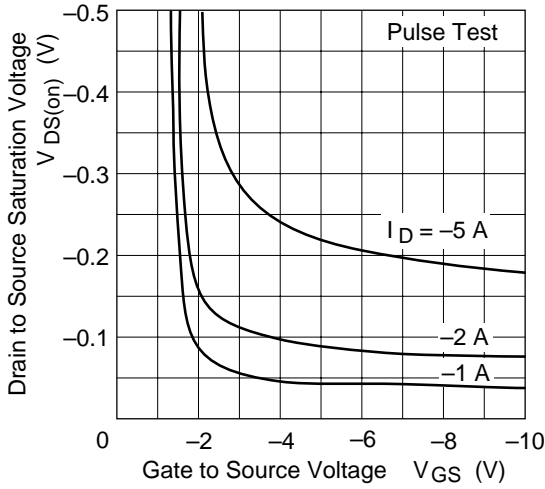
Main Characteristics



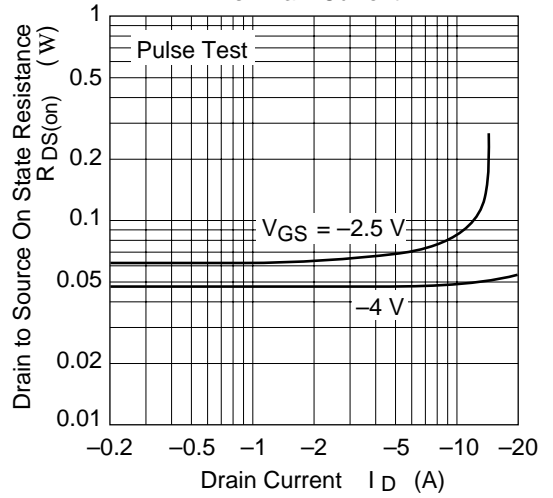
Note 4 :
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)



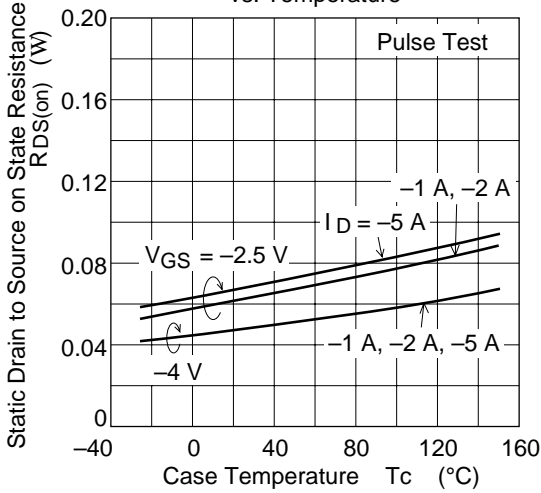
Drain to Source Saturation Voltage vs. Gate to Source Voltage



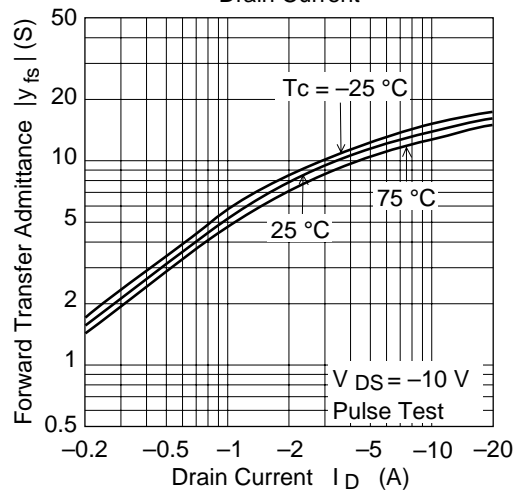
Static Drain to Source on State Resistance vs. Drain Current



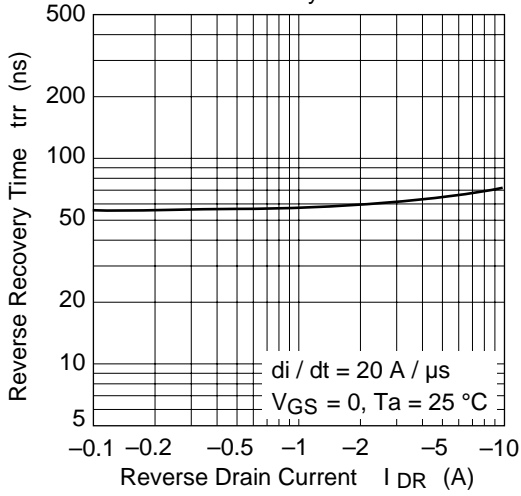
Static Drain to Source on State Resistance vs. Temperature



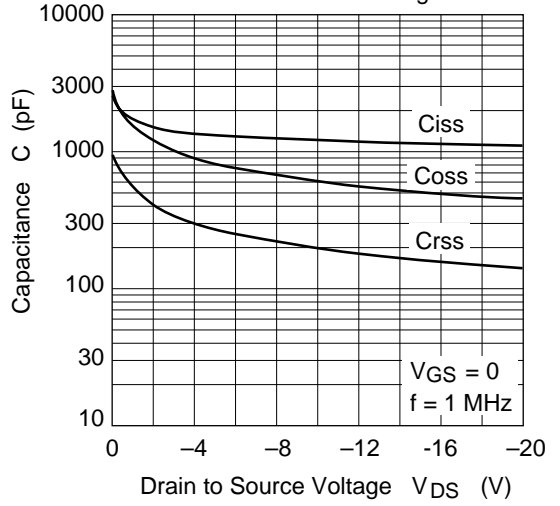
Forward Transfer Admittance vs. Drain Current



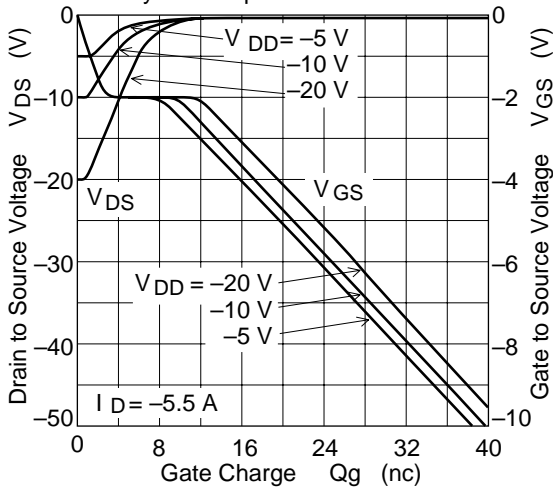
Body-Drain Diode Reverse Recovery Time



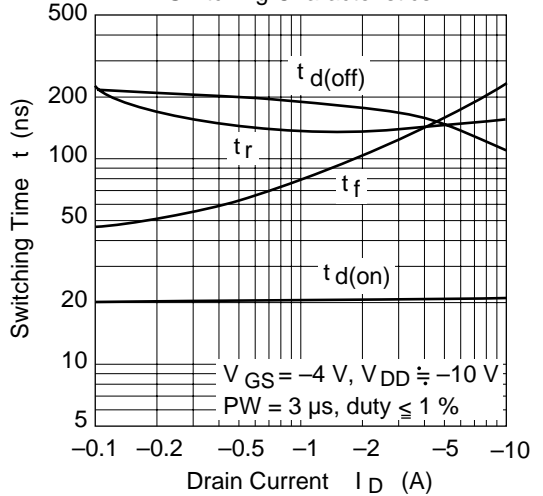
Typical Capacitance vs. Drain to Source Voltage

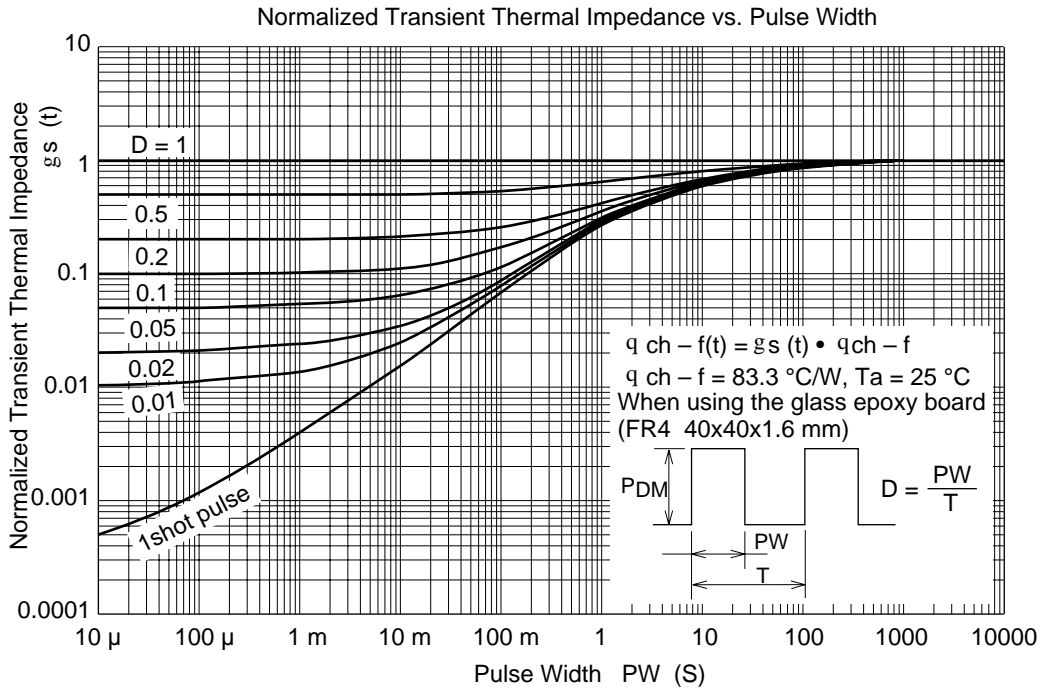
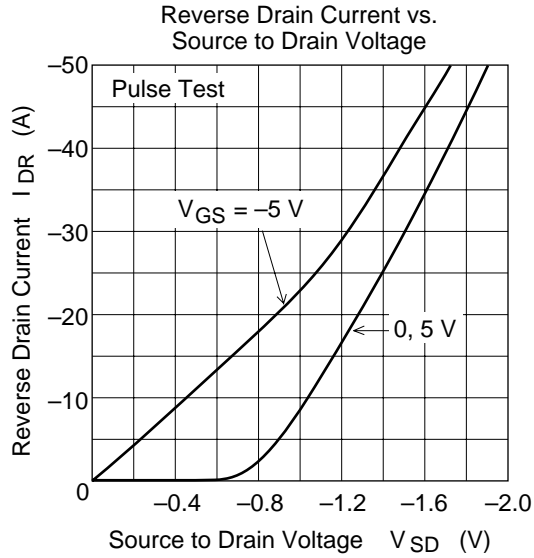


Dynamic Input Characteristics

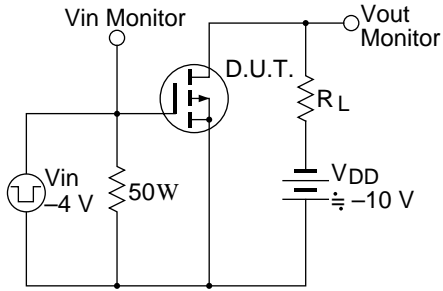


Switching Characteristics

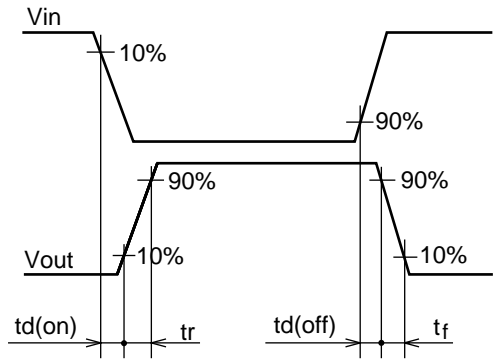




Switching Time Test Circuit



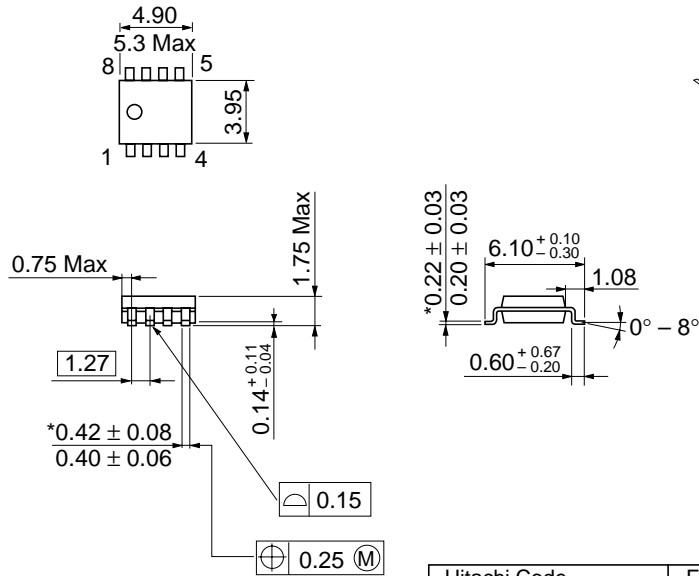
Switching Time Waveform



Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | FP-8DA |
| JEDEC | Conforms |
| EIAJ | — |
| Mass (reference value) | 0.085 g |

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