

4-bit Single Chip Microcomputer



- Core CPU Architecture
- Dot Matrix LCD Driver
- Programmable SVD Circuit/Sound Generator

■ DESCRIPTION

The E0C624A is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 4-bit core CPU. The chip contains the ROM, RAM, dot matrix LCD driver, programmable SVD circuit, time base counter and clock synchronous serial port.

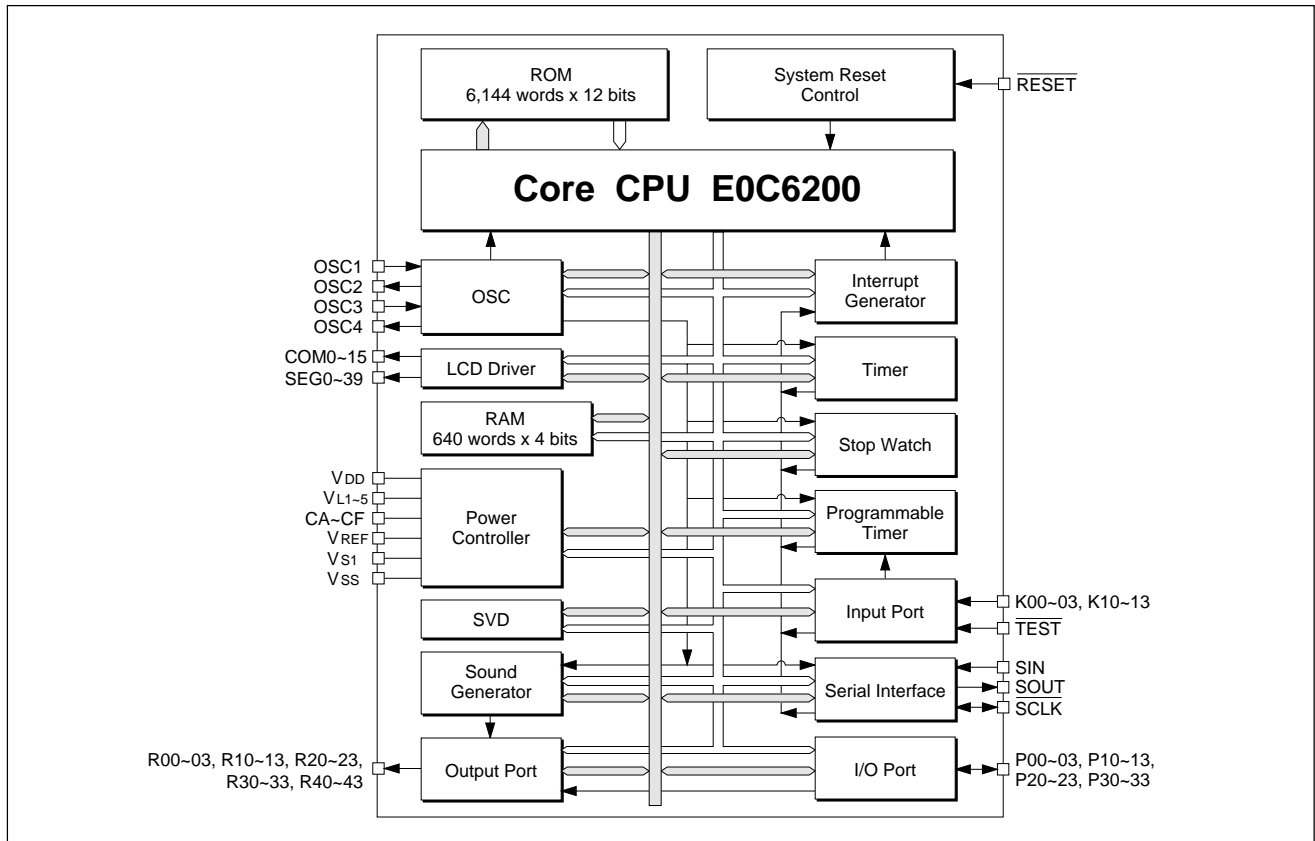
Interfacing with the external memory, the E0C624A can be applied to any system requiring large memory such as schedule reminder, and dot matrix display function.

■ FEATURES

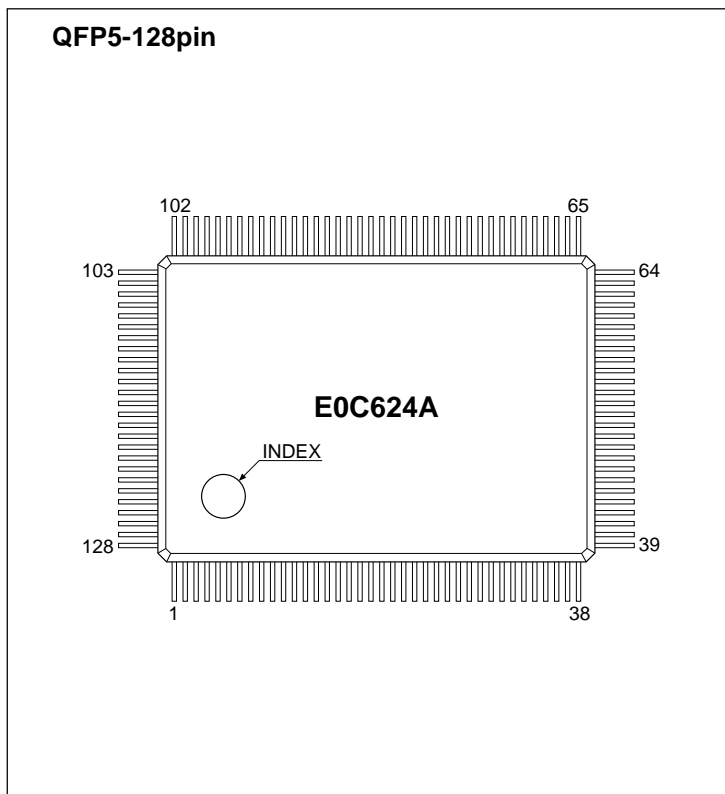
- CMOS LSI 4-bit parallel processing
- Clock 32.768kHz/2MHz (Max.) (selectable by software)
- Instruction set 108 instructions
- Instruction cycle time 153μsec, 214μsec or 366μsec at 32kHz
(depending on instruction)
5μsec, 7μsec or 12μsec at 1MHz
(depending on instruction)
- ROM capacity 6,144 × 12 bits
- RAM capacity 640 × 4 bits
- External memory capacity Read/Write 512K bits (Max.)
Read only 1M bits (Max.)
- Input port 8 bits (pull-up resistors are available by mask option)
- Output port 20 bits (clock output or buzzer output is available by mask option)
- I/O port 16 bits (pull-up resistors are available by mask option)
- Serial I/O port 1 port (clock sync.)
- Dot matrix LCD driver 40 segments × 8 commons/40 segments × 16 commons
(1/8 or 1/16 duty is selectable by mask option)
- Built-in SVD circuit 2.3V/2.6V/3.3V/4.5V programmable
- Built-in stopwatch timer
- Built-in watchdog timer
- Built-in time base counter 3 lines
- Interrupts External : Input interrupt 2 lines
Internal : Timer interrupt 3 lines
Serial I/O interrupt 1 line
- Built-in sound generator With digital envelope (8 sounds programmable)
- Supply voltage 2.2V to 5.5V
- Current consumption HALT mode (32kHz) : 2.5μA (Typ.)
OPERATING mode (1MHz) : 400μA (Typ.)
- Package QFP5-128pin (plastic)
Die form

E0C624A

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



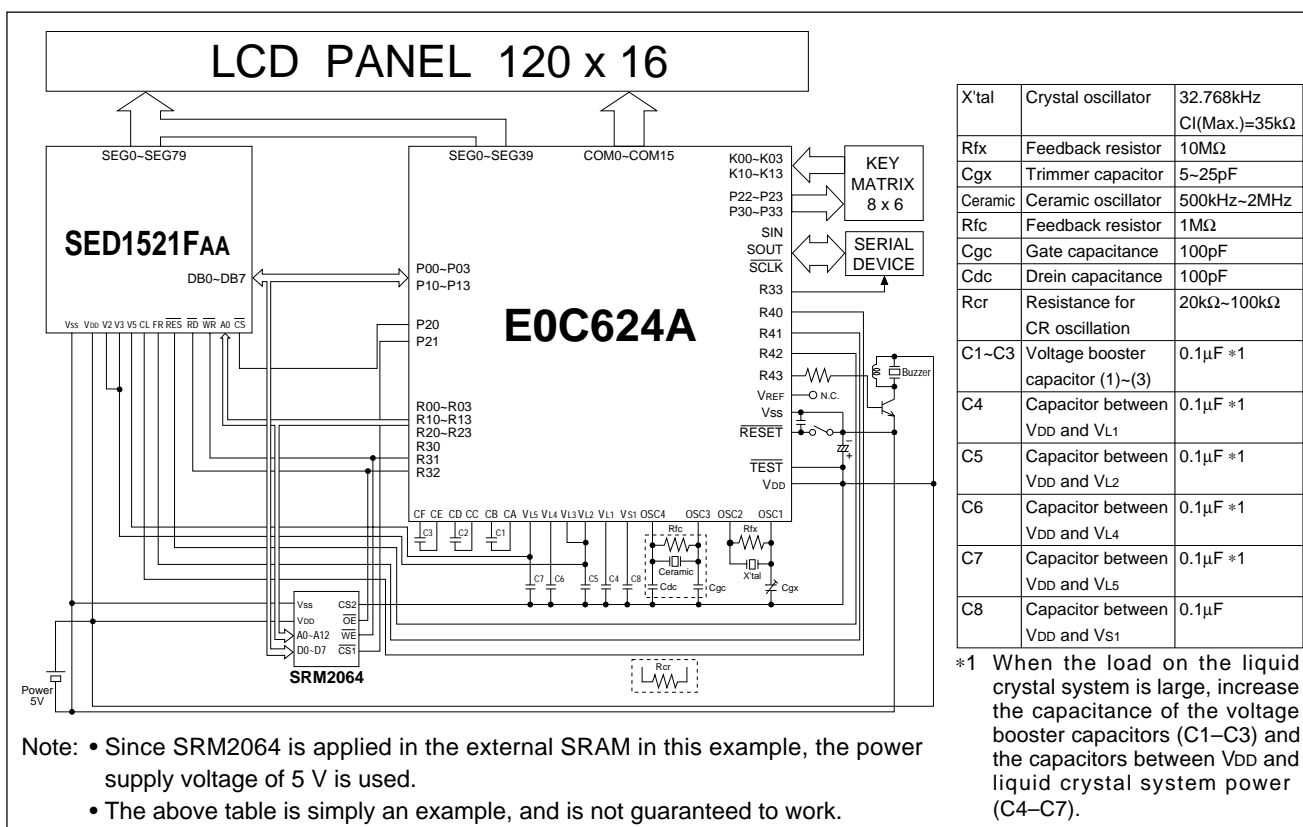
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VL3	33	SEG33	65	SEG2	97	R42
2	VL4	34	N.C.	66	SEG1	98	N.C.
3	VL5	35	SEG32	67	SEG0	99	R41
4	CF	36	SEG31	68	SCLK	100	R40
5	N.C.	37	SEG30	69	N.C.	101	R33
6	CE	38	SEG29	70	SOUT	102	R32
7	CD	39	SEG28	71	SIN	103	R31
8	CC	40	SEG27	72	K13	104	R30
9	CB	41	SEG26	73	K12	105	R23
10	CA	42	SEG25	74	K11	106	R22
11	COM0	43	SEG24	75	K10	107	R21
12	COM1	44	SEG23	76	K03	108	R20
13	COM2	45	SEG22	77	K02	109	R13
14	COM3	46	SEG21	78	K01	110	R12
15	COM4	47	SEG20	79	K00	111	R11
16	COM5	48	SEG19	80	P33	112	R10
17	COM6	49	SEG18	81	P32	113	R03
18	COM7	50	SEG17	82	P31	114	R02
19	COM8	51	SEG16	83	P30	115	R01
20	COM9	52	SEG15	84	P23	116	R00
21	COM10	53	SEG14	85	P22	117	VSS
22	COM11	54	SEG13	86	P21	118	RESET
23	COM12	55	SEG12	87	P20	119	TEST
24	COM13	56	SEG11	88	P13	120	OSC4
25	COM14	57	SEG10	89	P12	121	OSC3
26	COM15	58	SEG9	90	P11	122	Vs1
27	SEG39	59	SEG8	91	P10	123	OSC2
28	SEG38	60	SEG7	92	P03	124	OSC1
29	SEG37	61	SEG6	93	P02	125	VDD
30	SEG36	62	SEG5	94	P01	126	VREF
31	SEG35	63	SEG4	95	P00	127	VL1
32	SEG34	64	SEG3	96	R43	128	VL2

N.C. = No Connection

PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
VDD	125	I	Power source (+) terminal
VSS	117	I	Power source (-) terminal
Vs1	122	-	Oscillation and internal logic system regulated voltage
VL1-VL5	127, 128, 1-3	-	LCD system power (1/4 or 1/5 bias may be selected by mask option)
VREF	126	O	LCD system power test terminal
CA-CF	10-6, 4	-	Booster capacitor connecting terminal
OSC1	124	I	Crystal oscillation input terminal
OSC2	123	O	Crystal oscillation output terminal
OSC3	121	I	Ceramic or CR oscillation input terminal (selected by mask option)
OSC4	120	O	Ceramic or CR oscillation output terminal (selected by mask option)
K00-K03, K10-K13	79-72	I	Input terminal (Use of pull up resistor is selected by mask option)
P00-P03, P10-P13	95-88	I/O	I/O terminal (Setting for data bus may be selected by mask option)
P20-P23	87-84	I/O	I/O terminal (CS output may be selected by mask option)
P30-P33	83-80	I/O	I/O terminal
R00-R03, R10-R13 R20-R23, R30	116-104	O	Output terminal (Setting for address bus may be selected by mask option)
R31	103	O	Output terminal (DC, address or \overline{WR} output may be selected by mask option)
R32	102	O	Output terminal (DC or \overline{RD} output may be selected by mask option)
R33	101	O	Output terminal (DC or \overline{SRDY} output may be selected by mask option)
R40	100	O	Output terminal (DC, CL or \overline{FOUT} output may be selected by mask option)
R41	99	O	Output terminal (DC or FR output may be selected by mask option)
R42	97	O	Output terminal (DC, BZ or FOUT output may be selected by mask option)
R43	96	O	Output terminal (DC or BZ output may be selected by mask option)
SIN	71	I	Serial interface input terminal
SOUT	70	O	Serial interface output terminal
SCLK	68	I/O	Serial interface clock input/output terminal
SEG0-39	67-35, 33-27	O	LCD segment output terminal
COM0-15	11-26	O	LCD common output terminal
RESET	118	I	Initial reset input terminal
TEST	119	I	Test input terminal

BASIC EXTERNAL CONNECTION DIAGRAM



E0C624A

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-7.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _{IOsc}	V _{S1} - 0.3 to 0.5	V
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *1	P _D	250	mW

*1: In case of plastic package (QFP5-128pin).

● Recommended Operating Conditions

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	
Supply voltage	V _{SS}	V _{DD} =0V	V _{SC} ="0"	-3.8	-3.0	-1.8	V
			V _{SC} ="1"	-5.5	-3.0	-2.2	V
			V _{SC} ="2"	-5.5	-3.0	-3.5	V
Oscillation frequency (1)	fosc1		20	32.768	50	kHz	
Oscillation frequency (2)	fosc3	V _{SC} ="1"	50	1,000	1,200	kHz	
Oscillation frequency (3)	fosc3	V _{SC} ="2"	50	2,000	2,300	kHz	
Voltage booster capacitor (1)	C1			0.1		μF	
Voltage booster capacitor (2)	C2			0.1		μF	
Voltage booster capacitor (3)	C3			0.1		μF	
Capacitor between V _{DD} and V _{L1}	C4			0.1		μF	
Capacitor between V _{DD} and V _{L2}	C5			0.1		μF	
Capacitor between V _{DD} and V _{L4}	C6			0.1		μF	
Capacitor between V _{DD} and V _{L5}	C7			0.1		μF	
Capacitor between V _{DD} and V _{S1}	C8			0.1		μF	

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, fosc1=32.768kHz, fosc3=1MHz, T_a=25°C, C1-C8=0.047μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V _{HIN}	V _{SS} =-2.2 to -5.5V	0.2•V _{SS}		0	V
Low level input voltage	V _{LIN}	T _a =25°C	V _{SS}		0.8•V _{SS}	V
High level input voltage	V _{HIN}	V _{SS} =-2.2 to -5.5V	-0.2		0	V
Low level input voltage	V _{LIN}	T _a =25°C	V _{SS}		V _{SS} +0.2	V
High level input current	I _{IH}	V _{SS} =-3.0V V _{IH} =0V	0		0.5	μA
Low level input current (1)	I _{IL1}	V _{SS} =-3.0V V _{IL1} =V _{SS} With pull-up resistor	-45		-15	μA
Low level input current (2)	I _{IL2}	V _{SS} =-3.0V V _{IL2} =V _{SS} No pull-up resistor	-0.5		0	μA
High level output current (1)	I _{OH1}	V _{SS} =-2.2V V _{OH1} =-0.5V			-1.0	mA
Low level output current (1)	I _{OL1}	V _{SS} =-2.2V V _{OL1} =V _{SS} +0.5V	4.0			mA
High level output current (2)	I _{OH2}	V _{SS} =-2.2V V _{OH2} =-0.5V			-2.0	mA
Low level output current (2)	I _{OL2}	V _{SS} =-2.2V V _{OL1} =V _{SS} +0.5V	8.0			mA
Common output current	I _{OH3}	V _{OH3} =-0.05V			-30	μA
	I _{OL3}	V _{OL3} =V _{L5} +0.05V	30			μA
Segment output current	I _{OH4}	V _{OH4} =-0.05V			-10	μA
	I _{OL4}	V _{OL4} =V _{L5} +0.05V	10			μA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{osc1}=32.768kHz, f_{osc3}=1MHz, T_a=25°C, C₁-C₈=0.047μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Liquid crystal drive voltage (Normal mode)	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (No panel load)	1/2•V _{L2} -0.1		1/2•V _{L2} ×0.95	V	
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (No panel load)	LC="0"	Typ.×1.12	-1.80	Typ.×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
LC="14"	-2.53						
LC="15"	-2.59						
V _{L4}	Connect 1MΩ load resistor between V _{DD} and V _{L4} (No panel load)	3/2•V _{L2}		3/2•V _{L2} ×0.95	V		
V _{L5}	Connect 1MΩ load resistor between V _{DD} and V _{L5} (No panel load)	2•V _{L2}		2•V _{L2} ×0.95	V		
Liquid crystal drive voltage (Heavy load protection mode)	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (No panel load)	LC="0"	Typ.×1.12	-0.92	Typ.×0.88	V
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"		-1.11		
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
	LC="14"	-1.29					
LC="15"	-1.32						
V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (No panel load)	2•V _{L1}		2•V _{L1} ×0.90	V		
V _{L4}	Connect 1MΩ load resistor between V _{DD} and V _{L4} (No panel load)	3•V _{L1}		3•V _{L1} ×0.90	V		
V _{L5}	Connect 1MΩ load resistor between V _{DD} and V _{L5} (No panel load)	4•V _{L1}		4•V _{L1} ×0.90	V		
SVD voltage	V _{SVD0}	SVC="0"	-2.35	-2.20	-2.05	V	
	V _{SVD1}	SVC="1"	-2.70	-2.50	-2.30	V	
	V _{SVD2}	SVC="2"	-3.30	-3.10	-2.90	V	
	V _{SVD3}	SVC="3"	-4.50	-4.20	-3.90	V	
SVD circuit response time	t _{sVD}			100	μS		
Current consumption	I _{hlt}	During HALT	No panel load *1	2.5	5.0	μA	
	I _{EX1}	During operation at 32kHz		6.5	9.0	μA	
	I _{EX2}	During operation at 1MHz	No panel load *2	400	600	μA	
	I _{EX3}	During operation at 2MHz	No panel load *3	1,000	1,500	μA	

*1: SVD circuit: OFF status, VSC = "0", OSC1: oscillating with crystal, OSCC = "0"

*2: SVD circuit: OFF status, VSC = "1", OSC1: oscillating with crystal

*3: SVD circuit: OFF status, VSC = "2", OSC1: oscillating with crystal, V_{SS} = -5.0V

E0C624A

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Crystal: C-002R ($C_1=35k\Omega$), $C_{GX}=25pF$, C_{DX} =built-in, $R_{FX}=10M\Omega$, $V_{SC}="0"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			5	Sec
Built-in capacitance (drain)	C_D	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	$C_G=5pF$			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD} , V_{S1}	200			$M\Omega$

OSC3 CR oscillation circuit (1)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $V_{SC}="1"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-5		5	%
Oscillation frequency	f_{CR}	$R_{osc}=40k\Omega$	$860 \times 70\%$	860	$860 \times 130\%$	kHz

OSC3 CR oscillation circuit (2)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-5.0V$, $V_{SC}="2"$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-3.5$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-3.5$ to $-5.5V$	-5		5	%
Oscillation frequency	f_{CR}	$R_{osc}=20k\Omega$	$1.7 \times 70\%$	1.7	$1.7 \times 130\%$	MHz

OSC3 ceramic oscillation circuit (1)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $V_{SC}="1"$, Ceramic: CSB 1000J (Murata Mfg. Co.), $C_{GC}=C_{DC}=100pF$, $R_{FC}=1M\Omega$, $T_a=25^\circ C$)

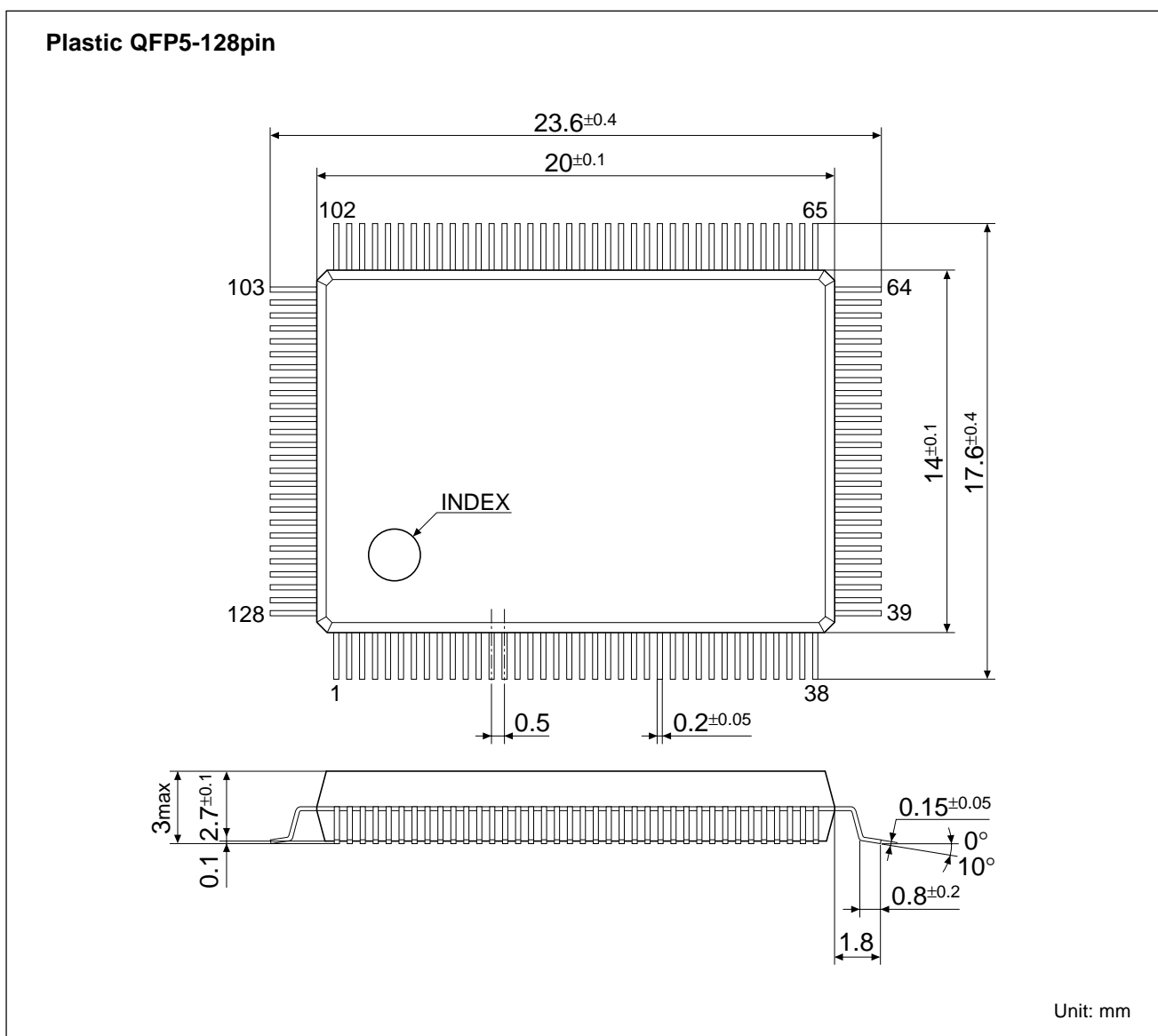
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-2.2$ to $-5.5V$	-3		3	%

OSC3 ceramic oscillation circuit (2)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-5.0V$, $V_{SC}="2"$, Ceramic: CSA 2.00MG (Murata Mfg. Co.), $C_{GC}=C_{DC}=100pF$, $R_{FC}=1M\Omega$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	$V_{SS}=-3.5$ to $-5.5V$			3	mS
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-3.5$ to $-5.5V$	-3		3	%

■ PACKAGE DIMENSIONS



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SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department II (Asia)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

