aptek technologies

AMS 3201
DTMF Receiver

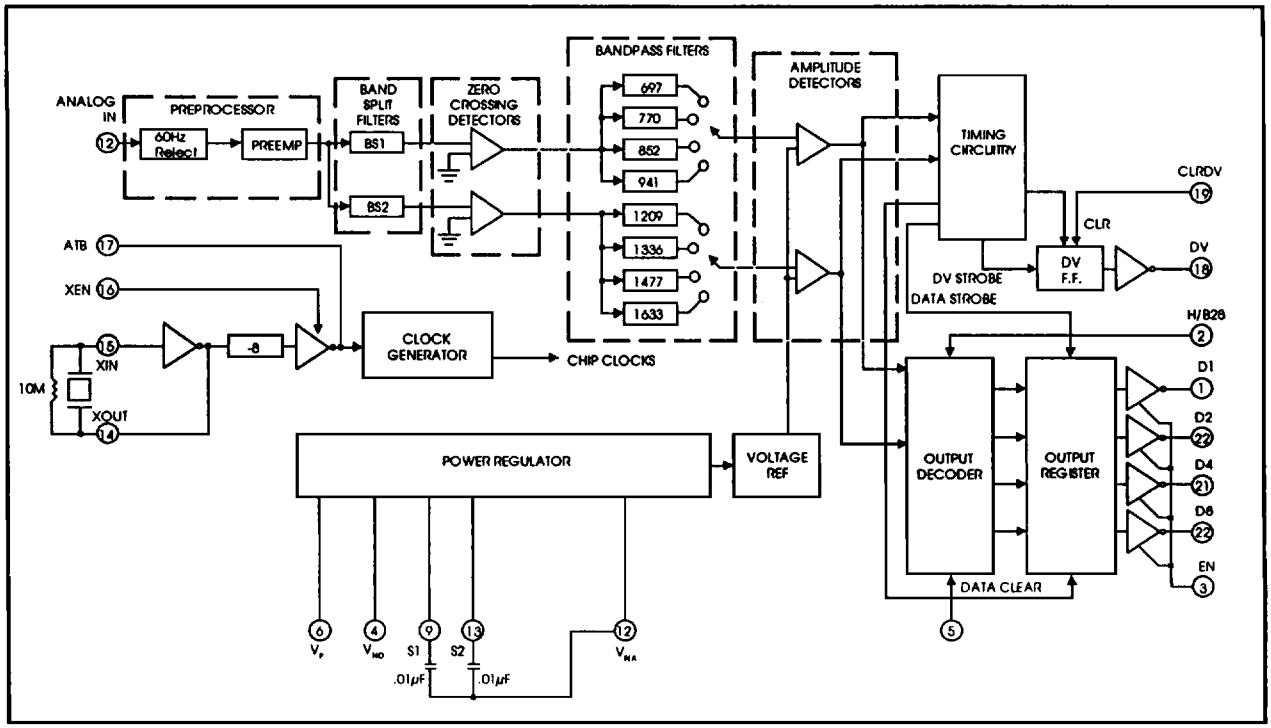
Central Office quality integrated DTMF receiver

DESCRIPTION

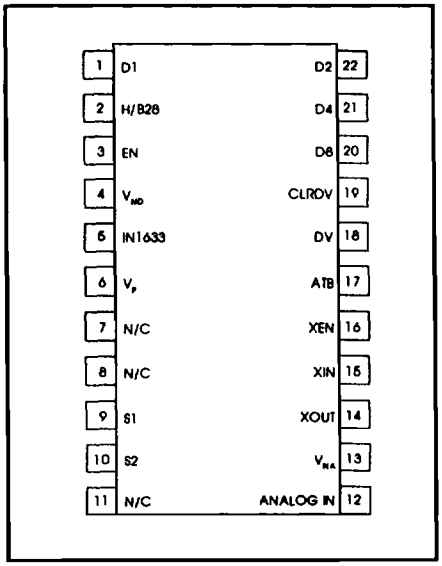
A complete Dual Tone Multi-Frequency receiver, the AMS 3201 features a monolithic integrated circuit fabricated with low-power CMOS processing. It requires only a single low-tolerance voltage supply. The only external components needed are an inexpensive 3.58MHz TV "colorburst" crystal (for frequency reference) and two non-critical bypass capacitors. The outputs interface with standard CMOS circuitry, and are three state enabled to facilitate bus-oriented architectures.

FEATURES

- Central office quality
- Excellent speech immunity
- Synchronous or handshake interface
- No front-end band-splitting filters needed
- Output in 4-bit hexidecimal code, or binary coded 2 of 8
- Detects either 12 or 16 standard DTMF signals
- Inexpensive TV "colorburst" crystal for reference
- Three-stage outputs
- Single 12V supply



PINOUT DRAWING



PIN	NAME	DESCRIPTION
1	D1	Digital outputs. See D2, D4, D8 below
2	H/B28	Code Select. When tied to VP, output on D8-D1 is hexidecimal; when tied to VND, output is binary coded 2 of 8. Truth table shows the codes on D8-D1
3	EN	Output Enable. When pin is a logic high, output codes on D8-D1 are enabled. When a logic low, outputs D8-D1 assume high impedance state
4	VND	Digital Negative Supply Voltage (ground). See pin 13
5	IN1633	Inhibit 1633. When pin is a logic high, 3201 will detect only digits 0-9, #and *. When a logic low, the 3201 will detect all 16 tone pair combinations
6	VP	Positive supply voltage
7	NC	
8	NC	
9	S1	These pins must be bypassed to VNA with 0.01μF ± 20% capacitors
10	S2	
11	NC	
12	ANALOG IN	Internally biased so the input signal may be AC coupled. Input may be a DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 2
13	VNA	Analog negative supply voltage. The analog (VNA) and digital (VND) supplies are brought out separately to enhance analog noise immunity on the chip. VNA and VND should be connected externally as shown in Figure 4
14	XIN	Crystal Out, 3.579 MHz crystal connected from pin 14to pin 15
15	XIN	Crystal In (Tie to VP if external oscillator is used)
16	XEN	Enable Internal Oscillator. Tie to VP if crystal is used, tie to VND if external oscillator is used (See Figure 3)
17	ATB	Alternate Time Base. If XEN = H, ATB is clock output. If XEN =L, ATB is clock input from other 3201
18	DV	Data Valid. Indicates tone burst has been detected by going to high logic level. Will remain high until tone is removed or CLRDV is pulsed high
19	CLRDV	Clear Data Valid. Pulsing this pin to a high logic level will reset DV
20	D8	Digital outputs. With D1 (above) provide a coded representation of the signal received when DV is high. Code is selected by H/B28 (pin 2)
21	D4	
22	D2	

FUNCTIONAL DESCRIPTION

The AMS 3201 accepts standard DTMF frequencies normally generated by a pushbutton telephone and produces an output directly compatible with standard CMOS. The input signal is received on ANALOG IN, which provides a minimum input impedance of 10KOhms. The circuit provides bandsplit, tone detection and timing functions for the input signal, produces the output code selected by H/B28, and raises DV, signifying that a tone is present and output data levels are valid.

Data output pins D8-D1 may be made high impedance for tri-state bus operation by taking signal EN to a logic low. CLRDV can reset DV until a new tone is detected by pulsing to a logic high. Or with CLRDV low, DV will return to a low state when the 3201 detects that the valid tone pair is no longer present.

Multiple devices may be operated from one crystal through use of XEN and ATB. The first is operated with a crystal attached to XIN and XOUT, with XEN tied to V_P. This causes ATB to be a clock output. Other devices using the same crystal have XEN tied low, XIN high, and ATB as an input for the clock signal generated by the single crystal.

Digital and analog functions are combined on the same CMOS chip. The analog input is pre-processed by 60Hz reject and band-splitting filters, then hard-limited to provide AGC. Eight band-pass filters detect the individual tones. A digital post-processor times them and provides correctly coded digital outputs.

OUTPUT TRUTH TABLE

Digit	H/B28 = H				H/B28 = L			
	D8	D4	D2	D1	D8	D4	D2	D1
1	L	L	L	H	L	L	L	L
2	L	L	H	L	L	L	L	H
3	L	L	H	H	L	L	H	L
4	L	H	L	L	L	H	L	L
5	L	H	L	H	L	H	L	H
6	L	H	H	L	L	H	H	L
7	L	H	H	H	H	L	L	L
8	H	L	L	L	H	L	L	H
9	H	L	L	H	H	L	H	L
0	H	L	H	L	H	H	L	H
*	H	L	H	H	H	H	L	L
#	H	H	L	L	H	H	H	L
A	H	H	L	H	L	L	H	H
B	H	H	H	L	L	H	H	H
C	H	H	H	H	H	L	H	H
D	L	L	L	L	H	H	H	H

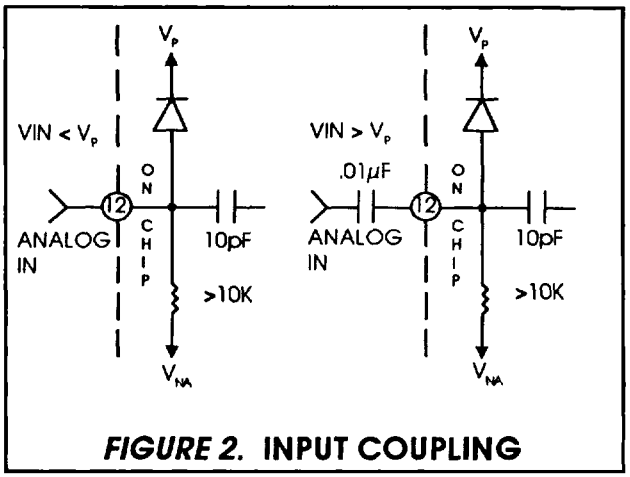


FIGURE 2. **INPUT COUPLING**

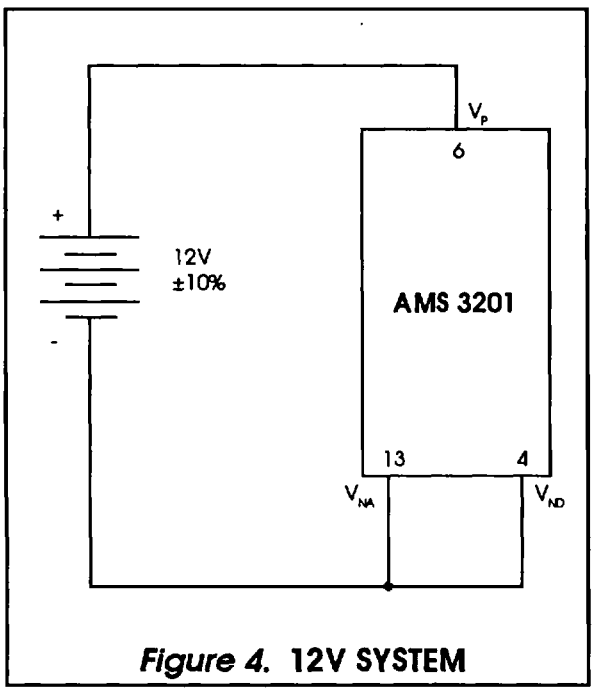


Figure 4. **12V SYSTEM**

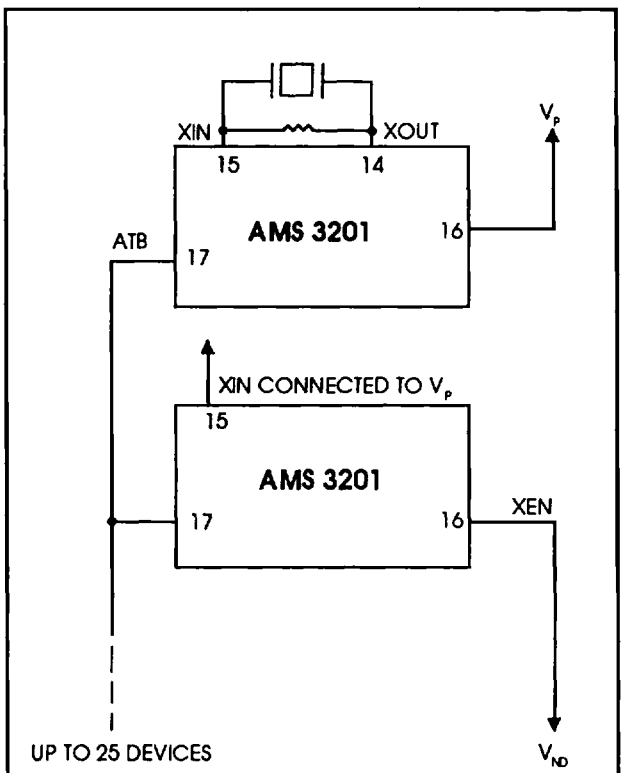


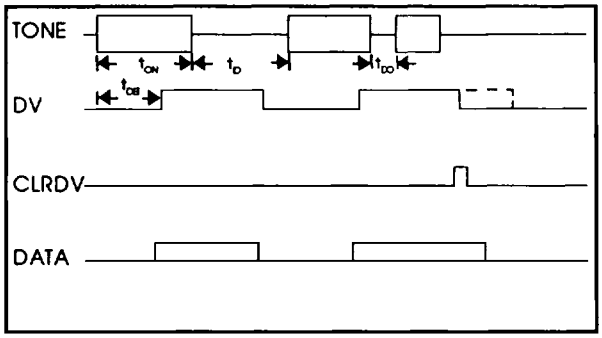
FIGURE 3. **CRYSTAL CONNECTION**

ABSOLUTE MAXIMUM RATINGS

(all voltages referred to VND) Operation above absolute Maximum ratings may permanently damage device

RATING	MIN	MAX	UNITS
Supply Voltage		14	Volts
Analog Input Voltage	V_P - 22	V_P + 0.5	Volts
Digital Input Voltage	V_P + 0.5	V_{ND} - 0.5	Volts
DC Current Into Any Input		± 1.0	mA
Operating Temperature Range	0	70	°C
Storage Temperature	-65	150	°C
Lead Temperature (Soldering 10 sec.)		300	°C
Power Dissipation		1	Watt

TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Test Conditions TA = 0° - 70°C, VP - VND = 12V, Unless otherwise Specified

Parameter	Symbol	Min	Typ	Max	Units	Notes
Operating Voltage	V_P-V_{ND}	10.8	12	13.2	V	
Operating Supply	I_P		13	20	mA	
Digital Output Low Level	V_{OL}	0		0.5	V	I_O=-1mA D1-D8, DV, ATB
Digital Output High Level	V_{OH}	11.5		12	V	I_O=1mA D1-D8, DV, ATB
Digital Input Low Level	V_{IL}	0		3.6	V	CLRDV, IN1633, ATB, EN
		0		1.0	V	H/B28,XEN
Digital Input High Level	V_{IH}	8.4		12		
3-State Output Leakage	I_{OS}		±10-4	±10	µADC	EN=LOW

AC ELECTRICAL AND TIMING PARAMETERS

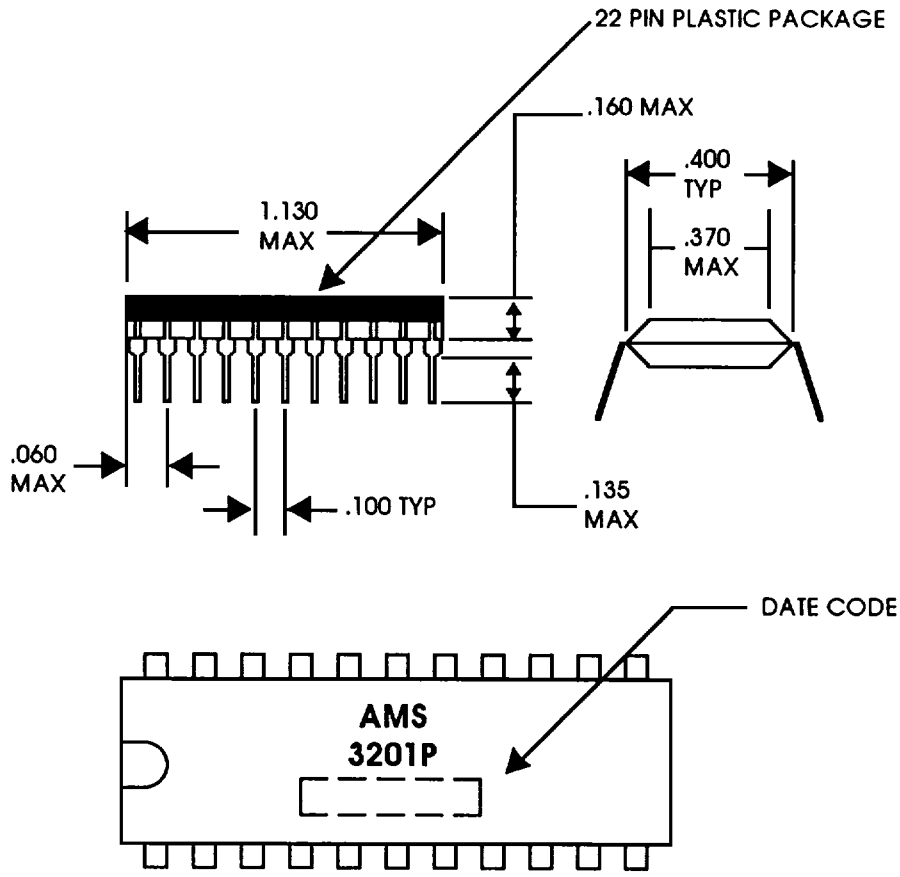
Unless Otherwise Specified TA = 0° - 70°C, VP- VNA = 12V ± 10%

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Valid Signal Level		-24		+6	dBm	Referred to 600 ohms each tone
Signal Noise Ratio		12			dB	Note 1
Working Twist (V_L / V_H)		-4		+8	dB	
Recognition Bandwidth		±(1.5%+2) Hz	±2.3 %	±3.5 %	Hz	Relative to Center Frequency
Dial Tone Tolerance		0			dB	Relative to input tone level, Note 2
60 Hz Tolerance				2	Vrms	
Must Detect Tone burst	t_{ON}	40			mSec	
Must Detect Pause	t_D	40			mSec	
Must not Detect Pause	t_{DO}			20	mSec	
Minimum Detection Time	t_{DET}			20	mSec	
Power Supply Noise Tolerance		25			mVp-p	
Input Impedance		10			KOhm	
Peak Input Voltage		Vp-22		Vp+0.5	V	

Notes:

1. Band limited white noise (300Hz - 3400Hz) tone burst 50 ms on 50 ms off
2. For dial tone frequencies 350-440Hz

PACKAGE OUTLINE



NOTE: COUNTRY OF ORIGIN LOCATED ON UNDER-SIDE OF DEVICE

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