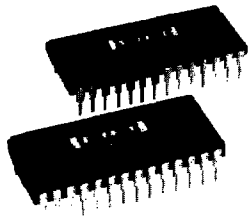
BURR-BROWN®



ADS807
ADS808

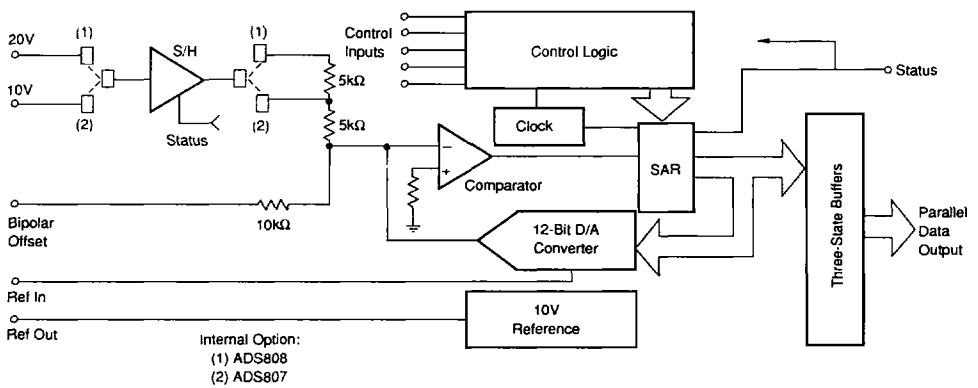
12-Bit Resolution Sampling A/D CONVERTER WITH MICROPROCESSOR INTERFACE

FEATURES

- 100ksps SAMPLING RATE
- DC SPECS:
  1/2LSB Integral Linearity Error
  1 LSB Differential Linearity Error
- AC SPECS:
  82dB Spurious-Free Dynamic Range
  72dB Signal-to-Noise Ratio
  80dB Total Harmonic Distortion
  75dB Two-Tone Intermodulation Distortion
- INTERNAL SAMPLE/HOLD, REFERENCE & CLOCK
- PIN COMPATIBLE WITH INDUSTRY STANDARD ADC574, ADC674, ADC774 A/D CONVERTERS
- POWER DISSIPATION: 660mW
- 28-PIN CERAMIC DIP

APPLICATIONS

- HIGH SPEED DATA ACQUISITION
- SPECTRUM ANALYSIS
- SPEECH SYNTHESIS AND RECOGNITION
- DSP PROCESS AND MOTION CONTROL



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-855A

DESCRIPTION

ADS807 and ADS808 are complete 12-bit sampling A/D converters. Each contain a sample/hold and a successive approximation A/D converter with a buried zener reference, clock, and 574/674/774-type microprocessor interface. ADS807 analog input pins can be connected for 0V to +10V or ±5V analog input ranges. ADS808 has a ±10V analog input range.

The sample/hold has a 1.5µs max acquisition time to ±0.01% for a full scale input step change. Aperture Time is 25ns and Aperture Uncertainty is 300ps. The A/D converter alone converts in 8µs max.

DC performance is completely specified. 11-bit (J and S grades) and 12-bit (K and T grades) integral linearity grades are available.

AC performance is completely characterized: total harmonic distortion, intermodulation distortion, signal-to-noise ratio and spurious-free dynamic range at the rated 100ksps sampling rate.

ADS807/808s are packaged in a 28-pin side-braze, hermetic, double-wide ceramic DIP and are specified over 0°C to +70°C, and –55°C to +125°C temperature ranges.

ADS807/808s are excellent single-package replacements for A/D converters that use the industry standard 574A/674A/774 pinout along with a separate sample/hold.

SPECIFICATIONS

ELECTRICAL

T_A = +25°C. Sampling Frequency: f_s = 100kHz, $+V_{CC}$ = +15V, $-V_{CC}$ = –15V, V_{DD} = +5V.

	ADS807/808JH			ADS807/808KH			ADS807/808RH			ADS807/808SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			12			•			•			•	BITS
INPUT													
ANALOG INPUT													
Voltage Range [1]													
ADS807		0 to +10V, ±5V			•			•			•		V
ADS808		±10V			•			•			•		V
Impedance	100	150		•	•		•	•		•	•		MΩ
Bias Current			±400			•			•			•	nA
At T_{MIN} or T_{MAX}			±400			•			•			•	nA
DIGITAL INPUTS (Over Temperature Range)													
Logic Levels (TTL Compatible)													
V_{IL}	–1.0		+0.8	•		•	•		•	•		•	V
V_{IH}	+2.0		+5.5	•		•	•		•	•		•	V
I_{IL} (V_I = +0.4V)	–5			•			•			•			µA
I_{IH} (V_I = +2.7V)			+5			•			•			•	µA
DC ACCURACY													
Full Scale Error [2, 3]		±0.3			•			•			•		%
T_{MIN} to T_{MAX} [5]			±0.5			±0.4			±0.8			±0.6	%
Integral Linearity Error			±0.024			±0.012			±0.024			±0.012	% FSR (4)
T_{MIN} to T_{MAX}			±0.024			±0.012			±0.024			±0.012	% FSR
Differential Linearity Error			±0.024			±0.012			±0.024			±0.012	% FSR
No Missing Codes Resolution			11			12			11			12	Bits
T_{MIN} to T_{MAX}			11			12			11			12	Bits
Unipolar Zero (ADS807)			±3			±2			±3			±2	LSB
T_{MIN} to T_{MAX}			±2			±1			±3			±2	LSB
Bipolar Zero			±10			±5			±10			±5	LSB
T_{MIN} to T_{MAX}			±2			±1			±4			±2	LSB
Power Supply Sensitivity													
Change in Full-Scale Calibration													
+14.5 < $+V_{CC}$ < +16.5			0.5			•			•			•	LSB
–16.5 < $-V_{CC}$ < –14.5			1.0			•			•			•	LSB
+4.5 < V_{DD} < +5.5			0.5			•			•			•	LSB
AC CHARACTERISTICS [6]													
Spurious-free Dynamic Range (SFDR)													
f_A = 10.7kHz (–0.5dB)		82			•			•			•		dB
Total Harmonic Distortion (THD)													
f_A = 10.7kHz (–0.5dB)		80			•			•			•		dB
Two-tone Intermodulation Distortion (IMD) [7]													
f_{IN1} = 24.4kHz (–6.5dB)	f_{IN2} = 25.9kHz (–6.5dB)												
ADS807		75			•			•			•		dB
ADS808		72			•			•			•		dB

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C. Sampling Frequency: f_S = 100kHz, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, V_{DD} = +5V.

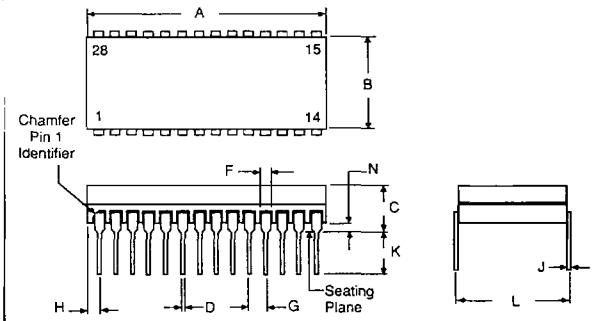
	ADS807/808JH			ADS807/808KH			ADS807/808RH			ADS807/808SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
AC CHARACTERISTICS (Cont.)													
Signal to Noise Ratio (SNR)													
f_{IN} = 10.7kHz (−0.5dB)		72			•			•			•		dB
Input Small Signal Bandwidth													
(2Vp-p sinewave)		2.5			•			•			•		MHz
SAMPLING DYMANICS													
Sampling Rate		100			•			•			•		kHz
Aperture Delay		25			•			•			•		ns
Aperture Uncertainty (Jitter)		300			•			•			•		ps, rms
Feedthrough (10Vp-p, 100kHz) [8]		0.02			•			•			•		%
Transient Response [9]		1.9			•			•			•		µs
Overvoltage Recovery [10]		11.4			•			•			•		µs
REFERENCE OUTPUT													
Voltage	9.9	10.0	10.1	•	•	•	•	•	•	•	•	•	V
Source Current Available for													
External Loads [11]	2			•			•			•			mA
DIGITAL OUTPUTS (Over Temperature)													
Format		Parallel			•			•			•		
Coding		Bipolar Offset Binary (BOB)				•			•			•	
Logic Levels (3-state output, TTL compatible)													
V_{OL} (I_{SINK} = 1.6mA)	0.0		+0.4	•		•	•		•	•		•	V
V_{OH} (I_{SOURCE} = 500µA)	+2.4		+5.0	•		•	•		•	•		•	V
$I_{LEAKAGE}$ (High-Z State)	−5	−0.1	+5	•	•	•	•	•	•	•	•	•	µA
POWER SUPPLIES													
Rated Voltage													
$+V_{CC}$	+14.5	+15	+16	•	•	•	•	•	•	•	•	•	V
$-V_{CC}$	−14.5	−15	−16	•	•	•	•	•	•	•	•	•	V
V_{DD}	+4.5	+5.0	+5.5	•	•	•	•	•	•	•	•	•	V
Current													
$+V_{CC}$		15	18		•	•		•	•		•	•	V
$-V_{CC}$		26	33		•	•		•	•		•	•	V
V_{DD}		9	15		•	•		•	•		•	•	V
Power Consumption		660	850		•	•		•	•		•	•	mW
TEMPERATURE RANGE													
Specification	0		+70	•		•	−55		+125	•		•	°C
Storage	−65		+150	•		•	•		•	•		•	°C

*Specification same as grade to the left.

NOTES: (1) ADS807: For input ranges −5V to +5V, 0 to +10V; ADS808: For input range ±10V (2) Adjustable to zero with external potentiometer. (3) Specifications assume a fixed 50Ω resistor between Ref Out (Pin 8) and Ref In (Pin 10). This specification measured at the FFE_{16} to FFF_{16} transition, includes offset. (4) FSR means Full Scale Range. For ADS807, FSR = 10V; for ADS808 FSR = 20V. (5) Change specifications for unipolar offset, bipolar zero and full-scale error correspond to the change from the initial value (at 25°C) to the value at T_{MIN} or T_{MAX}. (6) Refer to Discussion of Specifications section for definitions. (7) Intermodulation distortion is referred to the larger of the two input test signals. If referred to the peak envelope signal (approx. 0dB), the intermodulation products will be 6dB lower. (8) Sample/Hold Feedthrough: Feedthrough to the output of the A/D converter of a 100kHz sinewave signal when the Sample/Hold is in the HOLD mode. (9) For a 10V step input, ½-bit accuracy attained in specified time. (10) Recovers to specified performance in specified time after 2 x Full-Scale input overvoltage. (11) External load must be constant during conversion.

MECHANICAL

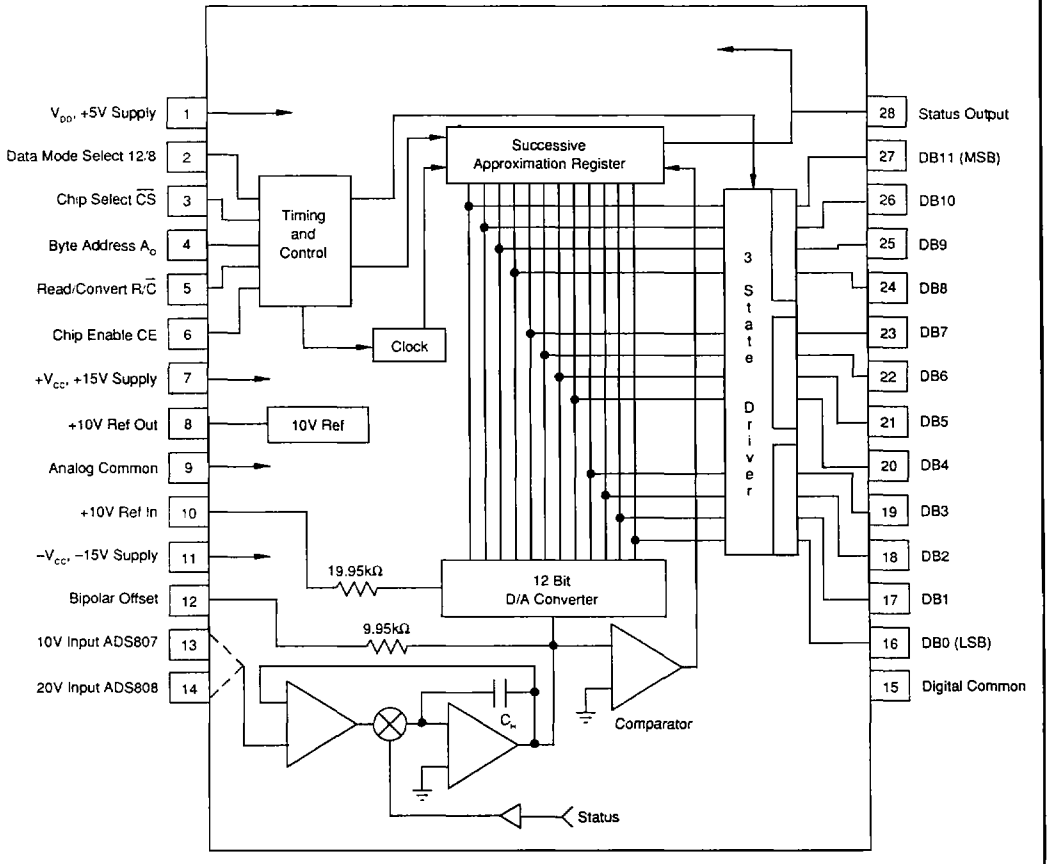
H Package — 28-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	0.38	0.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	0.23	0.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION



NOTE: Pin 14 is a "No Connect" on the ADS807. Pin 13 is a "No Connect" on the ADS808.

ORDERING INFORMATION

Model	Input Range (V)	Linearity Error,%FSR	Specification Temperature Range
ADS307JH	–5 to +5	±0.024	0°C to +70°C
ADS307KH	or	±0.012	0°C to +70°C
ADS307RH	0 to +10	±0.024	–55°C to +125°C
ADS307SH		±0.012	–55°C to +125°C
ADS308JH	–5 to +5	±0.024	0°C to +70°C
ADS308KH	or	±0.012	0°C to +70°C
ADS308RH	–10 to +10	±0.024	–55°C to +125°C
ADS308SH		±0.012	–55°C to +125°C

BURN-IN SCREENING OPTION
See ext for details.

Model	Burn-in Temperature	Specification Temperature Range
ADS307JH-BI	+125°C	0°C to +70°C
ADS307KH-BI	+125°C	0°C to +70°C
ADS307RH-BI	+125°C	–55°C to +125°C
ADS307SH-BI	+125°C	–55°C to +125°C
ADS308JH-BI	+125°C	0°C to +70°C
ADS308KH-BI	+125°C	0°C to +70°C
ADS308RH-BI	+125°C	–55°C to +125°C
ADS308SH-BI	+125°C	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Digital Common	+16.5V
$-V_{CC}$ to Digital Common	–16.5V
V_{DD} to Digital Common	+7V
Analog Common to Digital Common	±1V
Control Inputs to Digital Common	–0.5 to V_{DD} + 0.5V
Ref In, BIP Odd, to Analog Common	±16.5V
Analog Input Voltage	$+V_{CC}$ or $-V_{CC}$
Ref Out	Indefinite Short to Common Momentary Short to V_{CC}
Maximum Junction Temperature	160°C
Internal Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}	50°C/W

BURN-IN SCREENING

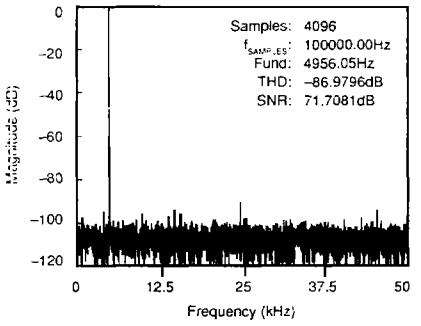
Burn-in screening is an option available for the ADS807/808. Burn-in duration is 160 hours at the temperatures listed below, or at an equivalent combination of time and temperature according to the Arrhenius equation using 1eV activation energy.

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number as shown in the table.

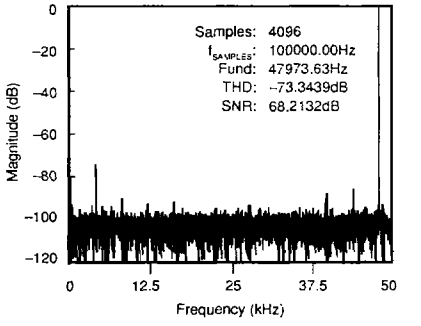
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $+V_{CC}$ = +15V, $-V_{CC}$ = –15V, V_{DD} = +5V.

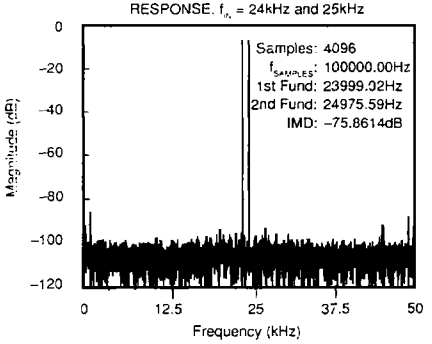
FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 5kHz



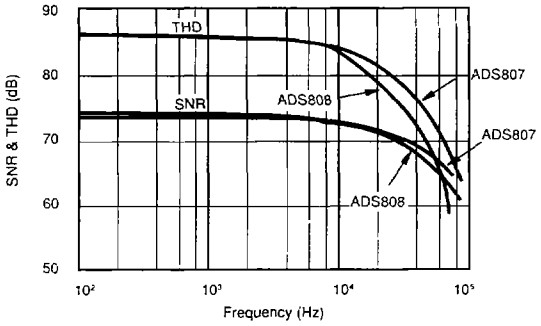
FULL-SCALE SINEWAVE RESPONSE, f_{IN} = 50kHz



TWO-TONE INTERMODULATION RESPONSE, f_{IN} = 24kHz and 25kHz

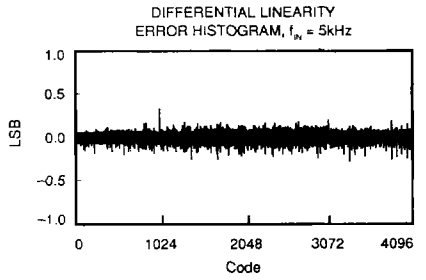


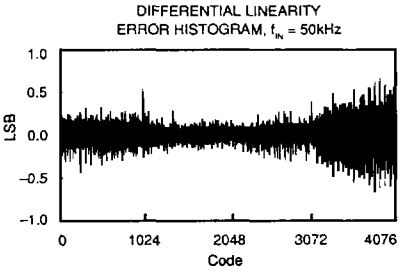
THD & SNR vs INPUT FREQUENCY, f_S = 100kHz



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, V_{DD} = +5V.





DISCUSSION OF SPECIFICATIONS

BASIC DEFINITIONS

Dynamic Range—The ratio of the maximum input signal to the smallest quantum the converter can produce. It is expressed in dB. For an ideal N-bit linear, binary-coded A/D converter, the Dynamic Range is:

$$\text{Dynamic Range} = 20 \log 2^N = 6.02N \text{ dB}$$

This ideal value is degraded by system noise, internal converter noise, and differential linearity error.

Full Scale Range, FSR—The nominal range of the A/D converter. ADS808 has a FSR of 20V for the −10V to +10V input range. ADS807 has a FSR of 10V for the 0V to +10V or −5V to +5V input ranges.

Least Significant Bit, LSB—The smallest analog input change that is resolved by the A/D converter. For an A/D converter with N bits output, the input value of the LSB is $FSR/2^N$.

Most Significant Bit, MSB—That binary digit that has the greatest value or weight. The MSB weight is FSR/2.

Resolution—An N-bit binary-coded A/D converter resolves the analog input into 2^N values represented by the 2^N digital output codes.

DC ACCURACY

Refer to Figure 1 for an illustration of A/D converter DC parameter terminology.

Linearity Error, Integral Linearity Error, (ILE)—Linearity error is defined as the deviation of actual analog input values from the ideal values about a straight line drawn through the code mid-points near full scale (at $+V_{FS}$ −1LSB) and at Zero input (at 1/2LSB below the first code transition, i.e. at zero) or, in the case of bipolar operation, near minus full scale (at 1/2LSB below the first code transition, i.e. at $-V_{FS}$).

Despite the definition, however, code transitions are easier to measure than code midpoints. Therefore linearity is measured as the deviation of the analog input values from a line drawn between the first and last code transitions. Linearity Error specifications are expressed in % of Full Scale Range (FSR). ADS807/808KH ILE is ±0.012% of FSR which is 1/2 LSB at 12-bits.

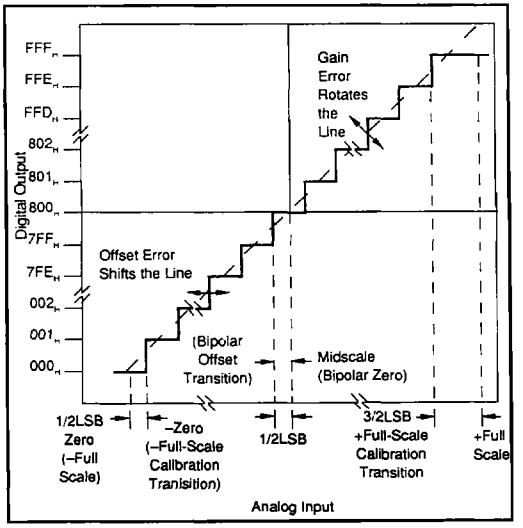


FIGURE 1. Transfer Characteristic Terminology.

Differential Linearity Error, (DLE); No Missing Codes—Differential Linearity Error is defined as the deviation in code width from the ideal value of 1LSB. If the DLE is greater than –1LSB anywhere along the range, the A/D will have at least one missing code. ADS807/808KH are specified to have a DLE of ±0.024% of FSR which is ±1LSB at 12 bits. ADS807/808s are specified to have No Missing Codes for 12-bit resolution over the specification temperature range.

Full Scale Error—The deviation from the ideal value of the input at the last code midpoint (V_{FS} – 1LSB). As with the linearity error measurements, code transition values are the locations actually measured for this spec. The ideal Full Scale transition value is FSR – 3/2LSB for unipolar input converters and FSR/2 – 3/2LSB for bipolar input A/D converters. Full Scale Error is expressed in % of FSR or in LSBs. Refer to Figure 1.

Full Scale Error of the ADS807/808 may be trimmed to zero using external trim potentiometers.

Offset Error

Unipolar Offset Error is defined as the deviation of the actual code-midpoint value of the first code from the ideal value located at 1/2LSB below the ideal first transition value (i.e. at zero volts).

Bipolar Offset Error is defined as the deviation of the actual code-midpoint of the first code from the ideal value located at 1/2LSB below the ideal first transition value located at $-V_{FS}$ +1/2LSB.

Again, transition values are the actual measured parameters. Offset and Zero errors of the ADS807/808 may be trimmed to zero using external trim potentiometers. Offset Error is expressed as a % of FSR.

Bipolar Zero Error is defined as the deviation of the actual mid-scale-code midpoint value of the input from the ideal mid-scale value (i.e. at ZERO volts). The transition value actually measured is 1/2LSB below zero input and has a value of FSR/2 – 1LSB. Refer to Figure 1. Bipolar Zero Error is the sum of the Bipolar Offset Error, 1/2 the Gain Error, and the Linearity Error. It is measured, rather than calculated to avoid tolerance buildup resulting from summing the tolerances of each spec.

Power Supply Sensitivity (Rejection) [PSS, PSR]—Power Supply Sensitivity describes the maximum change in the full-scale transition value from the initial value for a change in each power supply voltage. It is specified in units of LSB over the power supply range.

AC PERFORMANCE

Dynamic Differential Linearity Error—The deviation of the frequency of occurrence of output codes from the ideal when the A/D converter is operated with an input of specified frequency. If a particular code is wider than the ideal 1LSB width, then more counts than the theoretical will accumulate at that code. This characterization is done using a histogram method.

Signal-to-Noise Ratio (SNR)—The ratio of the signal power of a full-scale input sinewave to the RMS output noise power.

$$SNR_{dB} = 10 \log \left(\frac{\text{Sinewave Signal Power}}{\text{Output Noise Power}} \right)$$

For an ideal N-bit A/D converter (measured over an $f_S/2$ bandwidth) the SNR is:

$$SNR_{dB} = 6.02N + 1.76$$

This definition assumes that the output noise is described by what remains after all fundamental, harmonic, DC and outstanding spurious components have been removed. The noise power that is left is a "noise floor" that appears across all frequencies of the measured spectrum at some relatively flat level. SNR is expressed in dB.

Effective Bits—The effective number of bits is calculated using the rewritten formula above and the measured SNR.

$$N_{EFF} = \left(\frac{SNR_{MEAS} - 1.76}{6.02} \right)$$

Spurious-Free Dynamic Range (SFDR)—The power of the peak non-fundamental component (harmonic or spurious, in-band or out-of-band) in the output specturm to the input signal power. Some manufacurers data sheets label this spec as "Harmonics and Spurious Noise" or "AC Linearity Error". SFDR is expressed in dB at specified input frequencies and sampling rates.

$$SFDR_{dB} = 10 \log \left(\frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}} \right)$$

Total Harmonic Distortion (THD)—The ratio of power of the harmonic output to the sinewave input power. THD is expressed in dB at specified input frequencies and sampling rates.

$$THD_{dB} = 10 \log \left(\frac{\text{Harmonic Output Power (to 9 harmonics)}}{\text{Sinewave Signal Power}} \right)$$

Intermodulation Distortion (IMD)—The ratio of the power of the intermodulation products to the input power of the sum of two sinewaves of different frequency. IMD is expressed in dB at specified input frequencies and sampling rates.

$$IMD_{dB} = 10 \log \left(\frac{\text{IMD Product Power (to 5th order products)}}{\text{Sinewave Signal Power}} \right)$$

AC PERFORMANCE CHARACTERIZATION

SPECTRAL CHARACTERIZATION

ADS807/808 are characterized for AC performance using Fast Fourier Transform (FFT) techniques. Figure 2 shows a typical equipment configuration for single-tone testing of THD, SNR and SFDR. Figure 3 shows the setup for Two-tone IMD characterization.

Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. [1] Since no spectral leakage results, no window function is needed. This "rectangular window" was used to generate the spectral performance curves shown in the Typical Performance Curves section of this data sheet. A 4096 point FFT was used for this 12-bit resolution converter to assure that the majority of codes were exercised. If phase-locked signal sources are not available, a windowing function must be applied to the time-domain samples. The four-sample Blackman-Harris window [2] is recommended for evaluating high-performance A/D converters.

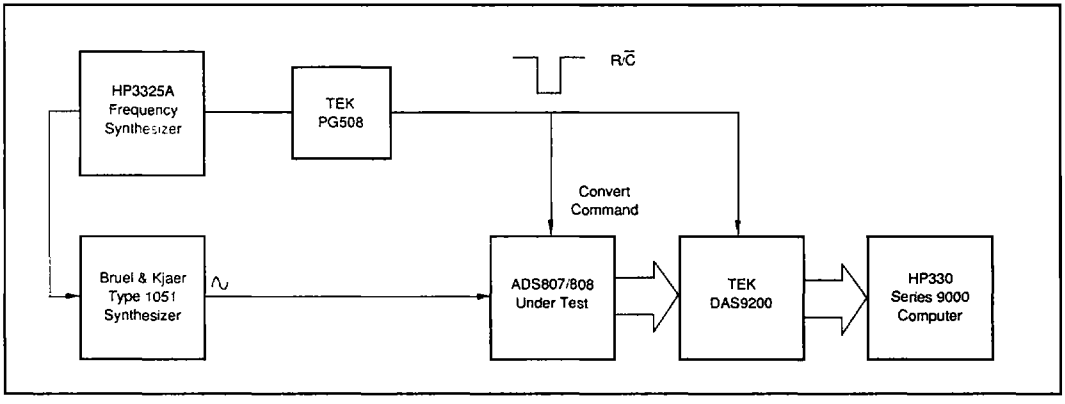


FIGURE 2. Equipment Configuration for Single-Tone Spectral Characterization.

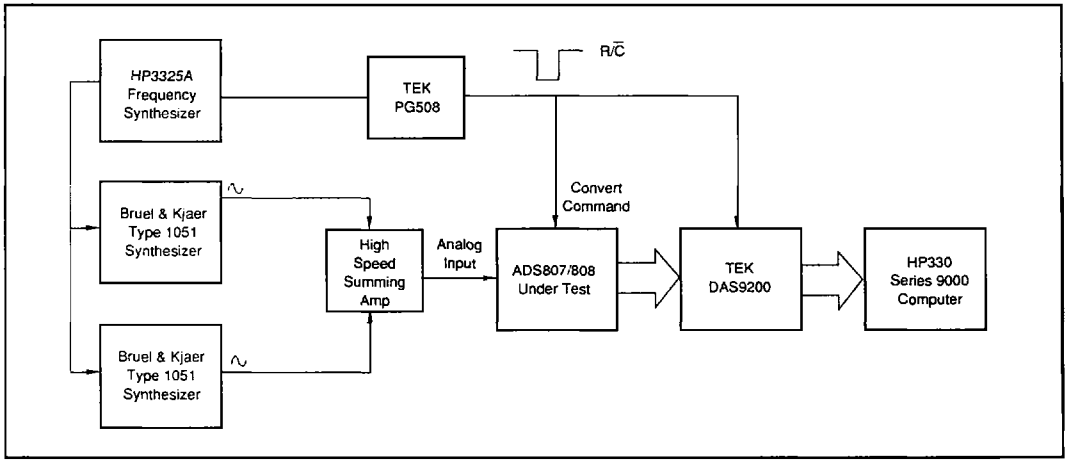


FIGURE 3. Equipment Configuration for Two-Tone Spectral Characterization.

DYNAMIC DLE CHARACTERIZATION

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral non-linearity of the sample/hold and A/D converter.

The influence of differential linearity errors is harder to distinguish in a plot of the output spectrum of an A/D converter — it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity error under dynamic conditions is the histogram.[3] The equipment setup is the same as for the single-tone FFT. Two histograms of ADS808 performance are shown in the Typical Performance Curves section of this data sheet. Note the low DLE at low frequency and the minor degradation of the DLE at the Nyquist frequency.

References:

1. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.

2. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform." *Proceedings of the IEEE*, Vol. 66, No. 1, January 1987, pp 51-83.

3. "Dynamic Tests for A/D Converter Performance," Application Note AN-133, Burr-Brown Corporation, Tucson, AZ, 1985.

INSTALLATION

POWER SUPPLY SELECTION

Linear power supplies are preferred. Switching power supply specifications may appear to indicate low noise output, but these specifications are rms specs. The spikes generated in switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

LAYOUT CONSIDERATIONS

Power Supply Wiring—Use heavy power supply and power supply common (ground) wiring. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits.

When passing converter power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the Analog and Digital Common lines.

Power Supply Returns—(Analog Common & Digital Common) Connect Analog Common and Digital Common together right at the converter with the ground plane. They are not connected internally. This will usually give the best performance. However, it may cause problems for the system designer. Where it is absolutely necessary to separate analog and digital power supply returns, each should be separately returned to the power supply. Do not connect Analog Common and Digital Common together and then run a single wire to the power supply. When using separate returns, connect a 1µF to 47µF tantalum capacitor between Digital Common and Analog Common pins as close to the package as possible.

Power Supply Bypassing—Every power-supply line leading into an A/D converter must be bypassed to its Common pin. The bypass capacitor should be located as close to the converter package as possible and tied to a solid ground — connecting the capacitors to a noisy ground defeats the purpose of the bypass. Use tantalum capacitors with values of from 1µF to 47µF and parallel them with smaller ceramic capacitors for high frequency filtering if necessary.

Separate Analog and Digital Signals—Digital signals entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

Wire-wrap construction is not recommended for best noise performance.

Shield Other Sensitive Points—If external gain and offset potentiometers are used, the potentiometers and associated series resistors should be located as close to the ADS807/808 as possible. If no trim adjusting is required and fixed resistors are used, they should also be located as close to the converter as possible.

ANALOG INPUT RANGES

Unipolar Connection (ADS807 only)

Analog input connections for the 0 to + 10V unipolar input range of ADS807 is shown in Figure 4.

When the 0V to +10V input range is used, apply the analog input to pin 13. If gain adjustment is not used, replace potentiometer R2 with a 50Ω ±1% metal film resistor to meet published specifications. If offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Common).

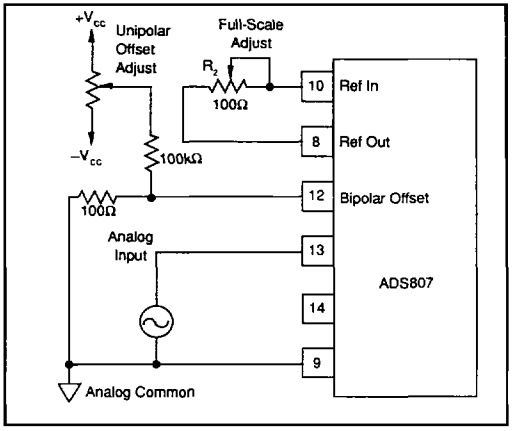


FIGURE 4. Unipolar Connection.

Bipolar Connection

Analog input connections for bipolar input ranges are shown in Figure 5.

Input pin 13 is used on the ADS807. Input pin 14 is used on the ADS808. If either bipolar offset or bipolar gain adjustments are not required, the trim potentiometer R_1 and R_2 are to be replaced with fixed 50Ω ±1% metal film resistors to meet published specifications.

CALIBRATION

UNIPOLAR RANGE (ADS807 only)

To adjust unipolar offset, sweep the input through the end-point transition voltage (0V +1/2LSB), +1.22mV for the ADS807, that causes the output code DB0 High. Adjust potentiometer R_1 until DB0 is alternately toggling High and Low with all other bits Low. Then adjust Full Scale by applying an input voltage of nominal full-scale minus 3/2LSB (V_{FS} –3/2LSB), the value which should cause all bits to be High. This value is +9.9963V. Adjust potentiometer R_2 until bits DB1-DB11 are High and DB0 is toggling High and Low.

BIPOLAR RANGES

The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, ADS807; –9.9976V for the ±10V range, ADS808). Adjust R1 for DB0 to toggle High and Low with all other bits Low. To adjust full-scale, apply a DC input voltage which is 3/2LSB below the nominal plus full-scale value (+4.9963V for the ±5V range, ADS807; +9.9927V for the ±10V range, ADS808) and adjust R2 for DB0 to toggle High and Low with all other bits High.

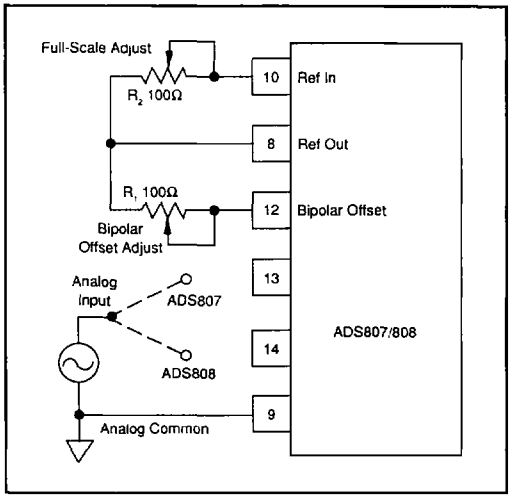


FIGURE 5. Bipolar Connection.

CONTROLLING THE ADS807/808

The Burr-Brown ADS807/808 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready — choosing either 12 bits all at once, 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE) all perform the same functions as the interface to the popular A/D converters ADC574A, ADC674A, and ADC774. They are TTL/5V-CMOS compatible. Table II contains a summary of the control line functions of the ADS807/808. The control function truth table is listed in Table III.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range	Defined As:	±10V (ADS808)	0V to +10V (ADS807)	±5V (ADS807)
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	10V/2^n
	n=8	78.13mV	39.06mV	39.06mV
	n=12	4.88mV	2.44mV	2.44mV
Output Transition Values				
FFE_H to FFF_H	+Full-scale	+10V-3/2LSB	+10V–3/2LSB	+5V–3/2LSB
$7FF_H$ to 800_H	Mid Scale, (BP Zero)	0V–1/2LSB	+5V–1/2LSB	0V–1/2LSB
000_H to 001_H	Zero, –Full Scale	–10V+1/2LSB	0V+1/2LSB	–5V+1/2LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0->1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (Active Low)	Must be low ("0") to either initiate a conversion or read output data. 1->0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12- bit operation. 1->0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0->1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8- bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing zeros (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADS807/808 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
0->1	0	0	X	0	Hold & Initiate 12-bit conversion
0->1	0	0	X	1	Hold & Initiate 8-bit conversion
1	1->0	0	X	0	Hold & Initiate 12-bit conversion
1	1->0	0	X	1	Hold & Initiate 8-bit conversion
1	0	1->0	X	0	Hold & Initiate 12-bit conversion
1	0	1->0	X	1	Hold & Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table. (X means Don't Care.)

STAND-ALONE (NO BUS INTERFACE) OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{DD} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a High-to-Low transition (Hold/Convert) of R/$\overline{C}$. This transition commands the sample/hold to Hold and the converter logic to start the conversion. The Sample-To-Hold settling time is so short that the sample/hold is fully settled to the required accuracy before the first successive approximation A/D decision occurs.

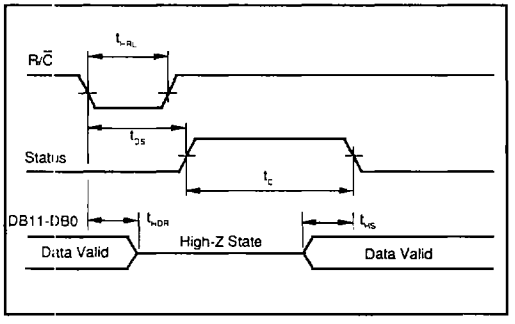


FIGURE 6. R/$\overline{C}$ Pulse Low — Output Enables After Conversion.

The three-state data output buffers are enabled when R/$\overline{C}$ is High and Status is Low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 6 illustrates timing when the Hold/Convert command is initiated by an R/$\overline{C}$ pulse which goes Low and returns to the High state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 7 illustrates the timing when Hold/Convert is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	115	150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-alone Mode Timing.

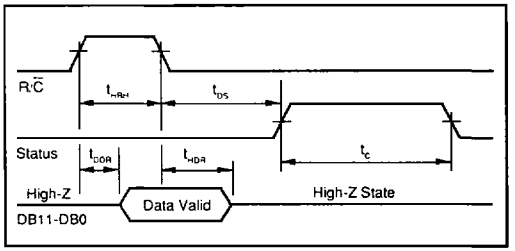


FIGURE 7. R/$\overline{C}$ Pulse High—Output Enables Only While R/$\overline{C}$ Is High.

Note that, unlike the R/$\overline{C}$ command input timing for non-sampling A/D converters such as the ADC574A/674A/774, a time period (Acquisition Time) must be allowed for the sample/hold amplifier to acquire the next sample. This time period, occurring immediately after the conversion is complete (Status goes Low), is 1µs typical (1.5µs maximum) for acquisition to ±0.01% of Full Scale Range for a 10V analog input change from the previous held value to the next.

FULLY CONTROLLED OPERATION

Throughput Period

The throughput period, reciprocal of the sampling rate, (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a Hold/Convert start transition (described below). If A_0 is latched High, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is Low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be Low (logic 0) and DB3 will be High (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

Conversion Start

The converter is commanded to initiate a Hold/Convert operation by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three logic inputs to reach the required state and thus all three may be dynamically controlled. If necessary all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts the operation. If it is desired that a particular input establish the actual start of operation, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of operation timing are illustrated in Figure 8. The specifications for timing are contained in Table V.

The Status output indicates the current state of the converter by being in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of operation, any additional Hold/Convert transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8-bits vs. 12-bits) for that conversion.

As with stand-alone operation described above, sample/hold Acquisition Time must be provided before the next Hold/Convert command.

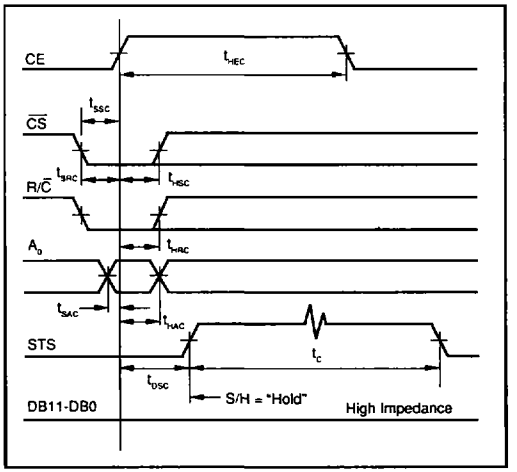


FIGURE 8. Conversion Cycle Timing.

READING OUTPUT DATA

After operation is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ High, Status Low, CE High and $\overline{CS}$ Low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 11 and Table V for timing relationships and specifications.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Conversion Mode					
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time plus				
	Acquisition time 12-bit cycle		9	10	µs
	8-bit cycle		6	6.5	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	115	150	375	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

TABLE V. Timing Specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the High or Low condition, although it is fully TTL-and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is High, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the state of A_0 is ignored.

When 12/$\overline{8}$ is Low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the Read cycle. Connection of the ADS807/808 to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is Low, the byte addressed contains the 8MSBs. When A_0 is High, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 10. The design of the ADS807/808 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the Read operation will be attempted only after the conversion is complete and the Status output has gone Low. In those situations requiring the earliest possible access to the data, the Read operation may be started as much as (t_{DD} max + t_{HS} max) before Status goes Low. Of course, Acquisition Time must be allowed for the sample/hold before the next Hold/Convert operation is initiated. Refer to Figure 11 for these timing relationships.

Word 1							
Processor							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter							
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Word 2							
Processor							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter							
DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 10. 12-Bit Data Format for 8-Bit Bus System.

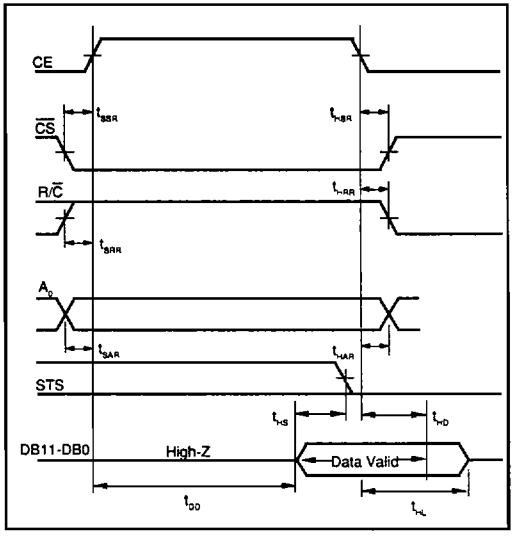


FIGURE 11. Read Cycle Timing.

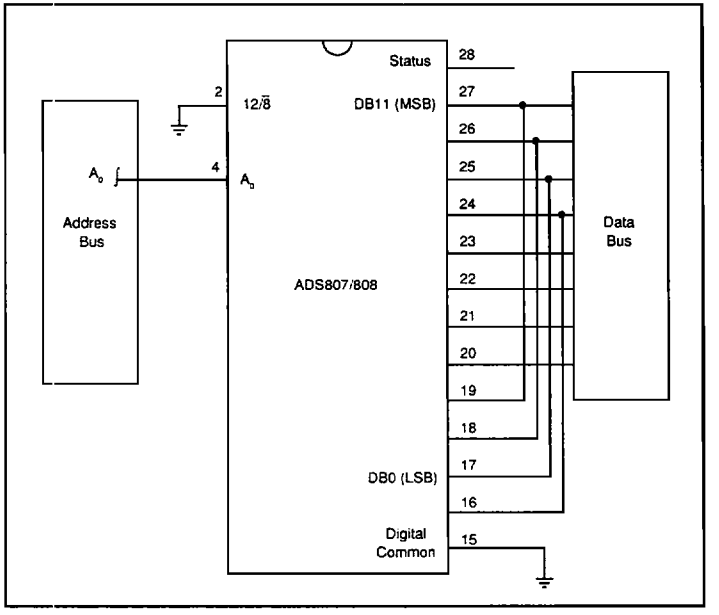


FIGURE 9. Connection to an 8-bit Bus.