HARRIS SEMICONDUCTOR

ACS630MS

Radiation Hardened EDAC (Error Detection and Correction Circuit)

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} Rads(Si)/s, 20ns Pulse
- Cosmic Ray Upset Immunity (1 x 10^{-11}) Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH
- Fast Processing Time
  - Write Cycle: Generates Check Word In 20ns (Typ)
  - Read Cycle: Flags Errors In 10ns (Typ)

Description

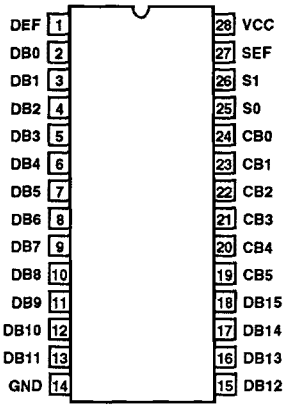
The Harris ACS630MS is a Radiation Hardened 16-bit parallel error detection and correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle, during a memory read cycle a 22-bit word is taken form memory and checked for errors. Single bit errors in the data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

The ACS630MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family .

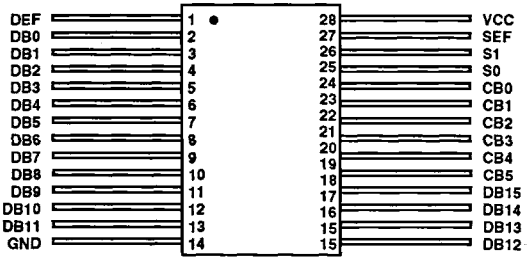
The ACS630MS is supplied in a 28 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

28 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S DESIGNATOR CDIP2 - T28, LEAD FINISH C
TOP VIEW



28 PIN CERAMIC FLAT PACK
MIL-STD-183S DESIGNATOR CDFP3-F28, LEAD FINISH C
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3199**

Function Tables

Control Functions

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECKWORD	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data and Checkword	Input Data	Input Checkword	Low	Low
READ	High	High	Latch and Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word and Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

Check Word Generation

CHECKWORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

NOTE: The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit

Error Syndrome Codes

SYNDROME ERROR CODE	ERROR LOCATIONS																						
	DB																CB						NO ERROR
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Error Functions

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-BIT DATA	6-BIT CHECKWORD	SEF	DEF	
0	0	Low	Low	Not Applicable
1	0	High	Low	Correction
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output 50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 10ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	150	µA
			2, 3	+125°C, -55°C	-	3	mA
Output Current (Sink)	IOL1	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	mA
Output Current (Source)	IOH1	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	mA
DEF, SEF Output Current (Source)	IOL2	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
DEF, SEF Output Current (Sink)	IOH2	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay DB to CB	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	21	ns
			10, 11	+125°C, -55°C	1	23.5	ns
	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	20	ns
			10, 11	+125°C, -55°C	1	24.5	ns
Propagation Delay S1 to DEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	13	ns
			10, 11	+125°C, -55°C	1	15.5	ns
Propagation Delay S1 to SEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	13	ns
			10, 11	+125°C, -55°C	1	15.5	ns
Propagation Delay S0 to DB/CB	TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	21	ns
			10, 11	+125°C, -55°C	1	21.5	ns
	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	18	ns
			10, 11	+125°C, -55°C	1	20.5	ns
Propagation Delay S0 to DB/CB	TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	18	ns
			10, 11	+125°C, -55°C	1	20.5	ns
	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	15	ns
			10, 11	+125°C, -55°C	1	16.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Operation Current DB to CB	IOPER	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	Typical 4.25		mA
				+125°C, -55°C	Typical 4.75		mA
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C, -55°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C, -55°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1MRAD LIMITS MIN	1MRAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	3	mA
Output Current (Sink)	IOL1	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	12	-	mA
Output Current (Source)	IOH1	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-12	-	mA
DEF, SEF Output Current (Sink)	IOL2	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	4	-	mA
DEF, SEF Output Current (Source)	IOH2	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-4	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC - 0.1	-	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	+25°C	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V (Note 3)	+25°C	-	-	-
Propagation Delay DB to CB	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	23.5	ns
	TPLH		+25°C	1	24.5	ns
Propagation Delay S1 to DEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	15.5	ns
Propagation Delay S1 to SEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	15.5	ns
Propagation Delay S0 to DB/CB	TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	21.5	ns
	TPLZ		+25°C	1	19.5	ns
Propagation Delay S0 to DB/CB	TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	20.5	ns
	TPZL		+25°C	1	16.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±30µA
IOL/IOH	5	±15%
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN Test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
-	2 - 18, 25, 26	1, 27, 19 - 24	28	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	14	1, 27	2 - 13, 15 - 26, 28	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	14, 25, 26	1, 19 - 24, 27	4 - 13, 15 - 26, 28	3, 17	2, 18

NOTES:

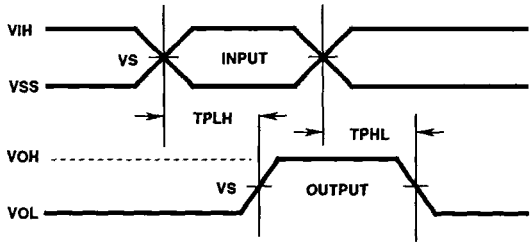
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.
2. Second dynamic burn-in assures proper stress in both directions. 400 additional hours at life test with a down point; 96 additional hours at production burn-in without a down point.

TABLE 9. RADIATION TEST CONNECTIONS

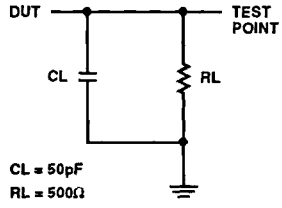
OPEN	GROUND	VCC = 5V ± 0.5V
-	14	2 - 13, 15 - 26, 28

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

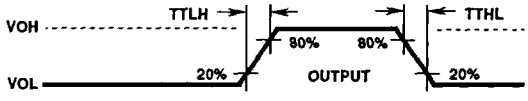
Propagation Delay Timing Diagram



Propagation Delay Load Circuit



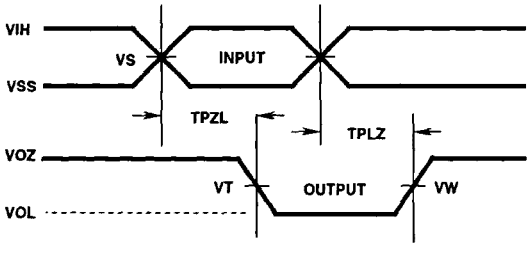
Transition Timing Diagrams



VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

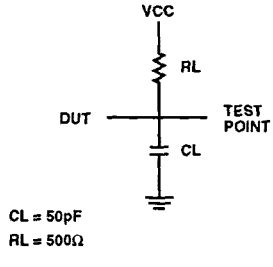
Tri-State Low Timing Diagrams



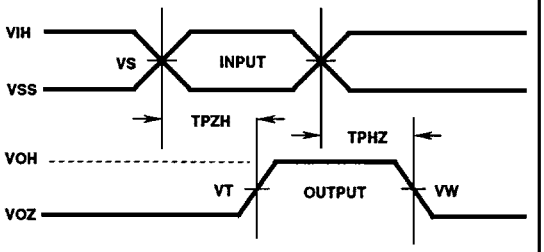
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.2	VCC
GND	0	V

Tri-State Low Load Circuit



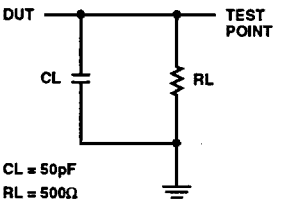
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.8	VCC
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
171 x 159 (Mils)
4340 x 4040 (mm)

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.4 x 4.4 (Mils)

Metallization Mask Layout