



## PCMCIA Flash Memory Card 2 MEGABYTE through 40 MEGABYTE (Intel/Sharp based)

### FEATURES

- Low cost High Density Linear Flash Card
- Supports 3V or 5V only systems
- x8/ x16 Data Interface
- Based on Intel/Sharp FlashFile Components
- Fast Read Performance
  - 150ns @ 5V
  - 200ns @ 3.3V
- High Performance Random Writes
  - 8 $\mu$ s Typical Word Write Time @ 5V
  - 17 $\mu$ s Typical Word Write Time @ 3.3V
- Automated Write and Erase Algorithms
  - Command User Interface
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

### GENERAL DESCRIPTION

WEDC's FLV Series Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLV series cards conform to the PCMCIA international standard

The card's control logic provides the system interface and controls the internal Flash memories. The card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLV Flash cards provide removable high-performance disk emulation.

The FLV series offers low power modes controlled by registers. Cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLV series is based on Intel/Sharp Flash memories.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

### ARCHITECTURE OVERVIEW

WEDC's FLV series is designed to support from 2 to 20 of 8Mb or 16MB components, providing a wide range of density options. Cards are based on the 28F008SC (8Mb) and 28F016SC (16Mb) devices for 3.3V or 5V only applications. Devices codes for the 28F008SC and the 28F016SC are: A6H and AAH respectively. Systems should be able to recognize all the codes. Cards utilizing the 8Mb components provide densities ranging from 2MB to 20MB in 2MB increments, cards utilizing 16Mb components provide densities ranging from 4MB to 40MB in 4MB increments.

In support of the PC Card 95 standard for word wide access, devices are paired. Therefore, the Flash array is structured in 64K word (128kBytes) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation. By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7.

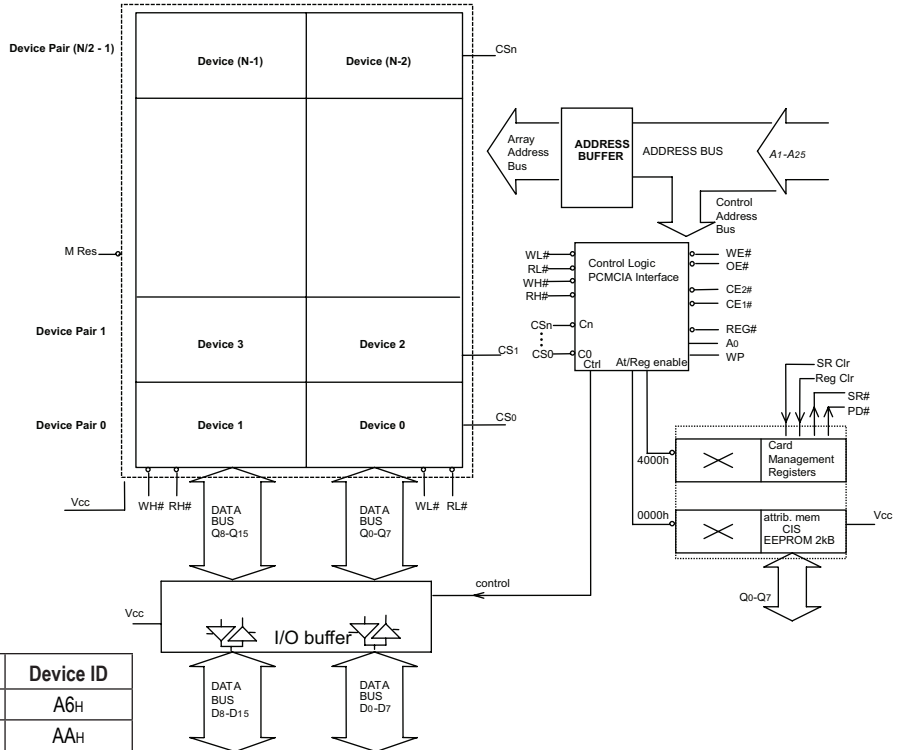
The **FLA21-FLA28** series also supports the following PCMCIA compatible register functions: Soft Reset via the Configuration Option Register, Power Down (sleep mode) via the Configuration and Status Register and monitoring of Ready/Busy, Soft Reset and Power Down via the Card Status Register (cards without attribute memory and versions **FLV51-FLV58** do not have registers). **FLV51-FLV58** do not support Ready/Busy and Reset signals.

The FLV series cards conform to the PC Card (PCMCIA) and JEIDA standards, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact your WEDC sales representative for further information on Custom artwork.



**BLOCK DIAGRAM**



Device type	Manuf ID	Device ID
28F008SC	89H	A6H
28F016SC	89H	AAH

**REGISTERS IN ATTRIBUTE MEMORY SPACE\***

ADDRESS	REGISTER NAME
4100h	Status Register
4002h	Config. and Status Register
4000h	Configuration Option Register

\* FLV51- FLV58 and cards without Attribute Memory do not have registers.

**COR  
CONFIGURATION OPTION REGISTER: ADRS =  
4000H WRITE ONLY**

SRES	LREQ	Configuration Index						
D7	D6	D5	D4	D3	D2	D1	D0	

- D7 Soft Reset, active High  
1 = Reset State  
0 = End Reset State
- D6 Level Req (not supported)
- D5-D0 Configuration index (not supported)

**CSR  
CONFIGURATION STATUS REGISTER: ADRS =  
4002H WRITE ONLY**

Not Supported					PDwn	Not Supported		
D7	D6	D5	D4	D3	D2	D1	D0	

- D2 Power Down, active High  
1 = Place all memory devices in power down mode  
0 = Normal Operation  
Power On default = 0

**SR  
STATUS REGISTER: ADRS = 4100H READ ONLY**

Not Supported	SReset		PDwn	Not Supported	R/BSY#		
D7	D6	D5	D4	D3	D2	D1	D0

- D5 Represents the state of SRESET bit in COR (4000h)  
1 = Reset  
0 = Normal Operation  
Power On default D5 = 0
- D3 Represents the state of Power Down bit (D2) in CSR (4002h)  
1 = Power Down
- D0 Reflects the card's Ready/Busy signal (pin 16) driven by memory components Ready/Busy outputs. This bit allows software polling of the card's Ready/Busy status.  
1 = Ready



**PINOUT**

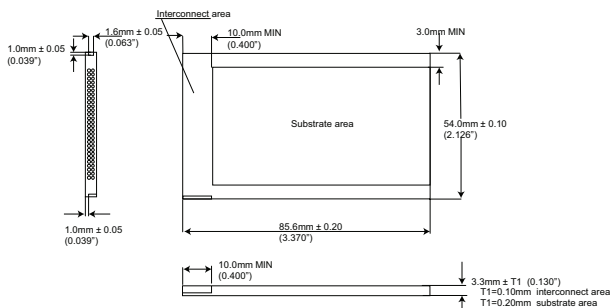
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW (4)
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	NC
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	NC (2)
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	
50	A21	I	Address bit 21	
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	NC
53	A22	I	Address bit 22	
54	A23	I	Address bit 23	
55	A24	I	Address bit 24	
56	A25	I	Address bit 25	
57	VS2	O	Voltage Sense 2	NC
58	RST	I	Card Reset	HIGH
59	WAIT#	O	Extended Bus cycle	Low (3)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(3)
63	BVD1	O	Bat. Volt. Detect 1	(3)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

1. RDY/BSY# signal is an "Open drain" type output, pull-up resistor on host side is required.
2. WAIT#, BVD1 and BVD2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie: 4MB A21 is MSB A22-A25 are NC).
4. NC - No Connection for FLV51-FLV58

**MECHANICAL**



White Electronic Designs Corp. reserves the right to change products or specifications without notice.



**CARD SIGNAL DESCRIPTION**

Symbol	Type	Name and Function
A0 - A25	INPUT	<b>ADDRESS INPUTS:</b> A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	<b>DATA INPUT/OUTPUT:</b> DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	<b>CARD ENABLE 1 AND 2:</b> CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Active low signal gating read data from the memory card.
WE#	INPUT	<b>WRITE ENABLE:</b> Active low signal gating write data to the memory card.
RDY/BSY#(*)	OUTPUT	<b>READY/BUSY OUTPUT:</b> Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	<b>CARD DETECT 1 and 2:</b> Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	<b>WRITE PROTECT:</b> Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
V <sub>PP1</sub> , V <sub>PP2</sub>	N.C.	<b>PROGRAM/ERASE POWER SUPPLY:</b> Provides programming voltages for card. Not connected for 3.3V/5V only card.
V <sub>cc</sub>		<b>CARD POWER SUPPLY:</b> 5.0V for all internal circuitry
GND		<b>CARD GROUND</b>
REG#	INPUT	<b>ATTRIBUTE MEMORY SELECT :</b> Active low signal, enables access to attribute memory space, occupied by the Card Information Structure (CIS) and Card Registers.
RST	INPUT	<b>RESET:</b> Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down control for the memory array.
WAIT#	OUTPUT	<b>WAIT#:</b> This signal is pulled high internally for compatibility. No WAIT# states are generated.
BVD1, BVD2	OUTPUT	<b>BATTERY VOLTAGE DETECT:</b> These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	<b>VOLTAGE SENSE:</b> Notifies the host socket of the card's V <sub>cc</sub> requirements. VS1 and VS2 are open to indicate a 5V card
RFU		RESERVED FOR FUTURE USE
NC		<b>NO INTERNAL CONNECTION TO CARD:</b> pin may be driven or left floating

(\*) Signals not supported by FLV51-FLV58 (NC)

**FUNCTIONAL TRUTH TABLE**

READ function						Common Memory			Attribute Memory		
Function Mode	CE2#	CE1#	A0	OE#	WE#	REG#	D15-D8	D7-D0	REG#	D15-D8	D7-D0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

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**ABSOLUTE MAXIMUM RATINGS (1)**

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85°C
Storage Temperature	
Commercial	-30°C to +80 °C
Industrial	-40°C to +85°C
Voltage on any pin relative to Vss	-0.5V to Vcc+0.5V
Vcc supply Voltage relative to Vss	-0.5V to +7.0V

Note: Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC CHARACTERISTICS (1)**

**V<sub>CC</sub> = 3.3V/5V**

Symbol	Parameter	Density (Mbytes)	Notes	3.3V Vcc		5V Vcc		Units	Test Conditions
				Typ <sup>(3)</sup>	Max	Typ <sup>(3)</sup>	Max		
I <sub>CCR</sub>	Vcc Read Current	All		10	12	20	35	mA	Vcc = Vcc max t <sub>cycle</sub> = 150ns, CMOS levels
I <sub>CCW</sub>	Vcc Program Current	All	28F008SC 28F016SC		60		75	mA	
I <sub>CCE</sub>	Vcc Erase Current	All			40		50	mA	
I <sub>CCS</sub> (CMOS)	Vcc Standby Current	2MB	2	50	200	60	230	μA	Vcc = Vcc max Control Signals = Vcc Reset = Vss, CMOS levels
		20MB	28F008SC	400		420			
		4MB	2	50	200	60	230		
		40MB	28F016SC	400		420			

CMOS Test Conditions: V<sub>CC</sub> = 5V ± 5%, V<sub>IL</sub> = V<sub>SS</sub> ± 0.2V, V<sub>IH</sub> = V<sub>CC</sub> ± 0.2V

Notes:

- All currents are RMS values unless otherwise specified. I<sub>CCR</sub>, I<sub>CCW</sub> and I<sub>CCE</sub> are based on Byte wide operations. For 16 bit operation values are double.
- Control Signals: CE<sub>1#</sub>, CE<sub>2#</sub>, OE#, WE#, REG#.
- Typical: V<sub>CC</sub> = 5V, T = +25°C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I <sub>LI</sub>	Input Leakage Current	1		±20	μA	Vcc = VccMAX VIN = Vcc or Vss
I <sub>LO</sub>	Output Leakage Current	1		±20	μA	Vcc = VccMAX VOUT = Vcc or Vss
V <sub>IL</sub>	Input Low Voltage	1	0	0.8	V	
V <sub>IH</sub>	Input High Voltage	1	0.7xVcc	Vcc+0.5	V	
V <sub>OL</sub>	Output Low Voltage	1		0.4	V	I <sub>OL</sub> = 3.2mA
V <sub>OH</sub>	Output High Voltage	1	Vcc-0.4	Vcc	V	I <sub>OH</sub> = -2.0mA
V <sub>LKO</sub>	Vcc Erase/Program Lock Voltage	1	2.0		V	

Notes:

- Values are the same for byte and word wide modes for all card densities.
- Exceptions: Leakage currents on CE<sub>1#</sub>, CE<sub>2#</sub>, OE#, REG# and WE# will be < 500 μA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be < 150μA when VIN=Vcc due to internal pull-down resistor.

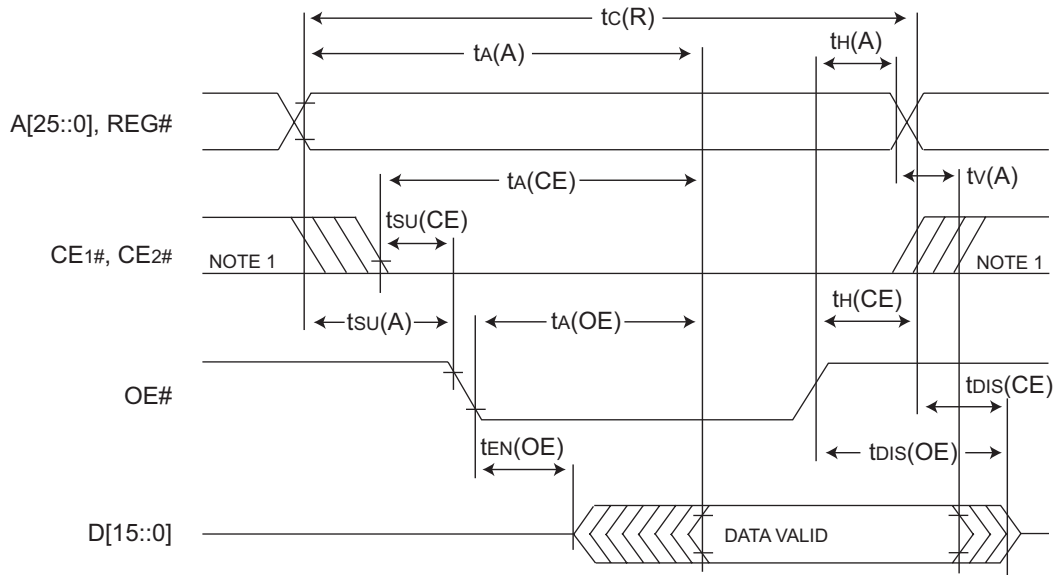


**AC CHARACTERISTICS - READ TIMING PARAMETERS**

SYMBOL (PCMCIA)	Parameter	150ns		250ns		Unit
		Min	Max	Min	Max	
$t_c(R)$	Read Cycle Time	150		250		ns
$t_A(A)$	Address Access Time		150		250	ns
$t_A(CE)$	Card Enable Access Time		150		250	ns
$t_A(OE\#)$	Output Enable Access Time		75		125	ns
$t_{su}(A)$	Address Setup Time		20		30	ns
$t_{su}(CE)$	Card Enable Setup Time		0		0	ns
$t_H(A)$	Address Hold Time		20		30	ns
$t_H(CE)$	Card Enable Hold Time		20		30	ns
$t_v(A)$	Output Hold from Address Change		0		0	ns
$t_{dis}(CE)$	Output Disable Time from CE		75		100	ns
$t_{dis}(OE\#)$	Output Disable Time from OE#		75		100	ns
$t_{en}(CE)$	Output Enable Time from CE	5		5		ns
$t_{en}(OE\#)$	Output Enable Time from OE#	5		5		ns
$t_{rec}(RSR)$	Power Down recovery to Output Delay. $V_{CC} = 5V$		500		600	ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

**READ TIMING DIAGRAM**



Note: Signal may be high or low in this area.

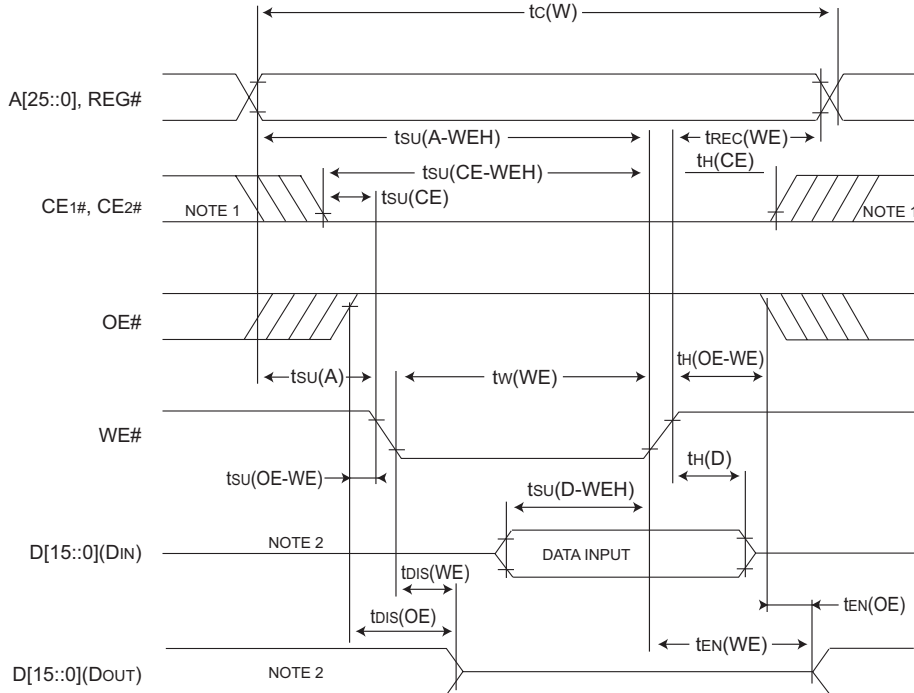


**AC CHARACTERISTICS - WRITE TIMING PARAMETERS**

SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
tcW	Write Cycle Time	150		250		ns
tw(WE)	Write Pulse Width	80		150		ns
tsu(A)	Address Setup Time	20		30		ns
tsu(A-WEH)	Address Setup Time for WE#	100		180		ns
tsu(CE-WEH)	Card Enable Setup Time for WE#	100		180		ns
tsu(D-WEH)	Data Setup Time for WE#	50		80		ns
th(D)	Data Hold Time	20		30		ns
trec(WE)	Write Recover Time	20		30		ns
tdis(WE)	Output Disable Time from WE#		75		100	ns
tdis(OE#)	Output Disable Time from OE#		75		100	ns
tEN(WE)	Output Enable Time from WE#	5		5		ns
tEN(OE#)	Output Enable Time from OE#	5		5		ns
tsu(OE#-WE)	Output Enable Setup from WE#	10		10		ns
th(OE#-WE)	Output Enable Hold from WE#	10		10		ns
tsu(CE)	Card Enable Setup Time from OE#	0		0		ns
th(CE)	Card Enable Hold Time	20		20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

**WRITE TIMING DIAGRAM**



Notes:

- Signal may be high or low in this area.
- When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.



DATA WRITE AND ERASE PERFORMANCE (1,3)

V<sub>CC</sub> = 5V ± 5%, TA = 0C° TO + 70C°

Symbol	Parameter	Notes	Min	Typ <sup>(1)</sup>	Max	Units
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Word/Byte Program time	4		8		µs
t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Program Time	Device SC	0.4	0.5		sec
	Block Erase Time	Device SC	0.9	1.1		sec

V<sub>CC</sub> = 3.3V ± 0.3V, TA = 0C° TO + 70C°

Symbol	Parameter	Notes	Min	Typ <sup>(1)</sup>	Max	Units
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Word/Byte Program time	4		17		µs
t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Program Time	Device SC	0.4	1.1		sec
	Block Erase Time	Device SC	0.9	1.8		sec

Notes:

1. Typical: Nominal voltages and T<sub>A</sub> = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

PRODUCT MARKING

EDI

WED 7P016FLV5600C15 C995 9915

COMPANY NAME \_\_\_\_\_

PART NUMBER \_\_\_\_\_

LOT CODE/TRACE NUMBER \_\_\_\_\_

DATE CODE \_\_\_\_\_

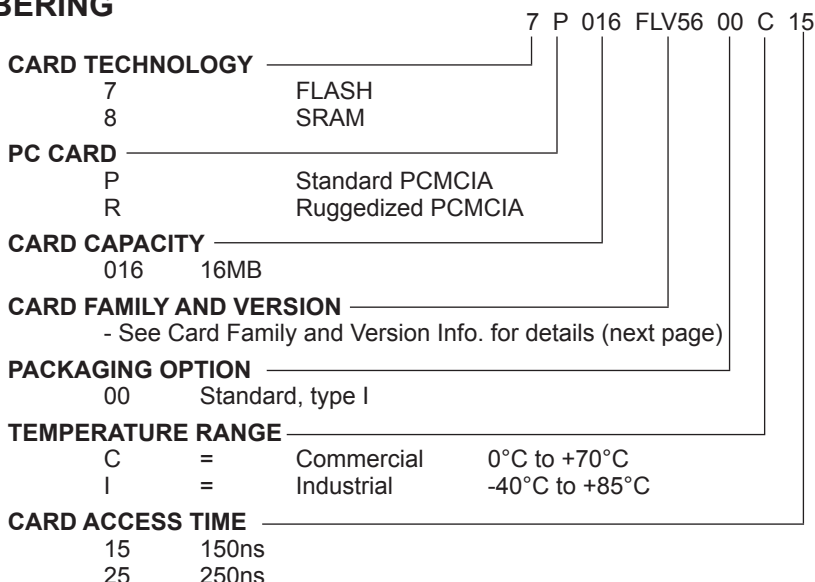
Note:

Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.





PART NUMBERING



CARD FAMILY AND VERSION INFORMATION

**FLV21-FLV24** Based on **28F008SC** for 3.3V/5V application

- FLV21** No Attribute Memory, no Write Protect switch
  - FLV22** With Attribute Memory, no Write Protect switch
  - FLV23** No Attribute Memory, with Write Protect switch
  - FLV24** With Attribute Memory, with Write Protect switch
- Example P/N **7P XXX FLV 22 SS T ZZ**

**FLV25-FLV28** Based on **28F016SC** for 3.3V/5V application

- FLA25** No Attribute Memory, no Write Protect switch
  - FLA26** With Attribute Memory, no Write Protect switch
  - FLA27** No Attribute Memory, with Write Protect switch
  - FLA28** With Attribute Memory, with Write Protect switch
- Example P/N **7P XXX FLV 26 SS T ZZ**

**FLV51-FLV54** Based on **28F008SC** for 3.3V/5V application. The same as FLA21-FLA24 with exception:

- no registers
- signals RST, RDY/BSY#, WAIT# are not connected

- FLA51** No Attribute Memory, no Write Protect switch
  - FLA52** With Attribute Memory, no Write Protect switch
  - FLA53** No Attribute Memory, with Write Protect switch
  - FLA54** With Attribute Memory, with Write Protect switch
- Example P/N **7P XXX FLV 52 SS T ZZ**

**FLV55-FLV58** Based on **28F016SC** for 3.3V/5V application. The same as FLA25-FLA28 with exception:

- no registers
  - signals RST, RDY/BSY#, WAIT# are not connected
- FLA55** No Attribute Memory, no Write Protect switch
  - FLA56** With Attribute Memory, no Write Protect switch
  - FLA57** No Attribute Memory, with Write Protect switch
  - FLA58** With Attribute Memory, with Write Protect switch
- Example P/N **7P XXX FLV 56 SS T ZZ**



**ORDERING INFORMATION**

7P XXX FLVYY SS T ZZ

**XXX**

002 <sup>1)</sup>	2MB	012	12MB	024 <sup>2)</sup>	24MB
004		4MB	014 <sup>1)</sup>	14MB	028 <sup>2)</sup> 28MB
006 <sup>1)</sup>	6MB	016	16MB	032 <sup>2)</sup>	32MB
008		8MB	018 <sup>1)</sup>	18MB	036 <sup>2)</sup> 36MB
010 <sup>1)</sup>	10MB	020	20MB	040 <sup>2)</sup>	40MB

<sup>1)</sup>available only for FLV21/51-FLV24/54

<sup>2)</sup>available only for FLV25/55-FLV28/58

**FLVYY**

Card Version (See card family and version information)

**SS**

00	WEDC Silkscreen
01	Blank Housing, Type I
02	Blank Housing, Type I Recessed

**T**

C	Commercial
I**	Industrial

**ZZ**

15	150ns
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\*\*Denotes advanced information.

ADDRESS	VALUE	DESCRIPTION
00H	01H	CISTPL_DEVICE
02H	03H	TPL_LINK
04H	53H	FLASH = 150ns (device writable)
06H	0EH	CARD SIZE: 4MB
	1EH	8MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
08H	FFH	END OF DEVICE
0AH	1CH	CISTPL_DEVICE_OC
0CH	04H	TPL_LINK
0EH	02H	3 VOLT OPERATION
10H	51H	FLASH = 250ns (device writable)
12H	0EH	CARD SIZE: 4MB
	1EH	4MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
14H	FFH	END OF DEVICE
16H	18H	CISTPL_JEDEC_C

ADDRESS	VALUE	DESCRIPTION
18H	03H	TPL_LINK
1AH	89H	INTEL - ID
1CH	AAH	INTEL 28F016SC - ID(4-40MB)
1EH	FFH	END OF DEVICE
20H	17H	CISTPL_DEVICE_A
22H	03H	TPL_LINK
24H	42H	EEPROM - 200ns
26H	01H	Device Size = 2KBytes
28H	FFH	END OF TUPLE
2AH	1DH	CISTPL_DEVICE_OA
2CH	03H	TPL_LINK
2EH	02H	3 VOLT OPERATION
30H	11H	ROM - 250ns
32H	FFH	END OF DEVICE
34H	1AH	CISTPL_CONF
36H	06H	TPL_LINK
38H	01H	TPCC_SZ
3AH	00H	TPCC_LAST
3CH	00H	TPCC_RADR
3EH	40H	TPCC_RADR
40H	03H	TPCC_RMSK
42H	FFH	CISTPL_END
44H	1EH	CISTPL_DEVICEGEO
46H	06H	TPL_LINK

White Electronic Designs Corp. reserves the right to change products or specifications without notice.



**CIS INFORMATION FOR FLV SERIES CARDS  
EXAMPLE FOR FLV26 FAMILY, 4MB, BUILT WITH 28F016SC**

ADDRESS	VALUE	DESCRIPTION
48H	02H	DGTPL_BUS
4AH	11H	DGTPL_EBS
4CH	01H	DGTPL_RBS
4EH	01H	DGTPL_WBS
50H	01H	DGTPL_PART
52H	01H	FLASH DEVICE NON-INTERLEAVED
54H	20H	<b>CISTPL_MANFID</b>
56H	04H	TPL_LINK(04H)
58H	F6H	EDI TPLMID_MANF: LSB
5AH	01H	EDI TPLMID_MANF: MSB
5CH	00H	LSB: Number Not Assigned
5EH	00H	MSB: Number Not Assigned
60H	15H	<b>CISTPL_VERS1</b>
62H	47H	TPL_LINK
64H	05H	TPLL1_MAJOR
66H	00H	TPLL1_MINOR
68H	45H	<b>E</b>
6AH	44H	<b>D</b>
6CH	49H	<b>I</b>
6EH	37H	<b>7</b>
70H	50H	<b>P</b>
72H	30H	<b>0</b>
74H	34H	<b>4</b>
76H	30H	<b>0</b>
78H	46H	<b>F</b>
7AH	4CH	<b>L</b>
7CH	56H	<b>V</b>
7EH	32H	<b>2</b>
80H	36H	<b>6</b>
82H	2DH	-
84H	2DH	-
86H	2DH	-
88H	31H	<b>1</b>
8AH	35H	<b>5</b>
8CH	20H	SPACE
8EH	00H	END TEXT
90H	43H	<b>C</b>
92H	4FH	<b>O</b>
94H	50H	<b>P</b>
96H	59H	<b>Y</b>
98H	52H	<b>R</b>
9AH	49H	<b>I</b>
9CH	47H	<b>G</b>

ADDRESS	VALUE	DESCRIPTION
9EH	48H	<b>H</b>
A0H	54H	<b>T</b>
A2H	20H	SPACE
A4H	45H	<b>E</b>
A6H	4CH	<b>L</b>
A8H	45H	<b>E</b>
AAH	43H	<b>C</b>
ACH	54H	<b>T</b>
AEH	52H	<b>R</b>
B0H	4FH	<b>O</b>
B2H	4EH	<b>N</b>
B4H	49H	<b>I</b>
B6H	43H	<b>C</b>
B8H	20H	SPACE
BAH	44H	<b>D</b>
BCH	45H	<b>E</b>
BEH	53H	<b>S</b>
C0H	49H	<b>I</b>
C2H	47H	<b>G</b>
C4H	4EH	<b>N</b>
C6H	53H	<b>S</b>
C8H	20H	SPACE
CAH	49H	<b>I</b>
CCH	4EH	<b>N</b>
CEH	43H	<b>C</b>
D0H	4FH	<b>O</b>
D2H	52H	<b>R</b>
D4H	50H	<b>P</b>
D6H	4FH	<b>O</b>
D8H	52H	<b>R</b>
DAH	41H	<b>A</b>
DCH	54H	<b>T</b>
DEH	45H	<b>E</b>
E0H	44H	<b>D</b>
E2H	20H	SPACE
E4H	00H	END TEXT
E6H	31H	<b>1</b>
E8H	39H	<b>9</b>
EAH	39H	<b>9</b>
ECH	37H	<b>7</b>
EEH	00H	END TEXT
FOH	FFH	END OF LIST