TW8823 – TFT Flat Panel Controller

with built-in 3D Video Decoder, Triple ADCs , Dual PIP and 16-bit OSD Support

Datasheet from Techwell, Inc.

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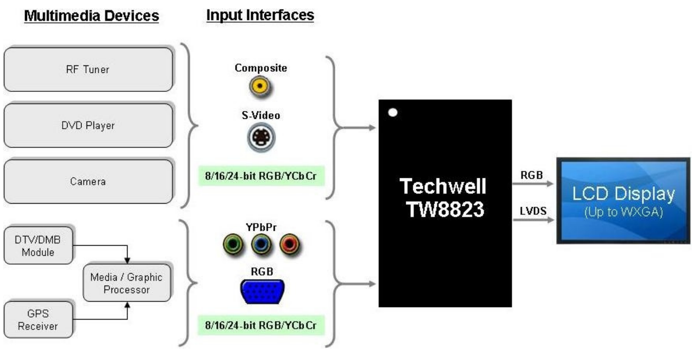
Introduction



Applications

In-car display controller
Portable DVD and DVRs players
Portable media player

Description

The TW8823 incorporates many of the features required to create multi-purpose in-car LCD display system in a single package. It integrates a high quality 3D comb NTSC/PAL/SECAM video decoder, triple high speed RGB ADCs, high quality scaler, bit-mapped OSD, triple DACs and images enhancement functions which include Black and White Stretch, favorite color enhancement and etc. It also supports panoramic scaling for conversion to wide screen display. On the input side, it supports a rich combination of CVBS, S-video, analog RGB as well as digital YCbCr/RGB inputs. On the output side, it supports both digital and analog panel type with its built-in timing controller and analog RGB output. It also support LVDS type panel.

TW8823 also has two PIPs (Picture in Picture) function that can display three display sources simultaneously on one single window. It also has built-in bit-mapped OSD with 16-bit color depth and acceleration function. It can also accept 18-bit external OSD input. In addition, TW8823 has built-in high performance microcontroller with cache. Its SPI interface supports various serial flash types.

Analog Video Decoder

- NTSC (M, 4.34) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection
- Two 10-bit ADCs and analog clamping circuit.
- Fully programmable static gain or automatic gain control for the Y or CVBS channel
- Programmable white peak control for the Y or CVBS channel
- Software selectable analog inputs allows either composite or S-video input
- High quality motion adaptive 3D comb filter for both NTSC and PAL with concurrent 3D noise reduction
- PAL delay line for color phase error correction
- Image enhancement with 2D dynamic peaking and CTI.
- Digital sub-carrier PLL for accurate color decoding
- Digital horizontal PLL and Advanced synchronization processing for VCR playback and weak signal performance.
- Programmable hue, brightness, saturation, contrast, sharpness.
- High quality horizontal and vertical filtered down scaling with arbitrary scale down ratio
- Detection of level of copy protection according to Macrovision standard

Analog RGB Inputs

- Triple high speed 10-bit ADCs with clamping and programmable gain amplifier.
- SOG and H/V sync support for YPbPr or RGB input
- Built-in line locked PLL with sync separator
- Support analog input resolution up to 1080i or WXGA

Dual Digital Inputs Support

- Dual channel digital inputs support with following combination:
  - 1 channel 18/16-bits inputs and 1 channel 8-bits inputs
  - 1 channel 24 bits digital RGB/YCbCr inputs
- Support both 656 and 601 video formats
- Allows connection to external HDMI receiver

Built-in Microcontroller

- Built-in 8052 MCU up to 72MHz clock
- Built-in code cache memory to enhance CPU performance.
- Support Single/Dual/Quad IO SPI Flash
- System programming through UART
- Support SPI DMA Read/Write to OSD memory
- Support I2C Master interface with GPIO
- Support two UART interface up to 115200bps

- Support IR receiver and interrupt output

TFT Panel Support

- Built-in both analog and digital timing controller with programmability.
- Supports optional single channel LVDS panel with resolution up to WXGA, 80Mhz
- Supports 3, 4, 6 or 8 bits per pixel up to 16.8 million colors with built-in dithering engine
- Support analog panel with resolution up to WQVGA, 20Mhz

On Screen Display

- Supports three window bitmapped OSD, one 16 bits and two 8 bits bitmap OSD.
- Built-in OSD controller with Bit blit Engine
- Supports variety functions included like blinking, transparency and blending.
- Supports External OSD with external alpha blending control.
- Support OSD compression

Image Processing

- High quality scaler with both up/down and nonlinear scaling support
- Built-in 2D de-interlacing function
- Programmable hue, brightness, saturation, contrast
- Sharpness control with vertical peaking up to +12db
- Programmable color transient improvement control
- Supports programmable cropping of input video and graphics.
- Independent RGB gain and offset controls
- Panorama / Water-glass scaling
- DTV hue adjustment
- Programmable 10-bit Gamma correction for each color
- Operated in Frame Sync mode only
- Black/White Stretch
- Programmable favorite color enhancement

PIP Function

- Two independent PIPs
- Variable sub window size
- POP with alpha blending
- Support both 16-bit YPbPr and RGB data format
- Built-in high quality up and down scaling engine for PIP

DDR-SDRAM

- Support 16 bits 155MHz DDR-SDRAM up to 256 Mb

Host Interface

- Supports 2-wire serial bus interface
- Supports 8-bits Parallel Host Interface

Clock Generation

- Frequency synthesizer with spread spectrum generate DDR memory and display clocks
- Spread spectrum profile based on triangular modulation with center spread
- Modulation frequency and spread width can be selectable

Power Management

- Supports Panel power sequencing.
- Supports DPMS for monitor power management.
- 1.8 / 2.5V / 3.3 V operation

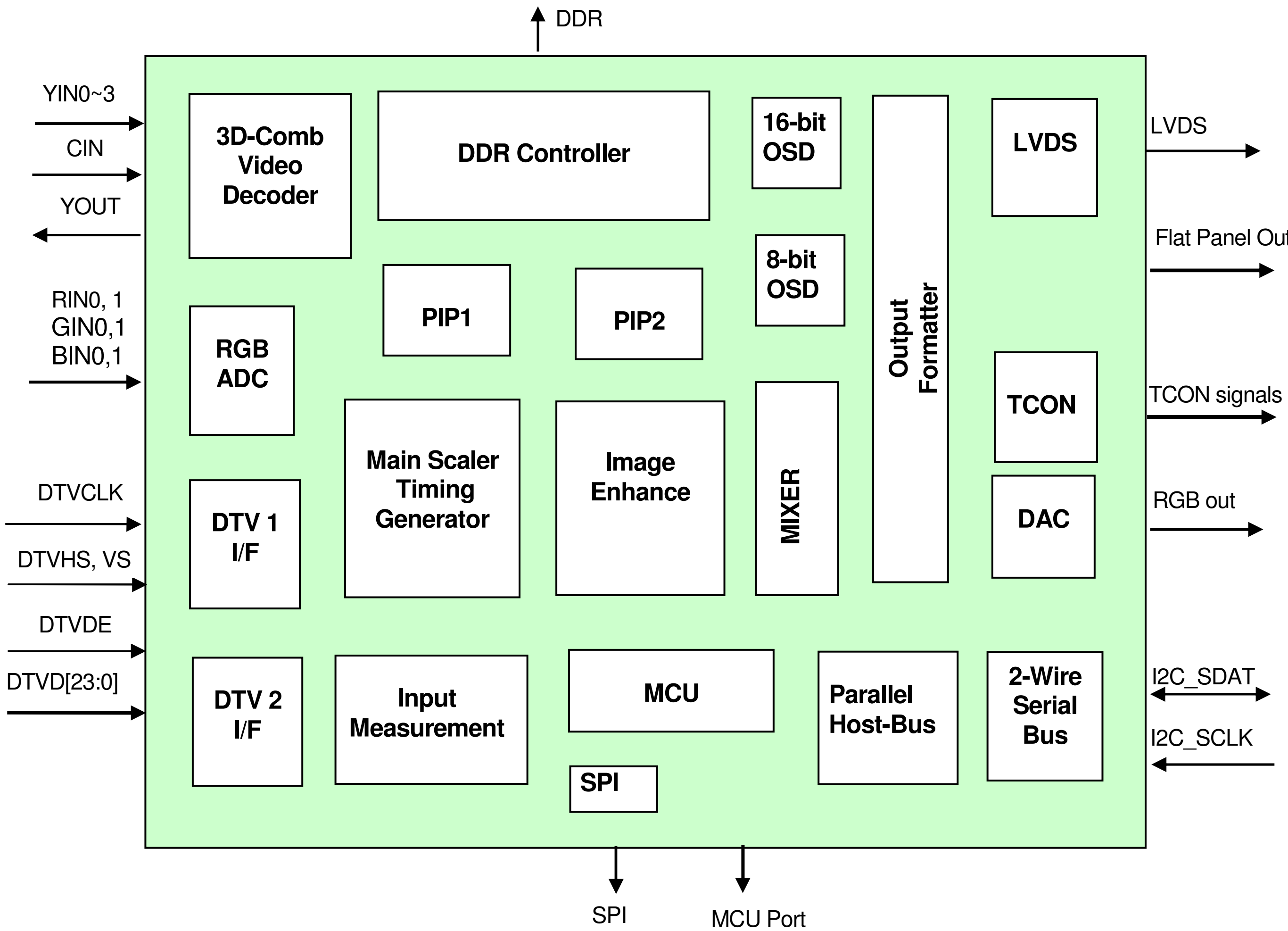
Miscellaneous

- Built-in single CCFL back light controller
- Built-in single LED back light controller
- Built-in Touch screen controller with 12-bit ADC
- LVR, provides 100~200 msec. low voltage reset
- Power-down mode
- Single 27MHz crystal
- 216-pin LQFP package

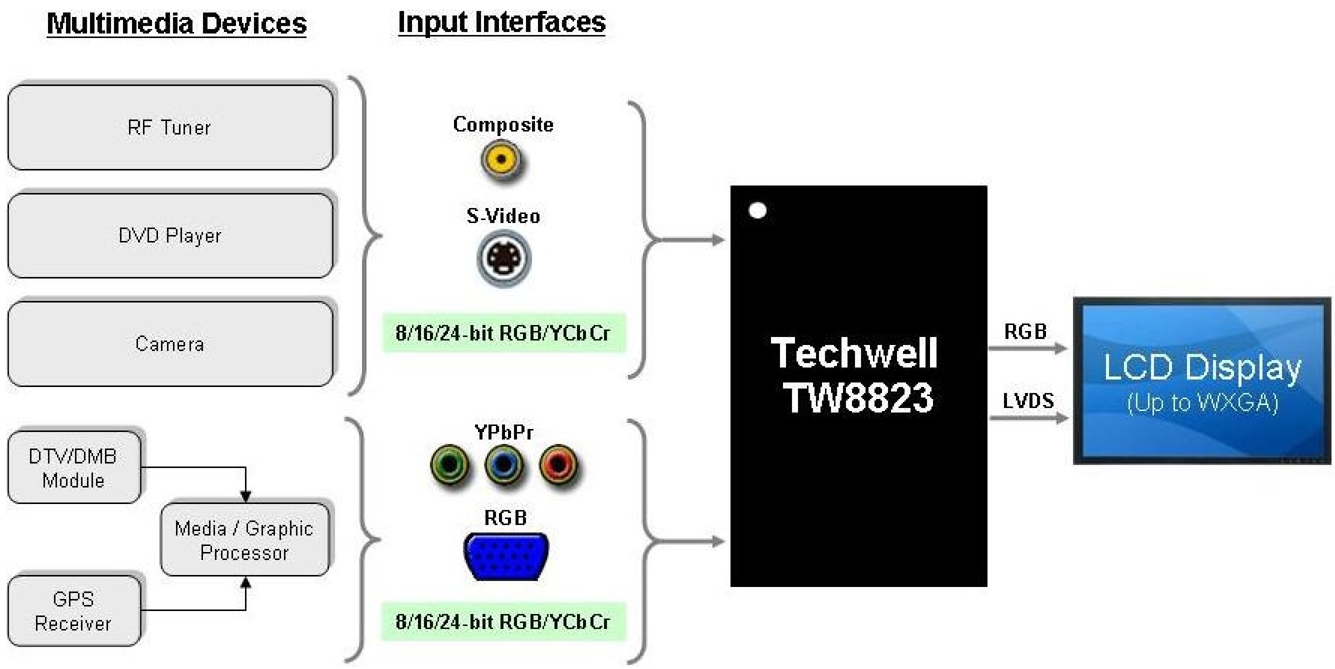
Order Information

Package Description

Part #	Name	Description	Pin Count	Body Size
	LQFP 216	Low Profile Quad Flat Package	216	24 x 24 mm^2



TW8823 Flat Panel TV/Monitor controller functional block diagram



TW8823 Flat Panel TV or TV + PC Monitor system

Functional Description

Overview

Techwell's TW8823 Flat Panel TV/Monitor controller is a highly integrated TFT panel controller. It integrates a high quality 3D comb NTSC/PAL/SECAM video decoder, triple high speed RGB ADC, single channel LVDS, dual scalers for PIPs support, timing controller, triple DACs and flexible bit-mapped OSD engine. This unique level of mixed signal integration turns a TFT panel into a flexible display system. Its built-in triple ADCs and PLL allow both YPbPr and RGB input support. Separate flexible digital inputs interface also allow it to connect other front-end chips. It incorporates easy-to-operate and powerful features in a single package for multi-purpose in-car LCD display, portable DVD and DVRs media players.

The TW8823 contains all the logic required to convert standard TV, DTV, and PC monitor signals to the digital control and data signals required to drive various TFT panel types. It supports LVDS panel resolutions up to WXGA(1366x768), 80MHz, as well as analog TFT panel resolutions up to WQVGA(480 x 234), 20MHz.

The chip accepts CVBS (composite) analog input or S-video analog input or analog RGB input for use as a video monitor and up to 11 analog inputs can be connected simultaneously..

The integrated analog front-end contains total five ADCs with clamping circuits and Automatic Gain Control (AGC) circuit on certain channel to minimize external component count. It employs proprietary 3D Comb filter Y/C processing technologies to produce exceptionally high quality pictures.

TW8823 has three high speed ADCs that can support various analog signal inputs up to 1080i or WXGA.

The chip's internal logic synchronizes the panel frame rate to the incoming input frame rate. A high quality image-scaling engine is used to convert the lower resolution formats or high resolution DTV formats to the output panel resolution. An internal de-interlacing engine also allows interlaced video to be supported.

On Screen Display is supported through either external OSD chip or on-chip OSD for maximum flexibility. The TW8823 also accepts a 24 bit digital RGB input from external HDMI™ receiver or ADCs. In addition, it accepts 8/16/24 bits digital YCbCr input.

The TW8823 has a built-in LVDS transmitter for direct connecting with various LCD panel. For the variety for usage, TW8823 has a built-in TCON for direct connecting with low cost TCON-less panel.

The TW8823 also supports TFT panel power sequencing, DPMS (VESATM Display Power Management Signaling) signaling and power management. It also has built-in single channel CCFL or LED back light controller to further simplify the system design. Besides, built-in touch screen controller in TW8823 can provides accurate position reading with simplified digital operation and can also be used to monitor up to four auxiliary analog inputs. The control interface supports both a 2-wire serial bus interface and 8bit parallel interface. In addition, TW8823 has built-in high performance Microcontroller with cache, and its SPI interface supports various serial flash types. The TW8823 core operates at 1.8 V, the IO at 2.5V and 3.3 V. TW8823 packaged in a 216-pin LQFP package.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are five analog front-end channels. Two channels are dedicated to analog video support. Every channel contains analog anti-aliasing filter, clamping circuit and 10-bit ADCs. It allows the support of CVBS, S-video input signals for main or sub display. The other three channels are dedicated to YPbPr component video or RGB input support. Every channel contains the analog clamping circuit, variable gain amplifier and ADCs. It allows three separate inputs to be connected simultaneously. A built-in line locked PLL is used to generate the sampling clock for various inputs.

Video Source Selection

TW8823 has total 11 analog inputs for maximum flexibility. Of the 11 inputs, 6 are used for 2 channels of YPbPr/RGB input with corresponding SOG pin. The other 5 inputs are used by video decoder to allow up to 4 CVBS or 1 S-Video input. All inputs are software selectable.

Clamping and Automatic Gain Control

All five channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a programmable level. The C channel restores the back porch of the digitized video to a level of 128. The R, G, and B channels restore the blank to a level of 16. This operation is automatic through internal feedback loop.

In the case of RGB channel, two clamping modes are provided. When the input is YPbPr signal, the clamping to pre-determined DC level is done through internal feedback loop. When the input is PC RGB signal, the input is self clamped to the zero level.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. The white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Video Decoder

Sync processor

TW8823 has two sync processors, one for RGB channel and one for video channel. The sync processor of video input detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-Video signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. It has wide lock-in range for tracking any non-standard video signal.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. A detection window controls the determination of sync. This provides more reliable synchronization. It simulates the functionality of a PLL without the complexity of a PLL. The field status is determined at vertical synchronization time based on the vertical and horizontal sync relationship.

Color Decoding

Y/C separation

The color-decoding block contains the luma / chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma / chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter can be found in the filter curve section.

In the case of comb filter, the TW8823 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 3D/2D adaptive comb filter. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color demodulation

The color demodulation for NTSC and PAL standard is done by quadrature mixing the chroma signal to the base band and extracting the chroma components with low-pass filter. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM color demodulation process consists of bell filtering, FM demodulator and de-emphasis filtering. The chroma carrier frequency is identified in the process and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by transmission loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then compensated in amplitude accordingly. The range of ACC control is –6db to +24db.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be "killed". The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

Automatic standard detection

The TW8823 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

TW8823 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by the TW8823

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.58 MHz	Japan
PAL-B, G, N	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	3.58 MHz	Brazil
PAL-CN	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43 MHz	China
NTSC (4.43)	525	60	4.43 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The TW8823 decoder adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW8823 decoder also provides a sharpness control function through a control register. The center frequency of the peaking filter is selectable. A coring function is provided along with the sharpness control to reduce enhancement to the noise.

The Hue and Saturation

When decoding NTSC signals, TW8823 decoder can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Analog RGB / YPbPr Processor

Analog Front-end

This input path has three ADCs to support analog RGB input or YPbPr input. The built-in clamping circuit works based on the mode selected. Every channel includes variable gain amplifier for gain adjustment. Both gain and offset can be adjusted for flexibility. Two software selectable inputs are available for each channel to allow two inputs to be connected simultaneously. Both separated H/V sync and sync-on-green are supported.

Sync Processor

The sync processor for the RGB channel either takes the separated H/V sync input or separates the composite sync input from one of the SOG inputs into H/V sync for driving the on-chip sampling PLL. It contains necessary logics to detect and bypass irregular syncs. The on-chip PLL has sub-phase control to enable accurate sampling timing.

Component Processor

There are built-in color space converter and tint control logic for the YPbPr input. During YPbPr component input operation, luminance Contrast and Brightness as well as Pb / Pr Saturation can be controlled by registers. In the case of RGB mode, the gain and offset of RGB can also be digitally controlled.

Touch Screen Controller

Built-in 12-bit ADC touch screen controller in TW8823 provides accurate position reading with simplified digital operation and can also be used to monitor up to four auxiliary inputs with touch interrupt.

Digital Input Support

In addition to analog inputs, the TW8823 has dual digital inputs mode for YCbCr or RGB data. The combination could be either one channel 18/16-bit and one channel 8-bit at dual digital input mode or a single 24-bit digital inputs mode. The input includes VSYNC, HSYNC, pixel clock and the optional data qualifier. For interlaced video, the timing relationship between VSYNC and HSYNC determine the field flag. The optional data qualifier is needed when input video data is not continuously valid within a line. For the YcbCr mode, TW8823 can support 8-bit 656 as well as 8/16-bit 601 modes. The 656 interface supports both interlaced and progressive standard.

TFT Panel Support

The TW8823 supports varieties of active matrix TFT panels including LVDS panel resolutions up to WXGA(1280x768), 80MHz, as well analog panel resolutions up WQVGA(480 x 234) , 20MHz.

Dithering

If the color depth of the input data is larger than the LCD panel color depth, the TW8823 can be set to dither the image. Up to four bits of apparent color depth can be added with the internal dithering ability of the TW8823. This allows LCD panels with 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel to can display up to 2.1 million colors.

The TW8823 has both spatial and frame modulation dithering. When dithering with the least significant 4-bits of input data the TW8823 uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, the TW8823 uses either spatial modulation with 2x2 pixel blocks, or frame modulation.

LVDS out put format

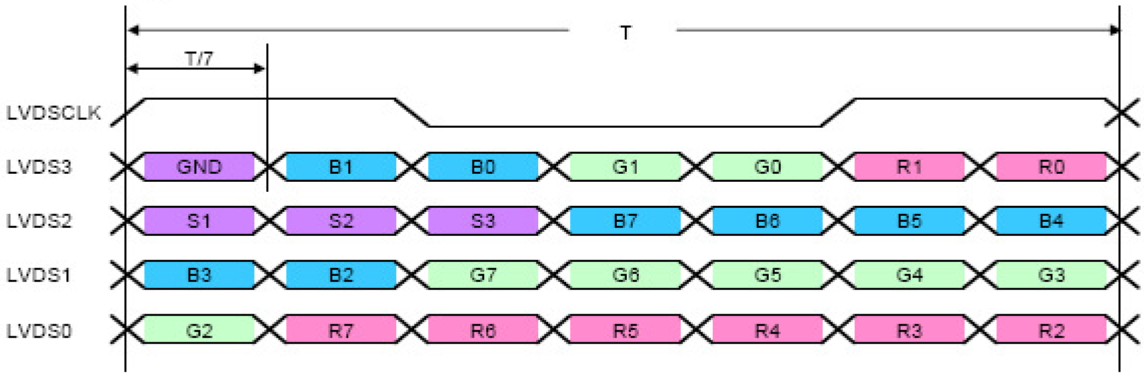
TW8823 is able to control output order for panel control signal that VS, HS and DE.

CTL_MAP	S1	S2	S3
0	DE	VS	HS
1	VS	HS	DE
2	HS	DE	VS
3	DE	VS	HS
4	DE	HS	VS
5	HS	VS	DE
6	VS	DE	HS
7	DE	VS	HS

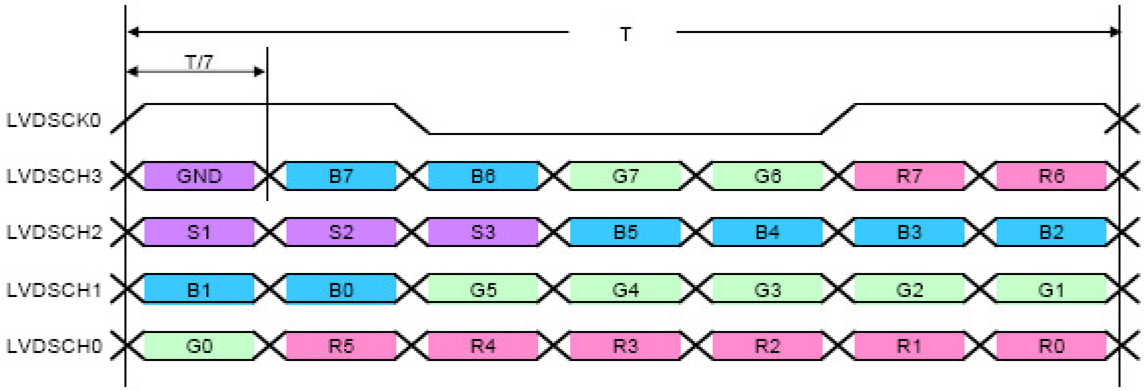
LVDS Color Mapping

TW8823 is able to control output color order.

SEL_LVDS=00, 11



SEL_LVDS=01



SEL_LVDS=10

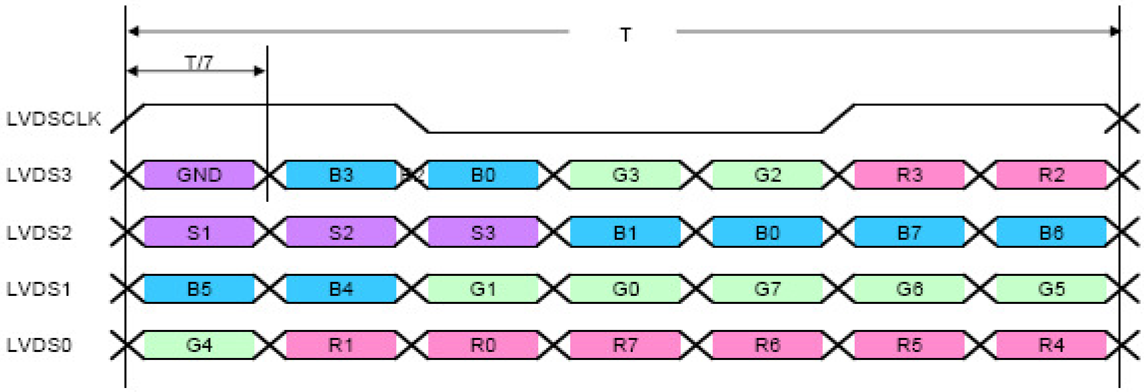


Image Control

Input Image Control

The input cropping control provides a way for programming the active display window region for the selected input video or graphic. In the normal operation, the first active line starts with the VSYNC signal. This and vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in one pixel increments for single pixel input mode or two pixels increments for double pixels input mode. If data qualifier is used, then only qualified pixels will be counted in the window size.

Image Scaling

The TW8823 internal image-scaling engine operates in several modes. The first is the bypass mode. No image scaling is done in this mode. The number of active output lines per frame and the number of active output pixels per line are identical to the input active lines and pixels, respectively. This mode is best used for displaying computer graphic at panel's native resolution.

By default, the input active window is zoomed up to the full screen for display. This is used for non-interlaced data like PC graphics or progressive scan video. The vertical and horizontal magnification ratio can be adjusted independently. TW8823 has frame-sync mode which does not use frame buffer. In this mode, the zoom ratio and output clock rate should be coordinated appropriately to avoid internal buffer overrun.

The TW8823 has a de-interlacing mode to process interlaced video inputs. In this mode, every input field is zoomed to the full output frame resolution. The de-interlaced fields can also be properly compensated to have fields aligned correctly to avoid any artifacts. The offset can be programmed to provide maximum flexibility.

The horizontal scaler can be programmed to perform non-linear scaling : panorama scaling for displaying 4:3 input on a 16:9 display and water-glass scaling for displaying 16:9 input on a 4:3 display.

Image Enhancement Processing

Adaptive Black/White Stretch

This feature is to expand dynamic range of the input image, which creates more vivid image impression.

Favorite Color enhancement

TW8823 provides three independent color enhancements. The center axis of each color can be adjusted over a 360 degrees range provided none of those two are overlapped. The range and the amount of enhancement can also be independently adjusted.

Picture-In-Picture

Double Window / Picture-in-Picture (PIP)

TW8823 can display two live pictures on a single display. In the case of what we called PIP, small size of sub-window can be displayed over full size of main-window.

The frame (outline of window) can be added with choice of color and width.

Example of double window modes

PIP alpha blending

PIP image can be used as an OSD type overlay graphics. User can specify specific color as a 'key color' which disabling overlaying and showing behind main image. Where PIP and main image are overlaid, user can define blending ratio (Alpha1). And also can define blending ratio of main image with Black color (Alpha2) as a dimming function.

[Usage]

- Enable PIP alpha blending (0x8280[7] = 1). Enable 565 mode (0x8280[6] = 1) as well, if it is preferred.

- Set 'Key color' center level by using Rkey (0x8282), Gkey (0x8283) and Bkey (0x8284). Also set 'Key range' (0x0685~0x0687) for the 'Key color' deviation from its center setting.

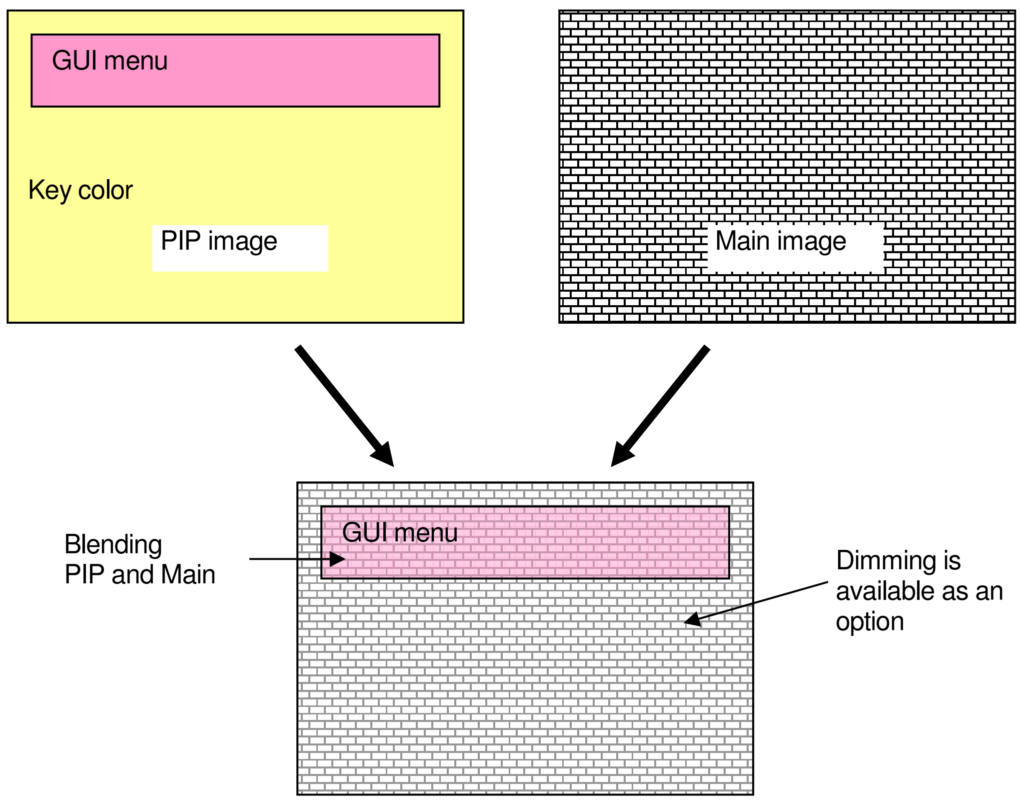
- Turn on 'Key position display' mode if you want to make sure the area detected as 'Keyed'.

- Adjust Alpha1 (0x8280[4:0]) and Alpha2 (0x8281[4:0]).

[Limitations]

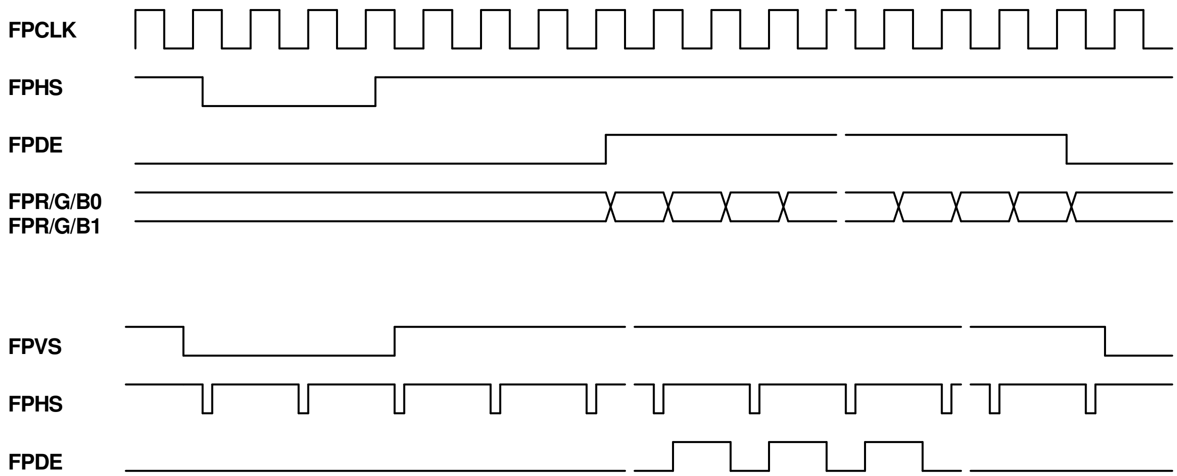
- When 565 mode, color depth is limited and may show steps on original gradation.

- When 565 mode, try to choose color of input image which truncated portion (LSB 2 bit will be truncated in Y, LSB 3 bit in Cb and Cr) has about middle value (If 3 bit is truncated, these portion better have value of around 3 or 4) to avoid input level translated into 2 different output level due to noise. (If input is digital signal, this situation may be avoidable.)



Display Timing

The TW8823 is operated in Frame Sync mode only with no external memory required. In this mode, the output frame rate is synchronized with the input frame rate. Since there is no frame buffer, the display clock frequency and zoom ratio have to be properly selected to match the panel resolution. The internal scaling engine absorbs the difference between the input line rate and output line rate as well as the difference between the input pixel rate and output pixel rate.



Flat Panel Output Signals

The frequency of the Flat Panel Clock Output pin can be controlled by an internal frequency synthesizer. It also has spread spectrum function to reduce EMI. The frequency equation of the Flat Panel Clock Output signal is described in the register section.

External DDR SDRAM Interface

TW8823 uses a unified external DDR SDRAM for various functions, such as bit-mapped OSD, 3D comb, 3D noise reduction and PIP. The memory controller of the TW8823 supports 16bit data width. The memory capacity can be up to 256 Mbytes.

When the chip is powered up, the CPU is responsible for setting all the on-chip configuration registers for DDR memory configuration. Once the registers are set, the CPU releases the software reset signal, then the DDR memory controller initializes the DDR memory configuration using the parameters in the registers. After the initialization is done, the DDR memory is ready for use. The memory controller does the memory refresh automatically.

On Screen Display

TW8823 OSD controller supports bitmap with 8/16 Bit-per-pixel mode up to 3 windows, one 16-bits and two 8-bits mode. Between 8-bits and 16-bits windows, color could be blended by OSD alpha blending controller. The powerful Bit-Blit Engine makes your system more fancier. Any pixel in an 8 bit OSD window can be assigned any one of 256 user-defined true colors through a 256 x 32 bits Look-Up-Table. Two Look-Up-Tables are available; one for each 8 bit OSD window.

The bitmap is loaded into external SDRAM by MCU write operation or OSD block fill operation. User can define the displayed pixel colors on a pixel by pixel basis. The pixels can be represented using either 8-bits or 16-bits per pixel. Alpha blending can be on either per pixel based or per window based. The maximum bitmapped image size depends on panel resolution and SDRAM size. .

External OSD port

A dedicated port is provided for an external OSD controller. The TW8823 provides the HSYNC, VSYNC and dot clock signals, and external OSD controller provides a 18 bits color data values together with valid data indicator (6 bits for each R, G and B color). It's compatible with popular OSD controllers from Renesas (Mitsubishi) and other companies.

In case of 18 bit OSD data reception, color palette is not used and 18 bit data represents 262144 color space directly. External OSD port share with MCU GPIO ports and DTV input ports.

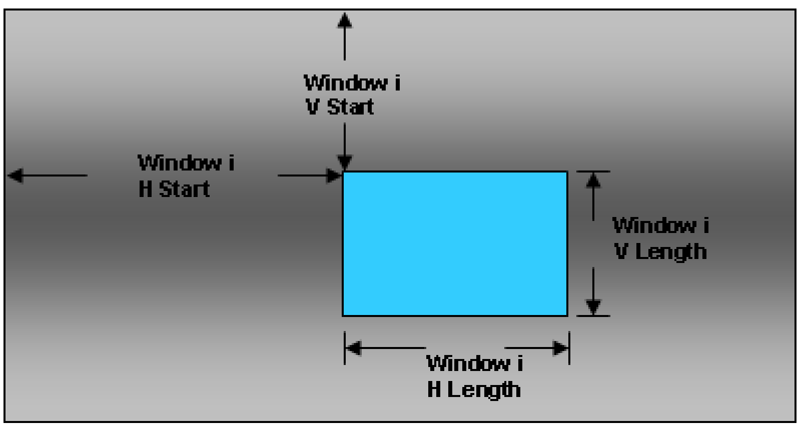
OSD Display and Image in Memory

The TW8823 OSD provides a flexible mapping between its display on the LCD and its image stored in the memory. In general a working space in the memory is defined for each window. The working space is much larger than the display size of the window. Multiple images can be stored in a working space. Pointers are provided to point to the starting location of the image to be displayed. Animation can be achieved by changing the pointers during the vertical blanking times.

Window Display Starting Location and Sizes

There are four registers used to specify the staring location and size on the LCD:
Window i Horizontal Start
Window i Vertical Start
Window i Horizontal Length
Window i Vertical Length

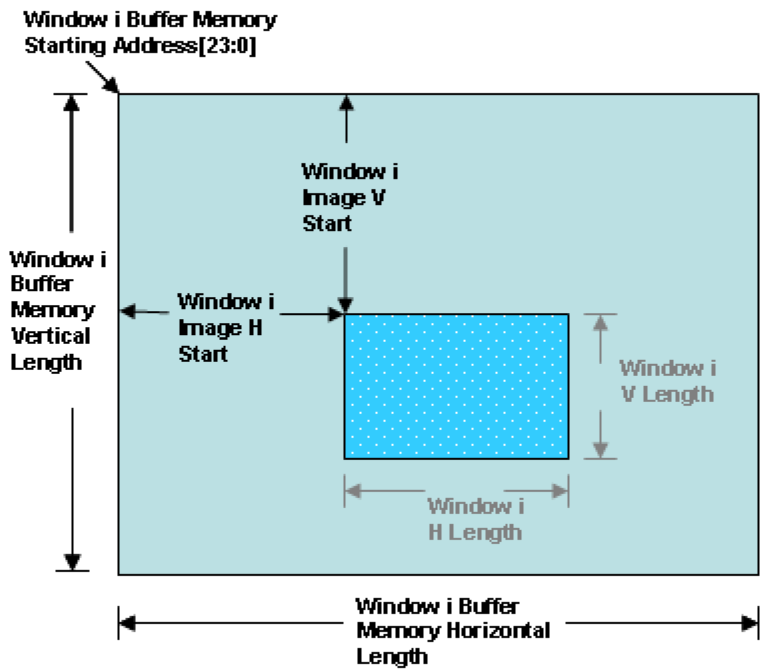
LCD Display



Window Working Space

Three registers together define the working space starting location and boundaries:
Window i Buffer Memory Starting Address
Window i Buffer Memory Horizontal Length
Window i Buffer Memory Vertical Length

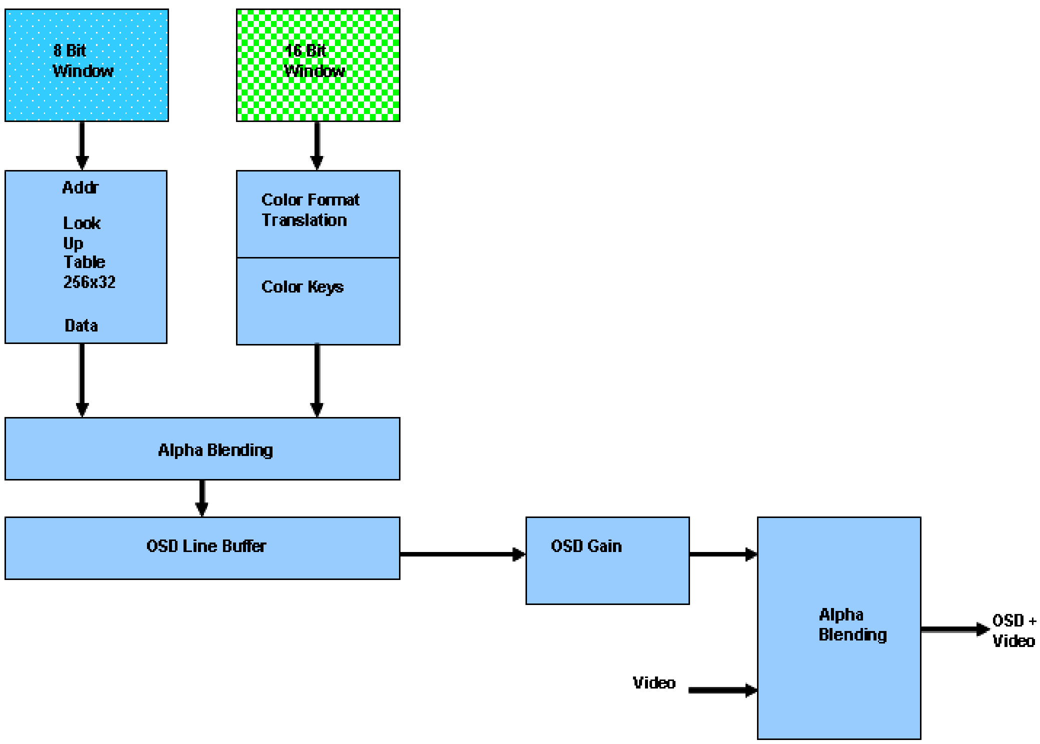
Two registers point to the starting location of the image stored:
Window i Image Vertical Start
Window i Image Horizontal Start



The above registers are per window based.
All horizontal length definitions are on per pixel base. The internal hardware takes into account 8-bit (one byte) or 16-bit (2 bytes) variation.
Different windows can share the same working space.

OSD Display Path

Two 8-bit windows, window 0 and window 1, are provided. Each has its own look up table.
When these two windows are overlapped, widow 0 has higher priority; i.e. the overlapped window 1 area will not show up on the LCD.
The look up table maps the 8 bit value stored in the memory to a 32 bits content, which consists of blink attribute, per pixel alpha value, and 24-bit RGB value.
One 16-bit window is provided. It supports five different formats: YCbCr422, YCbCr655, RGB565, RGB4444, and RGB1555.
A 16-bit pixel data fetched is converted to a 24-bit RGB. The resulting 24-bit RGB data is blended with the 24-bit RGB from the 8-bit window if the 8-bit window is overlapped with the 16-bit window. The blended OSD pixel and alpha values are then stored in a line buffer.
The line buffer is later shifted out to display. While it is shifting out the OSD pixel data is blended with the incoming video data.



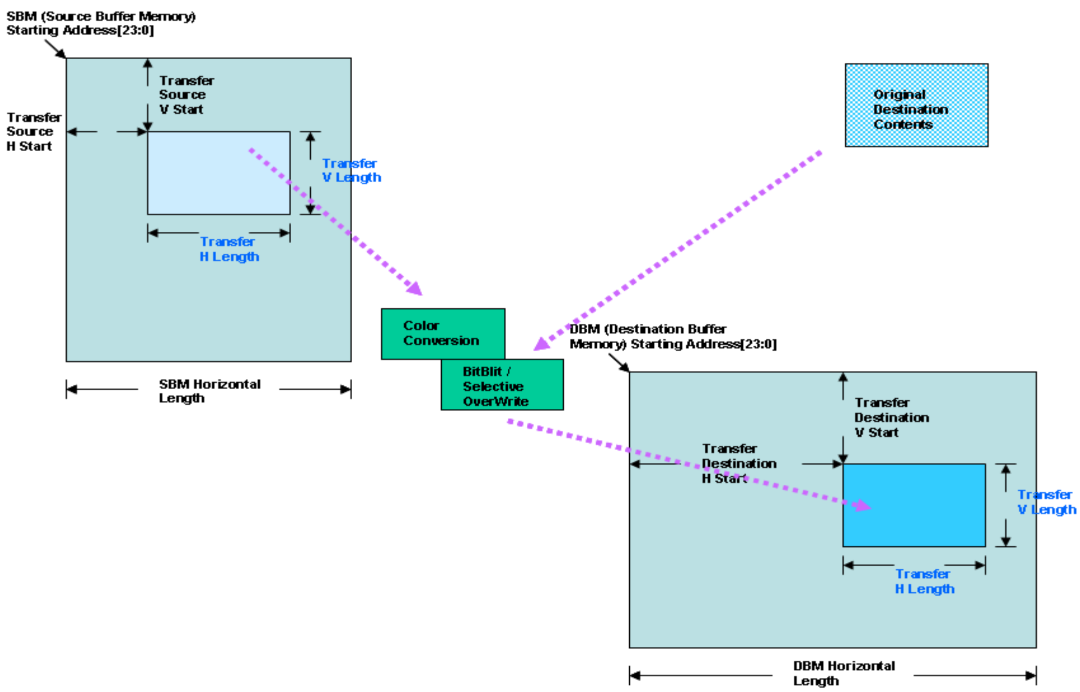
OSG Operation I – Block Fill
In the simplest Block Fill operation, the data in the Block Fill Color register is repeatedly used to fill up the destination region. For more advanced Block Fill operation, one can invoke the Color Conversion, Selective OverWrite, and BitBlt functios.

To perform the Block Fill, set the following registers properly.
OSGMODE (0x0700[7:6]) = 10
BEXPM (0x0700[1:0]) = 00
RLC Function Enable (0x0704[0]) = 0
Destination Buffer Memory Starting Address (0x0770 ~ 0x0772)
Destination Buffer Memory Horizontal Length (0x0773)
Transfer Destination Horizontal Start (0x0774 ~ 0x0775)
Transfer Destination Vertical Start (0x0776 ~ 0x0777)
Transfer Horizontal Length (0x0768 ~ 0x0769)
Transfer Vertical Length (0x076A ~ 0x076B)
Block Fill Color (0x070E ~ 0x070F)
MSKSEL (0x0700[5:4])
COLOR_CON (0x0700[3])
BPP (0x0700[2])

If any one of the functions, Color Conversion, Selective OverWrite, BitBlt, is selected, the additional register corresponding that function needs to be set properly.

To start the operation, write "1" to
OP_START (0x0701[0])

While the Block Fill operation is in progress, the
OSG_STUS (0x0701[7])
stays at "1" until it is done.
When the **OSG_STUS** returns to "0", write "0" to
OP_START to conclude the operation.



OSG Operation II – MCU/DMA Write
The MCU/DMA Write operation provides the means to import an existing image to the OSD. In addition to the Color Conversion, Selective OverWrite, and BitBlt functions, one can invoke Bit Expansion, Special 8 To 16 Bit Expansion, and RLC Decompression.
The MCU Write is carried out by writing data to the Data Port for MCU Write register (0x0702), while the DMA Write is carried out by SPI DMA tunnels its data to OSD directly. Either way the data is directed to a 64-byte FIFO. As soon as the FIFO is filled, the actual operation commences. Additional data is accepted when the FIFO becomes empty. One must ensures that there are enough data to fill up the destination block area, defined by Transfer Vertical Length and Transfer Horizontal Length.

To perform the MCU/DMA Write, set the following registers properly.
OSGMODE (0x0700[7:6]) = 00
Destination Buffer Memory Starting Address (0x0770 ~ 0x0772)
Destination Buffer Memory Horizontal Length (0x0773)
Transfer Destination Horizontal Start (0x0774 ~ 0x0775)
Transfer Destination Vertical Start (0x0776 ~ 0x0777)
Transfer Horizontal Length (0x0768 ~ 0x0769)
Transfer Vertical Length (0x076A ~ 0x076B)
MSKSEL (0x0700[5:4])
COLOR_CON (0x0700[3])
BPP (0x0700[2])
BEXPM (0x0700[1:0])
SP8TO16 (0x0703[4])
RLC Function Enable (0x0704[0])

If any one of the functions, Color Conversion, Selective OverWrite, BitBlt, Bit Expansion, Special 8-To-16 Bit Expansion, RLC Decompression, is selected, the additional register corresponding that function needs to be set properly.

MCU Write

To start the MCU Write operation, write “1” to
OP_START (0x0701[0]).
Once this bit is set the
OSG_STUS (0x0701[7]) becomes “1”.

Write 64-byte data to
Data Port for MCU Write (0x0702)

Check the
FIFO_STUS (0x0701[6])
Wait till it becomes “0”, then write the next 64-byte data.

Upon finishing the last byte data write, write “1” to
MCUWD (0x0701[1])
This makes the internal circuitry to fill up the destination area if the destination area is not fully filled yet.

Check the
OSG_STUS (0x0701[7])

If it becomes “0”, write “0” to both
OP_START (0x0701[0]) and **MCUWD** (0x0701[1])
to conclude the operation.

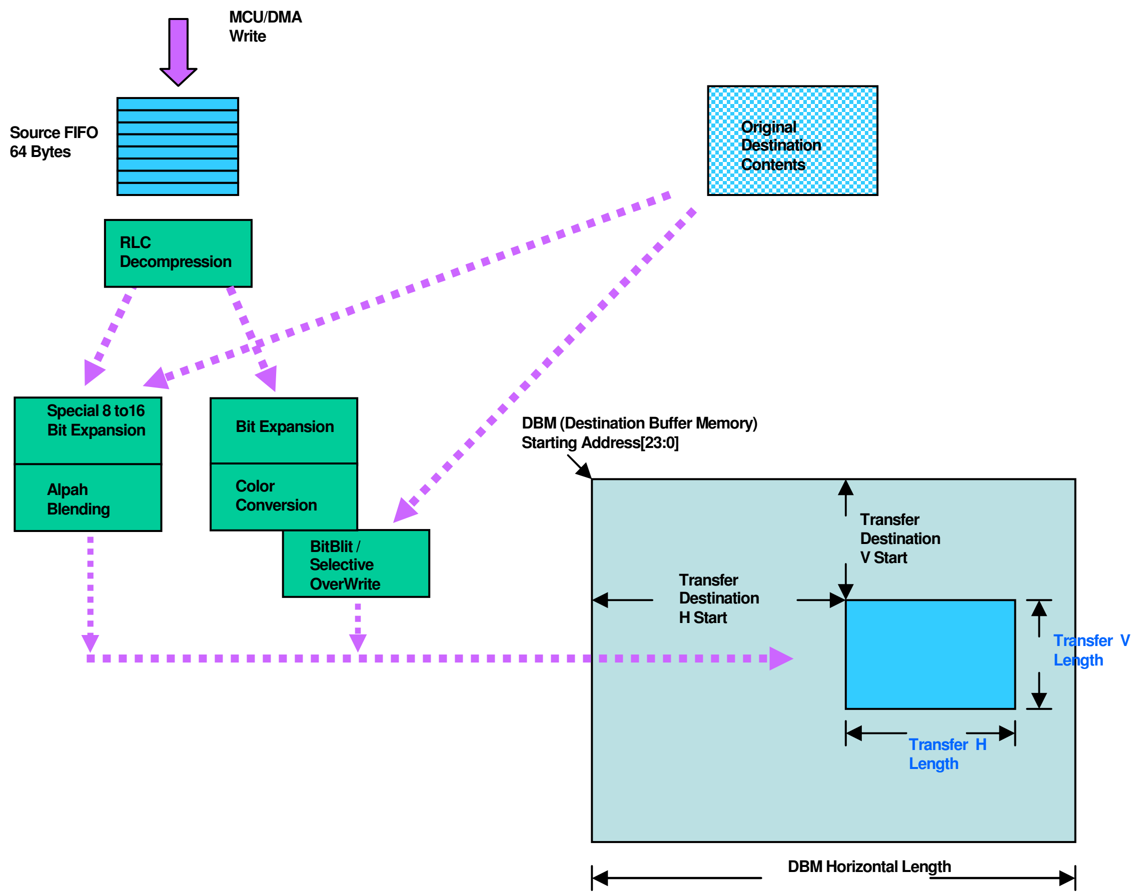
DMA Write

To start the DMA Write operation, write “1” to both
OSD_HW (0x0703[6]) and
OP_START (0x0701[0]).
(Thereafter the **OSG_STUS** (0x0701[7]) would change to “1”.)

Set up the SPI DMA to perform DMA read SPI data (refer to MCU operation documents)

Upon the SPI DMA operation is done (refer to MCU document), check
OSG_STUS (0x0701[7])

If it becomes “0”, write “0” to
OP_START (0x0701[0])
to conclude the operation.



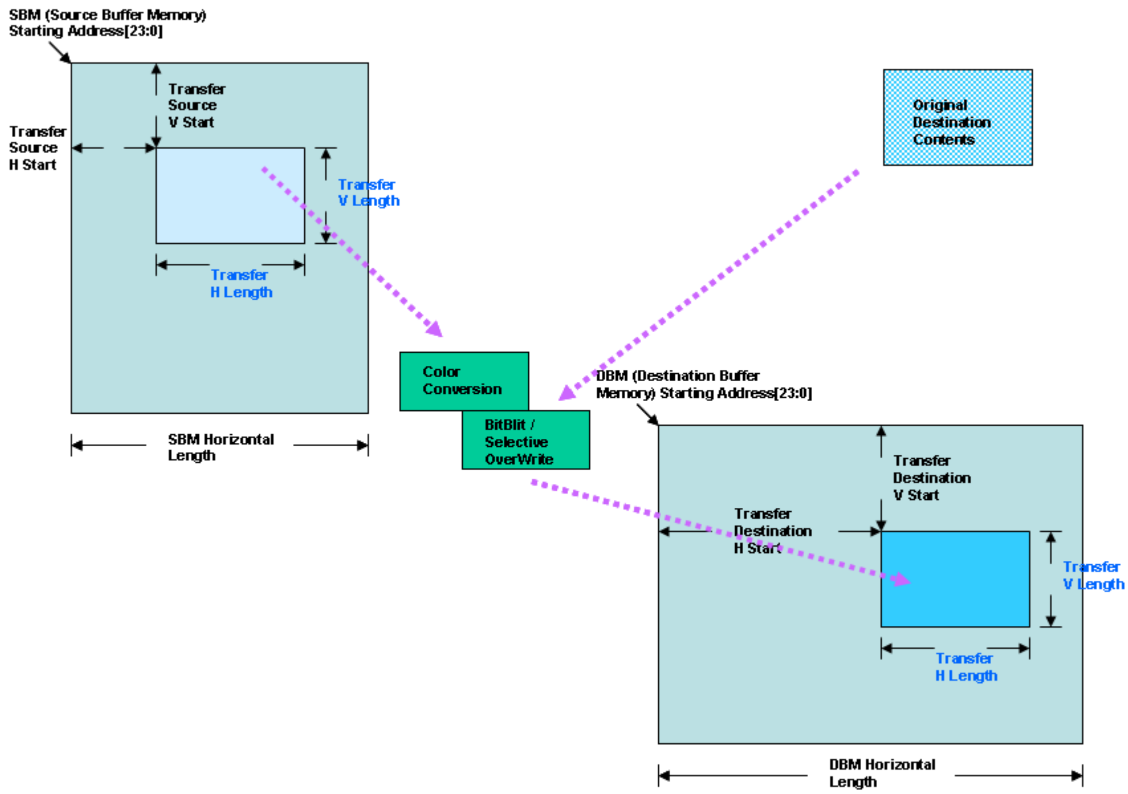
OSG Operation III – Block Transfer
Block Transfer is used to transfer a block (rectangular shaped) of data from one place to another. Functional operations available during block transfer are Color Conversion, Selective OverWrite, and BitBlt. The source block of data as well as the destination block of data are fetched and functionally operated. The resultant block of data is then written back to the destination.

To perform the Block Transfer, set the following registers properly.
OSGMODE (0x0700[7:6]) = 01
BEXPM (0x0700[1:0]) = 00
RLC Function Enable (0x0704[0]) = 0
Source Buffer Memory Starting Address (0x0760 ~ 0x0762)
Source Buffer Memory Horizontal Length (0x0763)
Transfer Source Horizontal Start (0x0764 ~ 0x0765)
Transfer Source Vertical Start (0x0766 ~ 0x0767
Destination Buffer Memory Starting Address (0x0770 ~ 0x0772)
Destination Buffer Memory Horizontal Length (0x0773)
Transfer Destination Horizontal Start (0x0774 ~ 0x0775)
Transfer Destination Vertical Start (0x0776 ~ 0x0777)
Transfer Horizontal Length (0x0768 ~ 0x0769)
Transfer Vertical Length (0x076A ~ 0x076B)
MSKSEL (0x0700[5:4])
COLOR_CON (0x0700[3])
BPP (0x0700[2])

If any one of the functions, Color Conversion, Selective OverWrite or BitBlt is selected, additional register(s) corresponding that function needs to be set properly.

Block Transfer

To start the Block Transfer operation, write "1" to
OP_START (0x0701[0]).
Check the
OSG_STUS (0x0701[7]).
If it becomes "0", write "0" to
OP_START (0x0701[0])
to conclude the operation.


SBM (Source Buffer Memory)
Starting Address[23:0]
Transfer
Source
V Start
Transfer
Source
H Start
Transfer
V Length
Transfer
H Length
SBM Horizontal
Length
Original
Destination
Contents
Color
Conversion
BitBlit /
Selective
OverWrite
DBM (Destination Buffer
Memory) Starting Address[23:0]
Transfer
Destination
V Start
Transfer
Destination
H Start
Transfer
V Length
Transfer
H Length
DBM Horizontal
Length

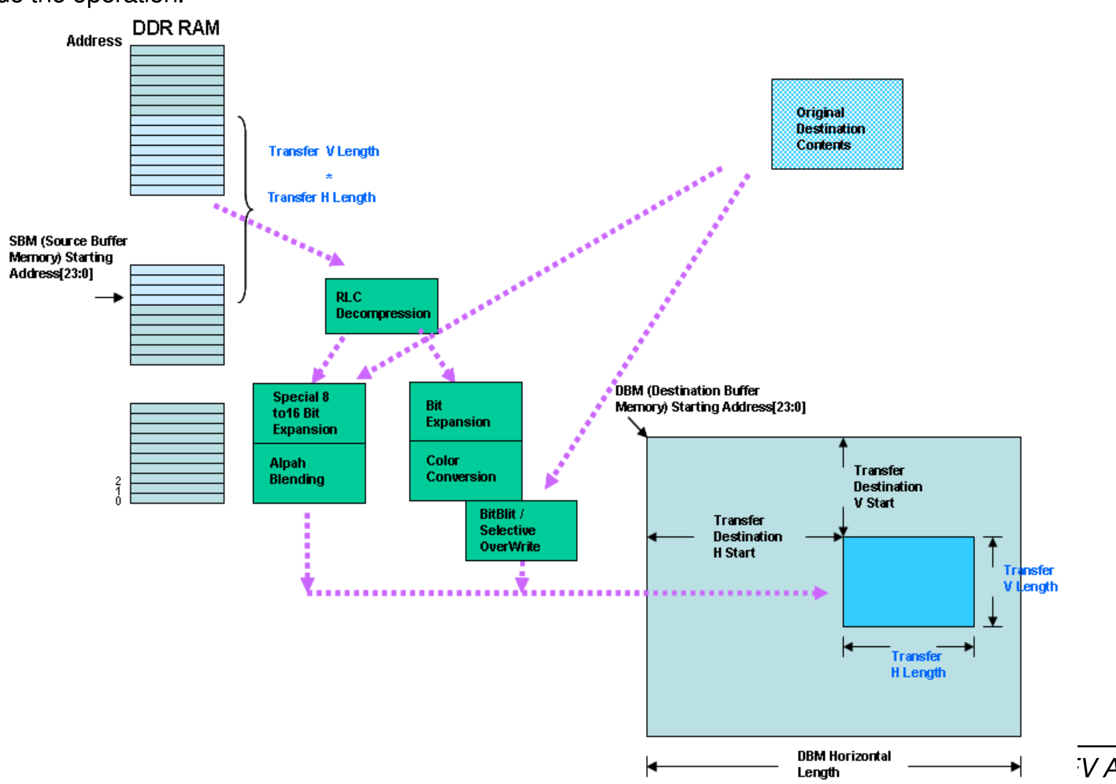
OSG Operation IV – Linear Block Transfer
Linear Block Transfer is similar to Block Transfer except the source is accessed linearly in the memory. On top of those functions available to Block Transfer, Linear Block Transfer can have these additional functional operations: RLC Decompression, Bit Expansion, and Special 8 to 16 Bit Expansion.

To perform the Block Transfer, set the following registers properly.
OSGMODE (0x0700[7:6]) = 11
Source Buffer Memory Starting Address (0x0760 ~ 0x0762)
Destination Buffer Memory Starting Address (0x0770 ~ 0x0772)
Destination Buffer Memory Horizontal Length (0x0773)
Transfer Destination Horizontal Start (0x0774 ~ 0x0775)
Transfer Destination Vertical Start (0x0776 ~ 0x0777)
Transfer Horizontal Length (0x0768 ~ 0x0769)
Transfer Vertical Length (0x076A ~ 0x076B)
MSKSEL (0x0700[5:4])
COLOR_CON (0x0700[3])
BPP (0x0700[2])
BEXPM (0x0700[1:0])
RLC Function Enable (0x0704[0])

If any one of the functions, Color Conversion, Selective OverWrite, BitBlt, Bit Expansion, Special 8-To-16 Bit Expansion, RLC Decompression, is selected, the additional register corresponding that function needs to be set properly.

Linear Block Transfer

To start the Linear Block Transfer operation, write “1” to
OP_START (0x0701[0]).
Check the
OSG_STUS (0x0701[7]).
If it becomes “0”, write “0” to
OP_START (0x0701[0])
to conclude the operation.



Color Conversion

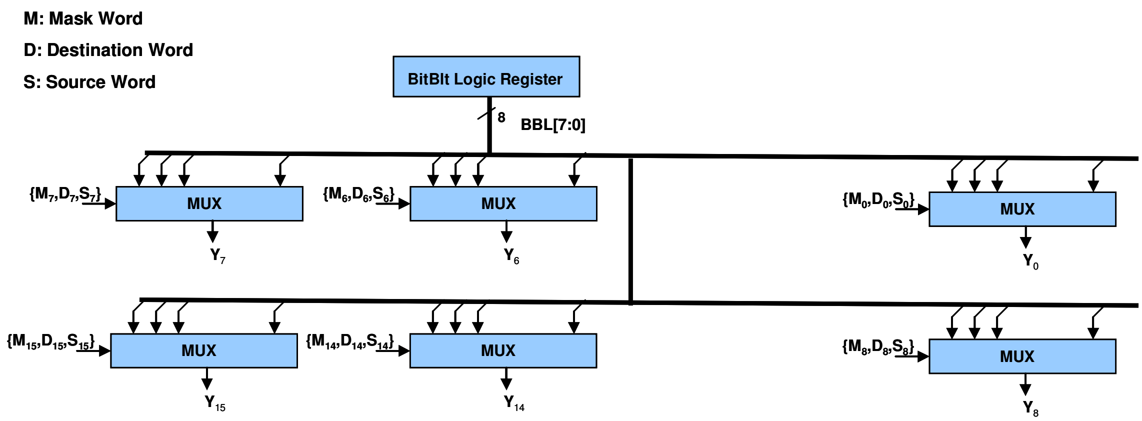
Related registers:
COLOR_CON (0x0700[3])
Color Conversion Source Color (0x0740 ~ 0x0747)
Color Conversion Target Color (0x0748 ~ 0x074F)

Function:
Each source data is compared against the four **Color Conversion Source Color** registers (0x0740 ~0x0747). If the source data matches one of the four colors defined, the content of the corresponding **Color Conversion Target Color** register (0x0748 ~ 0x074F) replaces the source data for further processing.

BitBlt Logic

Related Registers:
MSKSEL (0x0700[5:4])
BitBlt Logic (0x070B)
BitBlt Mask (0x070C ~ 0x070D)
Selective Overwrite (0x0750 ~ 0x0757)

Function:
BitBlt logic is a bit wise operation. For a given bit position, the bits from each of mask data, destination data, and source data forms a triplet with the mask data bit as the msb and source data bit as the lsb, {Mi, Di, Si}. The triplet together with the BitBlt Logic register content forms a truth table. Each bit of BitBlt Logic is bonded with one of the eight combinations of the triplet: BBL[0] ~ {000}, BBL[1] ~ {001}, … BBL[7] ~ {111}. The content of the BitBlt Logic register specifies the outcome of the bit wise combination logic operation of mask data, destination data, and source data. By changing the content of the BitBlt Logic register, various logic operations can be achieved.
The mask data is selectable by **MSKSEL**. **BitBlt Mask** register is one of the choices.



M_i	D_i	S_i	Y_i
0	0	0	BBL[0]
0	0	1	BBL[1]
0	1	0	BBL[2]
0	1	1	BBL[3]
1	0	0	BBL[4]
1	0	1	BBL[5]
1	1	0	BBL[6]
1	1	1	BBL[7]

M_i	D_i	S_i	Y_i
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Default BBL Content

Selective OverWrite

Related Registers:
MSKSEL (0x0700[5:4]) = 00
BitBlt Logic (0x070B) = 1100_1010
Selective OverWrite (0x0750 ~ 0x0757)

Function:
Selective Overwrite is a special case of the BitBlt logic operations. Destination data to be overwritten or kept unchanged are programmed in the Selective OverWrite registers. The MSKSEL must be set to "00". With the default content of the BitBlt Logic register (11001010), the destination data is kept unchanged if it matches one of the four Selective OverWrite registers. If unmatched, the destination data is overwritten by the source data.
If the BitBlt Logic is programmed with (10101100), the outcome becomes: the matched data is overwritten while the unmatched is kept..

Bit Expansion

Related Registers:
BPP (0x0700[2])
BEXPM (0x0700[1:0])
8 Bit Color Expansion Table (0x0710 ~ 0x071F)
16 Bit Color Expansion Table (0x0720 ~ 0x073F)

Function:
Bit expansion is used to expand source data of one/two/four bits to eight or sixteen bit data. The BPP determines the data after expansion is 8-bit or 16-bit. There are 16 entries for each table. The following shows the relationship between the incoming bits and the corresponding entries.

One bit	Table Entry #
0	0
1	1

Two Bit	Table Entry #
00	0
01	1
10	2
11	3

Four Bit	Table Entry #
0000	0
0001	1
0010	2
…	.
1111	15

Special 8 To 16 Bit Expansion

Related Registers:
BPP (0x0700[2]) = 0
BEXPM (0x0700[1:0]) = 11
SP8TO16 (0x0703[4]) = 1
OSG16FORM (0x0703[3:1])
16 Bit Color Expansion Table (0x0720 ~ 0x073F)

Function:
This special bit expansion is used to alpha blend the destination data. The source 8-bit data is not a pixel data but an alpha blending value. The source pixel data used to blend with the destination pixel is always taken from the first entry (Entry #0) of the **16 Bit Color Expansion Table**.
Using the 8-bit source data as the alpha blending parameter, the destination data is fetched and alpha blended with the first entry of the **16 Bit Color Expansion Table**. The resultant data is then written back to the destination.

Microcontroller Interface

The TW8823 registers are accessed via 2-wire serial bus interface as well as parallel host interface. It operates as a slave device.

Two Wire Serial Bus Interface

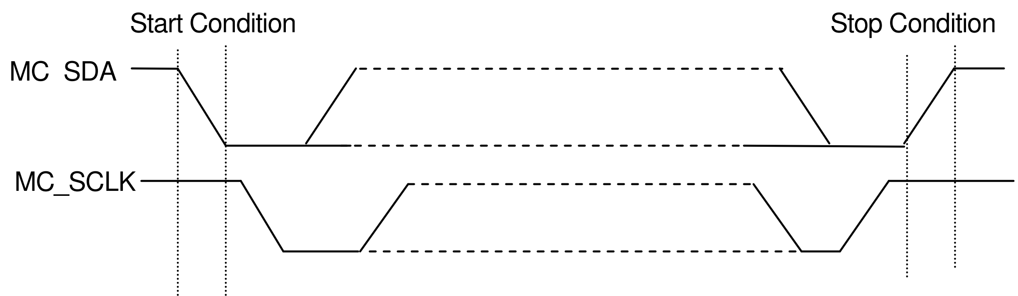


Figure 1. Definition of the serial bus interface bus start and stop

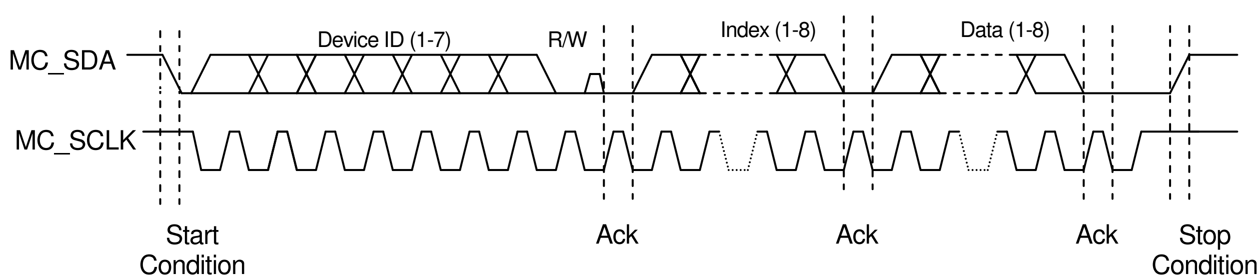


Figure 2. One complete register Write sequence via the serial bus interface

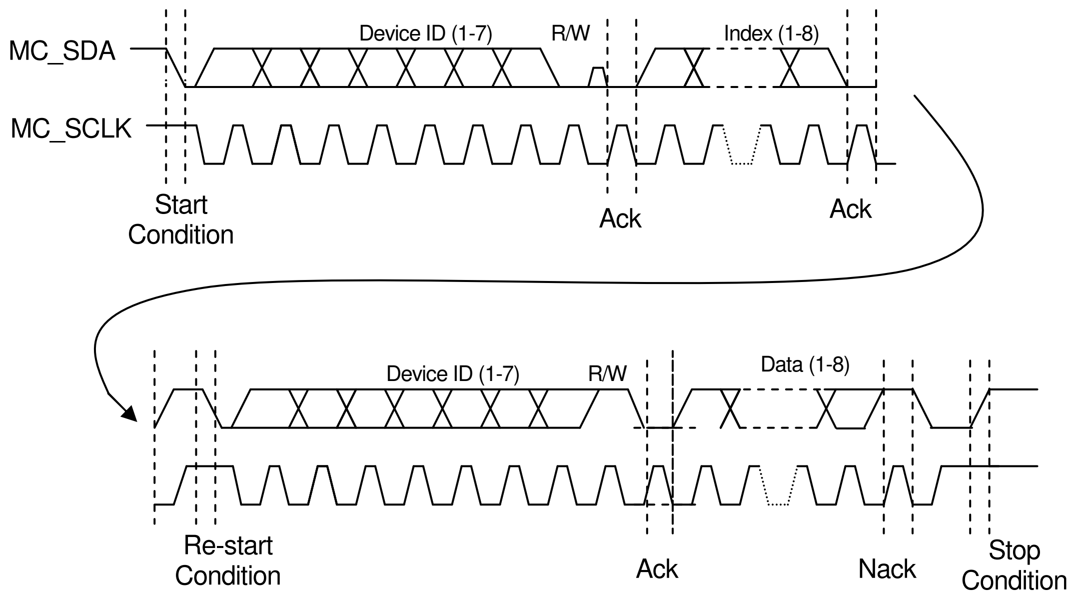


Figure 3. One complete register Read sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW8823 registers. MC_SCLK is the serial clock and MC_SDA is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling MC_SCLK and MC_SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of the MC_SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever MC_SCLK is high.

The TW8823 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the ADDRSEL (Serial Interface Address) pin ether to VDD or GND (See Table 2.). If the ADDRSEL pin is tied to VDD, then the least significant bit of the 7-bit address is a “1”. If the ADDRSEL pin is tied to GND then the least significant bit of the 7-bit address is a “0”. The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives MC_SDA from high to low, while MC_SCLK is high, this is defined to be a start condition (See Figure 1.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 2. (For the TW8823, the next byte is normally the index to the TW8823 registers and is a write to the TW8823 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the MC_SDA line while holding MC_SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the MC_SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of the TW8823, the master sends another 8-bits of data, the TW8823 loads this to the register pointed by the internal index register. The TW8823 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW8823 if they are in ascending sequential order. After each 8-bit transfer the

TW8823 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW8823 the host will issue a stop condition.

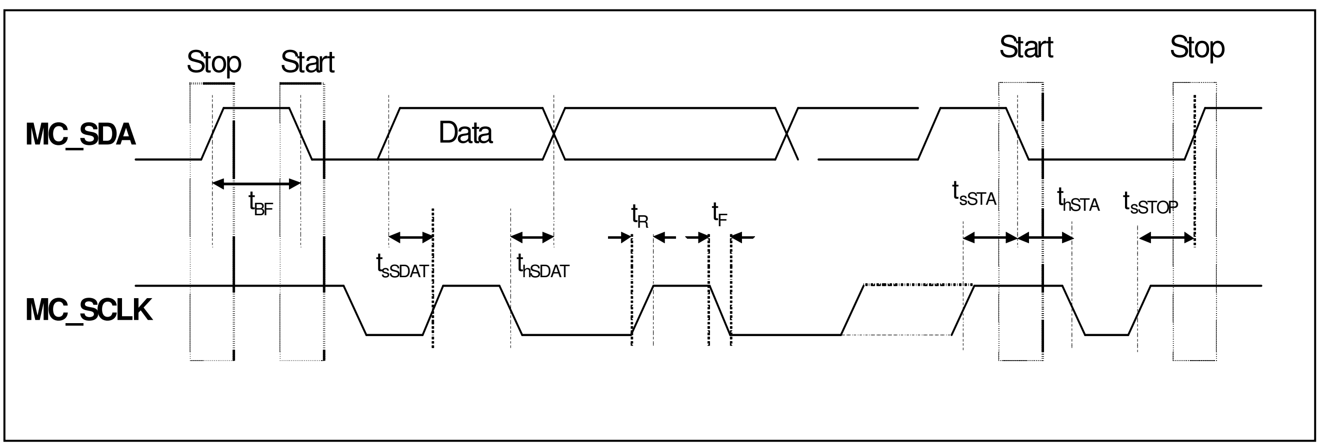
Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	ADDRSEL	0	1=Read 0=Write

Table 2. TW8823 serial bus interface 7-bit slave address and read write bit

A TW8823 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 3). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the MC_SDA line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (MC_SDA is left high during a clock pulse) and issue a stop condition.

Serial Bus Interface Timing Table

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	740	-	-	ns
MC_SDA setup time	t_{sSDAT}	74	-	-	ns
MC_SDA hold time	t_{hSDAT}	50	-	900	ns
Setup time for START condition	t_{sSTA}	370	-	-	ns
Setup time for STOP condition	t_{sSTOP}	370	-	-	ns
Hold time for START condition	t_{hSTA}	74	-	-	ns
Rise time for MC_SCLK and MC_SDA	t_R	-	-	300	ns

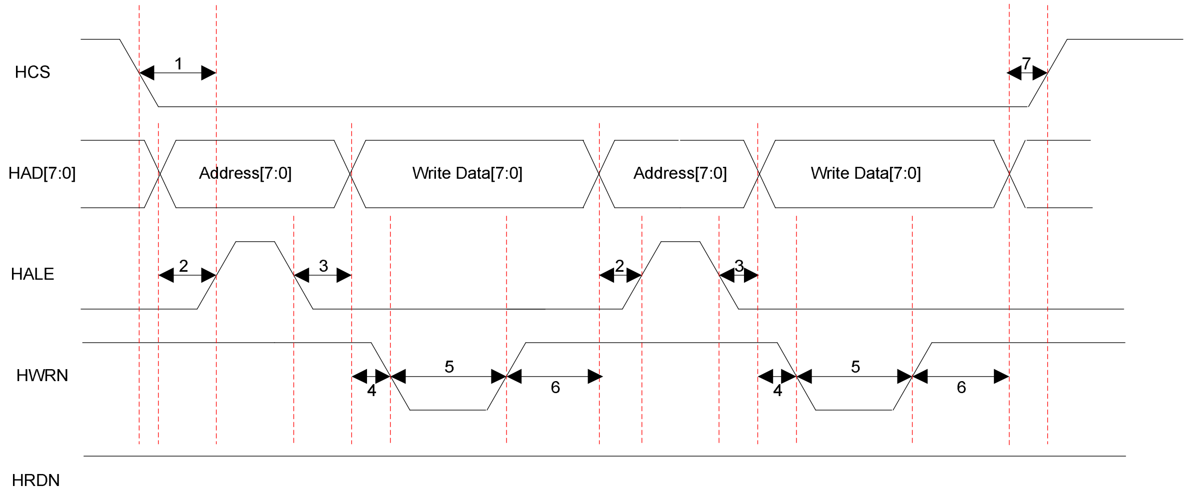


Serial Bus Interface Timing

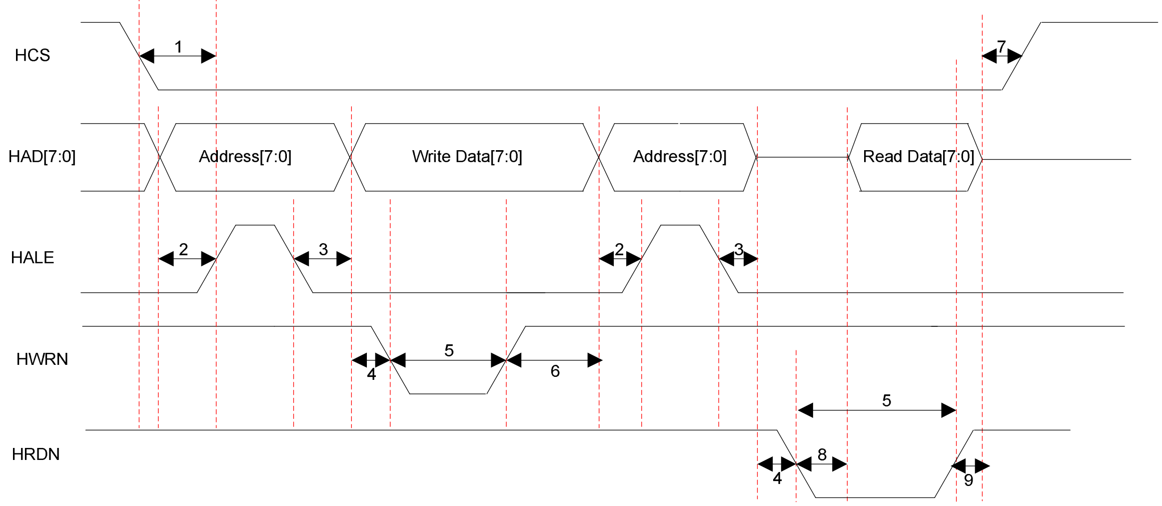
Parallel Host Interface for 8bit Micro Processor

1) HOST = 0

< Write-Write Operation >

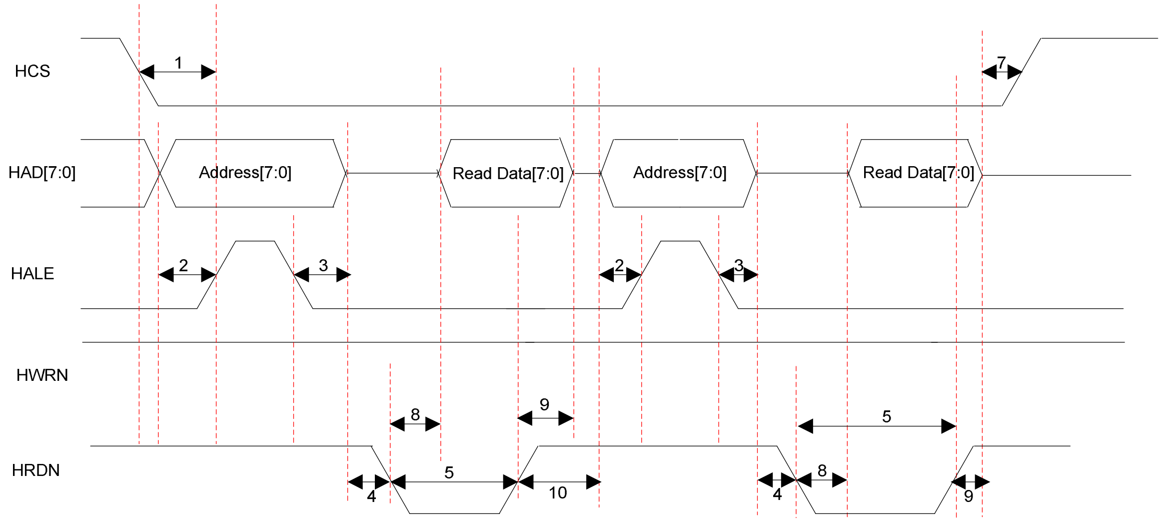


< Write-Read Operation >

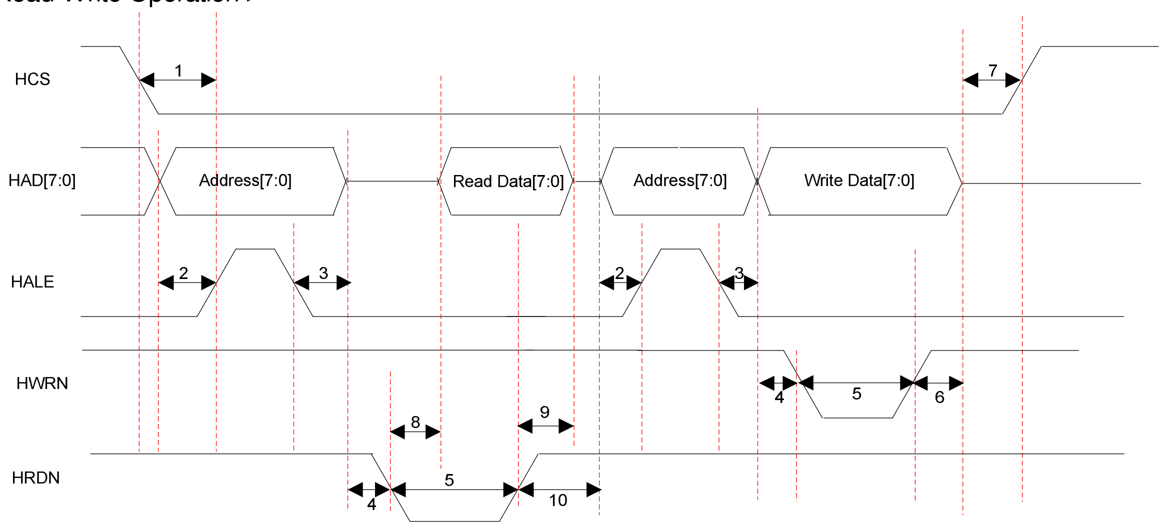


	MIN	MAX	Unit
1	1	*	ns
2	1	*	ns
3	3	*	ns
4	1	*	ns
5	2.0	*	Register Clock Cycle
6	3	*	ns
7	0	*	ns
8	0.5	1.5	Register Clock Cycle
9	0	10	ns

< Read-Read Operation >



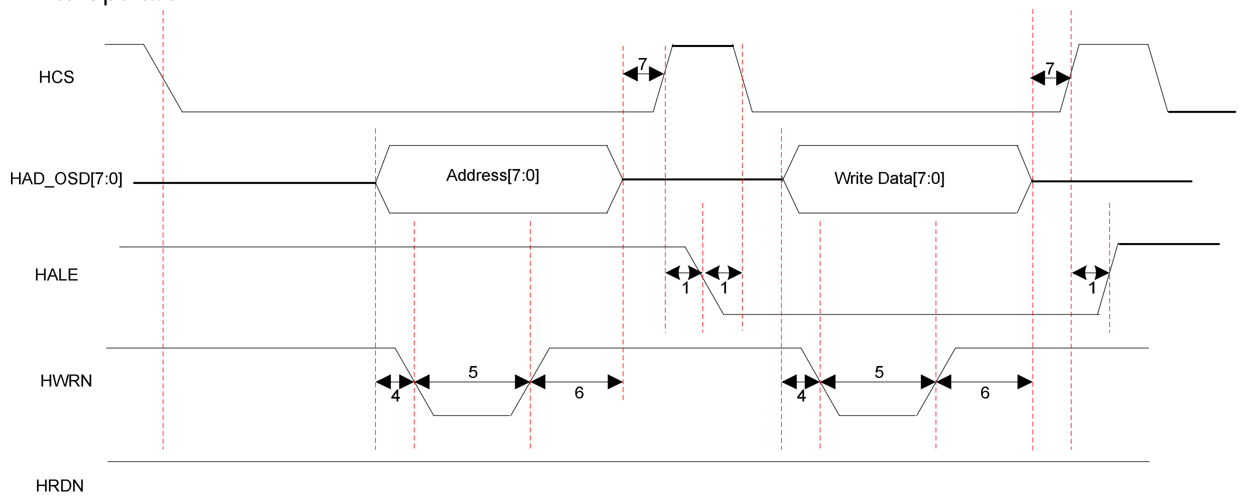
< Read-Write Operation >



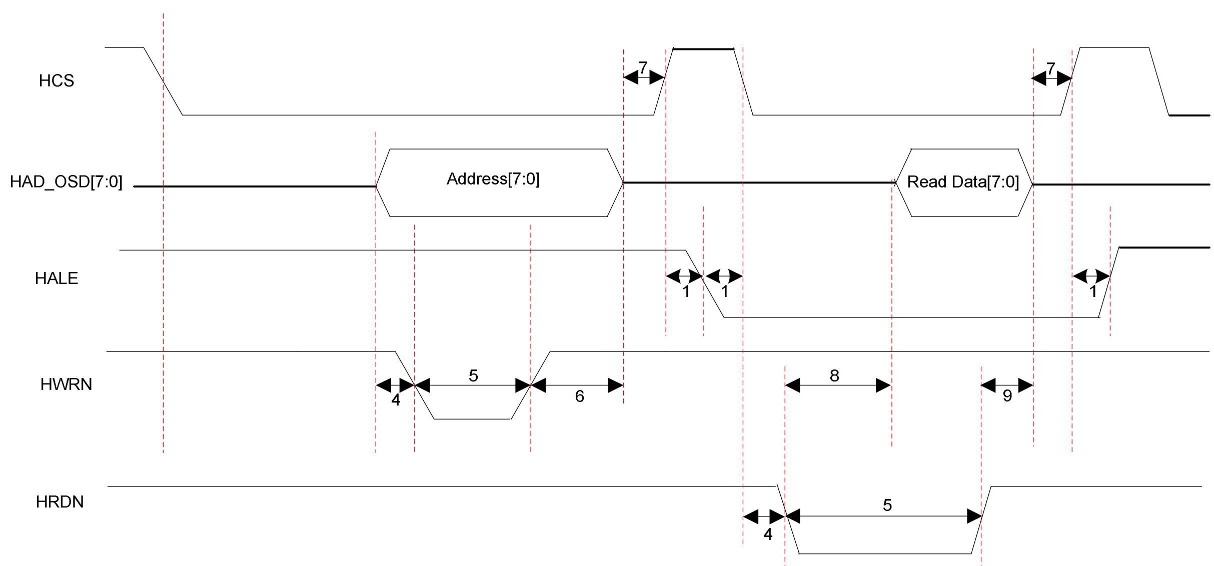
	MIN	MAX	Unit
1	1	*	ns
2	1	*	ns
3	3	*	ns
4	1	*	ns
5	2.0	*	Register Clock Cycle
6	3	*	ns
7	0	*	ns
8	0.5	1.5	Register Clock Cycle
9	0	10	ns
10	10	*	ns

2) HOST = 1

< Write Operation >



< Read Operation >



	MIN	MAX	Unit
1	1	*	ns
2	*	*	*
3	*	*	*
4	1	*	ns
5	2.0	*	Register Clock Cycle
6	3	*	ns
7	0	*	ns
8	0.5	1.5	Register Clock Cycle
9	0	10	ns

Parallel Host Interface for 8bit Micro Processor

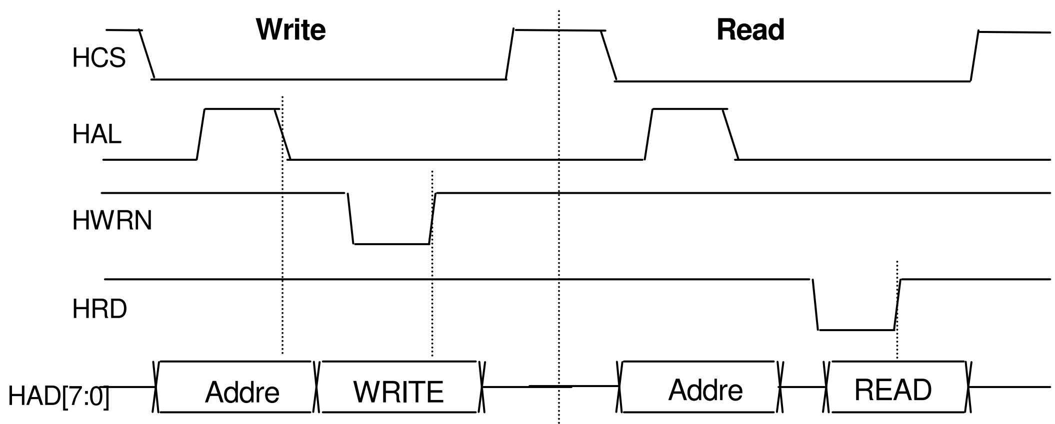


Figure 4. Parallel Interface mode1 Timing Diagram. (HOST = 0)

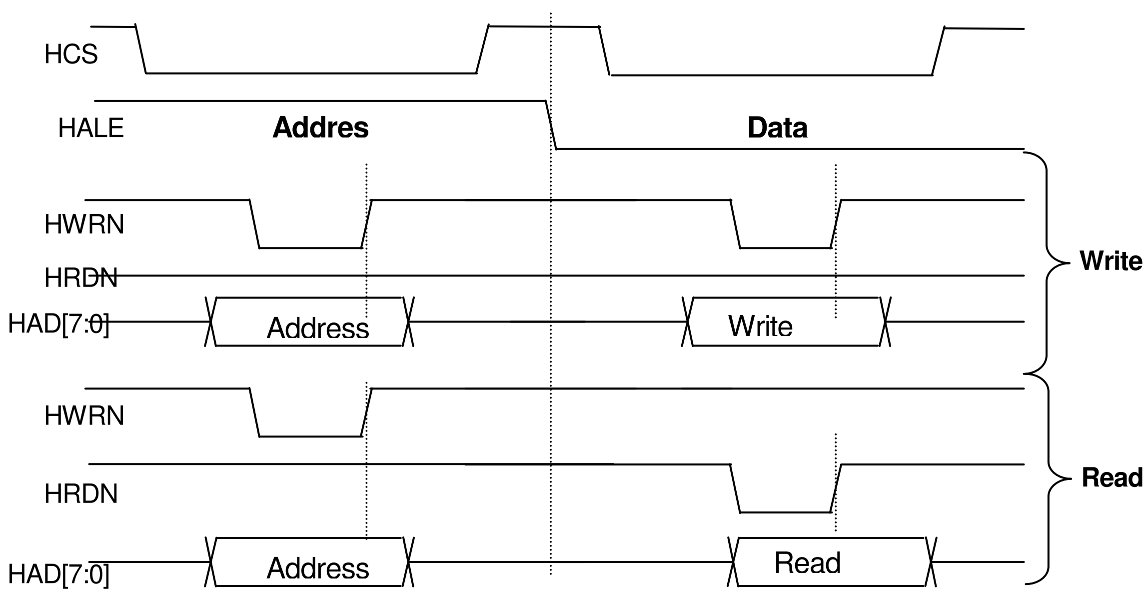


Figure 5. Parallel Interface mode2 Timing Diagram. (HOST =1)

Built-in Microcontroller

TW8823 has built-in 8052 microcontroller which core cache memory to enhance CPU performance. The features of TW8823 MCU are:

- Built-in 8052 MCU up to 72MHz clock speed
- Single/Dual/Quad IO SPI Flash and SPI Flash
- Support SPI DMA Read/Write.
- 1K bytes code cache and 3K byte xdata memery
- Support 2 UARTs up to 115200bps
- System programming through UART(Internal Boot ROM)
- Built-in 3 timer and 2 BaudRate generator
- Power Save Mode with internal 32KHz
- Support IR receiver and IRQ output
- GPIO – Most of digital pins can be configured to GPIO

Power Management

The TW8823 supports panel power sequencing. Typical TFT panels require different parts of the panel power to be applied in the right sequence to avoid premature damage to the panel. Pins are provided to control the panel backlight generator, digital circuitry and panel driver, separately. The TW8823 controls the power up and power down sequence for the LCD panels through firmware control. This gives flexibility to meet different panel requirements.

Gamma Correction

TW8823 has built-in independent RGB 10-bit Gamma RAM for the purpose of table lookup Gamma correction.

Memory configuration

TW8823 has embedded DDR SDRAM controller. It accepts 3 different memory configurations as noted in Table 6. TW8823 operates with SDRAM of 16bits data-bus. Register DDR size (0x0C0B[2:0]) need to be set properly according to the arrangement of external SDRAM.

For NTSC, 3D-comb and 3D-NR concurrent operation is available with at least one 16Mbit SDRAM.

For PAL, 3D-NR is available with one 16Mbit SDRAM but 3D-comb cannot be used. By using two 16Mbit SDRAM for PAL, either 3D-comb or 3D-NR is available. With 64Mbit or bigger SDRAM, 3D-comb and 3D-NR concurrent operation is available for PAL.

Table 3. Available 3D-Comb and 3D-NR operation for each memory configuration

BCONFIG	Config.	Available operation for NTSC	Available operation for PAL
0	64Mb x 1	3D-comb & 3D-NR concurrent operation	3D-comb & 3D-NR concurrent operation
1	128Mb x 2	3D-comb & 3D-NR concurrent operation	3D-comb & 3D-NR concurrent operation
2	256Mb x 1 and up	3D-comb & 3D-NR concurrent operation	3D-comb & 3D-NR concurrent operation

You also need to consider SDRAM space for PIP and OSD.

Memory Map

When 3D Comb is enabled, 3D Comb memory start address is fixed to 000000h, and when 3D Noise reduction is enabled, it will be allocated after 3D Comb.

Size: 3D Comb - NTSC: 1.25MB, PAL:4MB
3D Noise Reduction - NTSC: 640KB, PAL:768KB

Bitmap OSD memory start address = OSD Window0 memory start address (0x0789:0x078A:0x078B) * 4 Byte (unit).
Bitmap OSD memory size = depend on the bitmap data size.
Virtual Horizontal memory width is programmable.

PIP memory start address = PIP Base Address (0x060E:0x060F:0x0610) * 4 Byte (unit)
PIP memory size = window write width (0x0611[2:0], 0x0612) * window write height (0x0613[1:0], 0x0614) * 2Byte * 2 Frame.

PIP2 memory start address = PIP2 Base Address (0x063E:0x063F:0x0640) * 4 Byte(unit)
PIP2 memory size = window write width (0x0641[2:0], 0x0642) * window write height (0x0643[1:0], 0x0644).

Memory Interface

TW8823 supports external SDRAM for various functions including bit-mapped OSD, 3D comb, 3D noise reduction and PIP that require memory buffer. The memory controller of the TW8823 supports 16bit data width up to 155 MHz clock rate.

When power is up, it is reset by the internal reset signal and wait for the initial memory- timing period. To configuration of the SDRAM internal register memory controller performs initial cycle. After all initial cycles performed, memory controller does the normal operation. The memory controller performs arbitration, access timing generation and refresh and configuration.

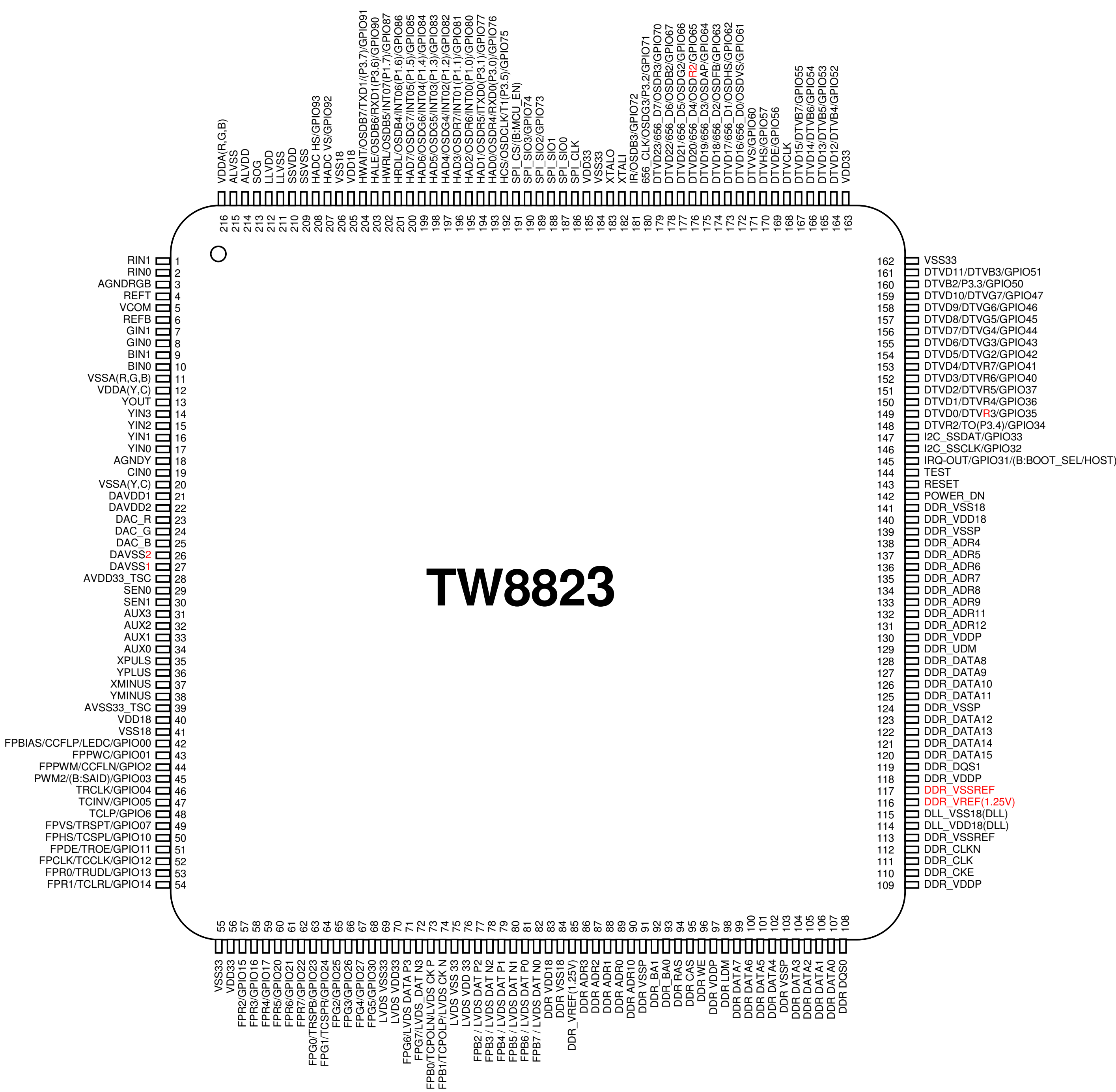
Test Modes

The TEST1 input pin provides test mode selection. If this pin is low at the rising edge of the RESET# pin and remains low, the TW8823 is in its normal operating mode. Table 3 shows the other test modes made available with this pin.

Table 4 Test modes

Test mode	TEST1 Before RESET# rising edge	TEST1 After RESET# rising edge	Description
Normal	0	0	Normal operation
Output tri-state	0	1	In this mode, all pin output drivers are tri-stated. Pin leakage current parameters can be measured.
Outputs high	1	0	In this mode, all pin output drivers are forced to the high output state. V_{OH} and I_{OH} can be measured.
Outputs low	1	1	In this mode, all pin output drivers are forced to the low output state. V_{OL} and I_{OL} can be measured.

Pin Diagram


TW8823
1 RIN1
2 RIN0
3 AGNDRGB
4 REFT
5 VCOM
6 REFB
7 GIN1
8 GIN0
9 BIN1
10 BIN0
11 VSSA(R,G,B)
12 VDDA(Y,C)
13 YOUT
14 YIN3
15 YIN2
16 YIN1
17 YIN0
18 AGNDY
19 CIN0
20 VSSA(Y,C)
21 DAVDD1
22 DAVDD2
23 DAC_R
24 DAC_G
25 DAC_B
26 DAVSS2
27 DAVSS1
28 AVDD33_TSC
29 SEN0
30 SEN1
31 AUX3
32 AUX2
33 AUX1
34 AUX0
35 XPULS
36 YPLUS
37 XMINUS
38 YMINUS
39 AVSS33_TSC
40 VDD18
41 VSS18
42 FPBIAS/CCFLP/LEDC/GPIO00
43 FPPWC/GPIO01
44 FPPWM/CCFLN/GPIO2
45 PWM2/(B:SAID)/GPIO03
46 TRCLK/GPIO04
47 TCINV/GPIO05
48 TCLP/GPIO6
49 FPVS/TRSPT/GPIO07
50 FPHS/TCSPL/GPIO10
51 FPDE/TROE/GPIO11
52 FPCLK/TCCLK/GPIO12
53 FPR0/TRUDL/GPIO13
54 FPR1/TCLRL/GPIO14
55 VSS33
56 VDD33
57 FPR2/GPIO15
58 FPR3/GPIO16
59 FPR4/GPIO17
60 FPR5/GPIO20
61 FPR6/GPIO21
62 FPR7/GPIO22
63 FPG0/TRSPB/GPIO23
64 FPG1/TCSPR/GPIO24
65 FPG2/GPIO25
66 FPG3/GPIO26
67 FPG4/GPIO27
68 FPG5/GPIO30
69 LVDS VSS33
70 LVDS VDD33
71 FPG6/LVDS DATA P3
72 FPG7/LVDS_DAT N3
73 FPB0/TCPOLN/LVDS CK P
74 FPB1/TCPOLP/LVDS CK N
75 LVDS VSS 33
76 LVDS VDD 33
77 FPB2 / LVDS DAT P2
78 FPB3 / LVDS DAT N2
79 FPB4 / LVDS DAT P1
80 FPB5 / LVDS DAT N1
81 FPB6 / LVDS DAT P0
82 FPB7 / LVDS DAT N0
83 DDR VDD18
84 DDR VSS18
85 DDR_VREF(1.25V)
86 DDR ADR3
87 DDR ADR2
88 DDR ADR1
89 DDR ADR0
90 DDR ADR10
91 DDR VSSP
92 DDR_BA1
93 DDR_BA0
94 DDR RAS
95 DDR CAS
96 DDR WE
97 DDR VDDP
98 DDR LDM
99 DDR DATA7
100 DDR DATA6
101 DDR DATA5
102 DDR DATA4
103 DDR VSSP
104 DDR DATA3
105 DDR DATA2
106 DDR DATA1
107 DDR DATA0
108 DDR DQS0
109 DDR_VDDP
110 DDR_CKE
111 DDR_CLK
112 DDR_CLKN
113 DDR_VSSREF
114 DLL_VDD18(DLL)
115 DLL_VSS18(DLL)
116 DDR_VREF(1.25V)
117 DDR_VSSREF
118 DDR_VDDP
119 DDR_DQS1
120 DDR_DATA15
121 DDR_DATA14
122 DDR_DATA13
123 DDR_DATA12
124 DDR_VSSP
125 DDR_DATA11
126 DDR_DATA10
127 DDR_DATA9
128 DDR_DATA8
129 DDR_UDM
130 DDR_VDDP
131 DDR_ADR12
132 DDR_ADR11
133 DDR_ADR9
134 DDR_ADR8
135 DDR_ADR7
136 DDR_ADR6
137 DDR_ADR5
138 DDR_ADR4
139 DDR_VSSP
140 DDR_VDD18
141 DDR_VSS18
142 POWER_DN
143 RESET
144 TEST
145 IRQ-OUT/GPIO31/(B:BOOT_SEL/HOST)
146 I2C_SSCLK/GPIO32
147 I2C_SSDAT/GPIO33
148 DTVR2/TO(P3.4)/GPIO34
149 DTVD0/DTVR3/GPIO35
150 DTVD1/DTVR4/GPIO36
151 DTVD2/DTVR5/GPIO37
152 DTVD3/DTVR6/GPIO40
153 DTVD4/DTVR7/GPIO41
154 DTVD5/DTVG2/GPIO42
155 DTVD6/DTVG3/GPIO43
156 DTVD7/DTVG4/GPIO44
157 DTVD8/DTVG5/GPIO45
158 DTVD9/DTVG6/GPIO46
159 DTVD10/DTVG7/GPIO47
160 DTVB2/P3.3/GPIO50
161 DTVD11/DTVB3/GPIO51
162 VSS33
163 VDD33
164 DTVD12/DTVB4/GPIO52
165 DTVD13/DTVB5/GPIO53
166 DTVD14/DTVB6/GPIO54
167 DTVD15/DTVB7/GPIO55
168 DTVCLK
169 DTVDE/GPIO56
170 DTVHS/GPIO57
171 DTVVS/GPIO60
172 DTVD16/656_D0/OSDVS/GPIO61
173 DTVD17/656_D1/OSDHS/GPIO62
174 DTVD18/656_D2/OSDFB/GPIO63
175 DTVD19/656_D3/OSDAP/GPIO64
176 DTVD20/656_D4/OSDR2/GPIO65
177 DTVD21/656_D5/OSDG2/GPIO66
178 DTVD22/656_D6/OSDB2/GPIO67
179 DTVD23/656_D7/OSDR3/GPIO70
180 656_CLK/OSDG3/P3.2/GPIO71
181 IR/OSDB3/GPIO72
182 XTALI
183 XTALO
184 VSS33
185 VDD33
186 SPI_CLK
187 SPI_SIO0
188 SPI_SIO1
189 SPI_SIO2/GPIO73
190 SPI_SIO3/GPIO74
191 SPI_CS/(B:MCU_EN)
192 HCS/OSDCLK/T1(P3.5)/GPIO75
193 HAD0/OSDR4/RXD0(P3.0)/GPIO76
194 HAD1/OSDR5/ITXD0(P3.1)/GPIO77
195 HAD2/OSDR6/INT00(P1.0)/GPIO80
196 HAD3/OSDR7/INT01(P1.1)/GPIO81
197 HAD4/OSDG4/INT02(P1.2)/GPIO82
198 HAD5/OSDG5/INT03(P1.3)/GPIO83
199 HAD6/OSDG6/INT04(P1.4)/GPIO84
200 HAD7/OSDG7/INT05(P1.5)/GPIO85
201 HRDL/OSDB4/INT06(P1.6)/GPIO86
202 HWRL/OSDB5/INT07(P1.7)/GPIO87
203 HALE/OSDB6/RXD1(P3.6)/GPIO90
204 HWAIT/OSDB7/TXD1/(P3.7)/GPIO91
205 VDD18
206 VSS18
207 HADC VS/GPIO92
208 HADC HS/GPIO93
209 SSVSS
210 SSVDD
211 LLVSS
212 LLVDD
213 SOG
214 ALVDD
215 ALVSS
216 VDDA(R,G,B)

Pin Description

This section provides a detailed description of each pin for the TW8823. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

The pin description also includes the buffer direction and type used for that pin.

PIN#	I/O	Pin Name	Description	Internal Connection	Recommended Connection of Unused Pin	Status at HW Reset
Analog I/F signals and Power						
1	AI	RIN1	Analog Red input 1		Connect to VSSA	
2	AI	RIN0	Analog Red input 0			
3	AI	AGNDRGB	Analog RGB input reference node			
4	AI	REFT	RGB A/D Voltage Reference Top. Connect a 0.1uF between VSSA and this pin.			
5	A	VCOM	Analog output for Mid Scale Voltage			X
6	AI	REFB	RGB A/D Voltage Reference Bottom. Connect a 0.1uF between VSSA and this pin.			
7	AI	GIN1	Analog Green input 1			
8	AI	GIN0	Analog Green input 0			
9	AI	BIN1	Analog Blue input 1			
10	AI	BIN0	Analog Blue input 0			
13	AO	YOUT	Y output (Y out or Y+C out)		Open/Unconnected	X
14	AI	YIN3	Analog composite or luma input 3		Connect to VSSA	
15	AI	YIN2	Analog composite or luma input 2			
16	AI	YIN1	Analog composite or luma input 1			
17	AI	YIN0	Analog composite or luma input 0			X
18	AI	AGNDY	Analog YC input reference node			
19	AI	CIN0	Analog component C input 0			
213	AI	SOG	Sync On Green input			
216	P	VDDA(RGB)	Analog A/D Power +1.8V			
11	P	VSSA(RGB)	Analog Ground for R, G, B channels. Connect a 0.1uF between VSSA and this pin.			
12	P	VDDA(YC)	Analog Video A/D Power +1.8V			
20	P	VSSA(YC)	Analog Video A/D Ground		-	Pwr
209	P	SSVSS	SS-PLL(Internal Analog) Ground			
210	P	SSVDD	SS-PLL(Internal Analog) Power +1.8V			
211	P	LLVSS	LL- PLL(Internal Analog) Ground			
212	P	LLVDD	LL- PLL (Internal Analog) Power +1.8V			
214	P	ALVDD	Low Voltage Analog Power +1.8V			

215	P	ALVSS	Analog Ground for low voltage analog power (ALVDD)			
DAC I/F Signals						
21	P	DAVDD1	DAC Analog Power +5.0V		-	Pwr
22	P	DAVDD2	DAC Analog Power +3.3V			
23	AO	DAC_R	DAC Analog Red data output		Open/Unconnected	X
24	AO	DAC_G	DAC Analog Green data output			
25	AO	DAC_B	DAC Analog Blue data output			
26	P	DAVSS2	DAC Analog Ground		-	Pwr
27	P	DAVSS1	DAC Analog Ground for 5V power			
29	AI	SEN0	Analog Sensing 0 input / CCFL or LED current sensing			
30	AI	SEN1	Analog Sensing 1 input / CCFL or LED voltage sensing			
31	AI	AUX3	Auxiliary channel 3			
32	AI	AUX2	Auxiliary channel 2			
33	AI	AUX1	Auxiliary channel 1			
34	AI	AUX0	Auxiliary channel 0			
35	AI	XPLUS	Positive X input			
36	AI	YPLUS	Positive Y input			
37	AI	XMINUS	Negative X input			
38	AI	YMINUS	Negative Y input			
28	P	AVDD33_TSC	Analog Power +3.3V		-	Pwr
39	P	AVSS33_TSC	Analog Ground			
DDR						
86	O	DDR_ADR3	DDR Address			
87	O	DDR_ADR2	DDR Address			
88	O	DDR_ADR1	DDR Address			
89	O	DDR_ADR0	DDR Address			
90	O	DDR_ADR10	DDR Address			
138	O	DDR_ADR4	DDR Address			
137	O	DDR_ADR5	DDR Address			
136	O	DDR_ADR6	DDR Address			
135	O	DDR_ADR7	DDR Address			
134	O	DDR_ADR8	DDR Address			
133	O	DDR_ADR9	DDR Address			
132	O	DDR_ADR11	DDR Address			
131	O	DDR_ADR12	DDR Address			
92	O	DDR_BA1	DDR Bank 1			
93	O	DDR_BA0	DDR Bank 0			
94	O	DDR_RAS	DDR RAS Signal			
95	O	DDR_CAS	DDR CAS Signal			
96	O	DDR_WE	DDR WE Signal			
98	O	DDR_LDM	DDR Data Mask			
99	O	DDR_DATA7	DDR Data Bus			
100	O	DDR_DATA6	DDR Data Bus			
101	O	DDR_DATA5	DDR Data Bus			
102	O	DDR_DATA4	DDR Data Bus			

104	O	DDR_DATA3	DDR Data Bus			
105	O	DDR_DATA2	DDR Data Bus			
106	O	DDR_DATA1	DDR Data Bus			
107	O	DDR_DATA0	DDR Data Bus			
128	O	DDR_DATA8	DDR Data Bus			
127	O	DDR_DATA9	DDR Data Bus			
126	O	DDR_DATA10	DDR Data Bus			
125	O	DDR_DATA11	DDR Data Bus			
123	O	DDR_DATA12	DDR Data Bus			
122	O	DDR_DATA13	DDR Data Bus			
121	O	DDR_DATA14	DDR Data Bus			
120	O	DDR_DATA15	DDR Data Bus			
108		DDR_DQS0	DDR DQS 0			
110		DDR_CKE	DDR Clock Enable Signal			
111	O	DDR_CLK	DDR Positive Clock Output Signal			
112	O	DDR_CLKN	DDR Negative Clock Output Signal			
119		DDR_DQS1	DDR DQS 1			
129	O	DDR_UDM	DDR Data Mask			
83, 140	P	DDR_VDD18	DDR Core Power +1.8V		-	Pwr
84, 141	P	DDR_VSS18	DDR Core Ground			
85, 116	P	DDR_VREF (1.25V)	DDR 1.25V Reference Voltage			
113, 117	P	DDR_VSSREF	DDR Ground for VREF(1.25V) shielding			
97, 109, 118, 130	P	DDR_VDDP	DDR IO Power +2.5V			
91, 103, 124, 139	P	DDR_VSSP	DDR IO Ground			
114	P	DLL_VDD18	DLL Power +1.8V			
115	P	DLL_VSS18	DLL Ground			
LCD Panel I/F, TCON I/F and LVDS Signals						
42	O	FPBIAS	Power on/off control for panel backlight bias	Pull down		0
	O	CCFLP	CCFLDriver Polarity (Positive)			
	O	LEDC	MCU LED			
	I/O	GPIO00	GPIO 00			
43	O	FPPWC	Power on/off control for flat panel display	Pull down		
	I/O	GPIO01	GPIO 01			
44	O	FPPWM	PWM control for panel backlight	Pull down		
	O	CCFLN	CCFL Driver Polarity (Negative)			
	I/O	GPIO02	GPIO 02			
45	O	PWM2	PWM control2	---		
	O	(B:SAID)	B:SAID			
	I/O	GPIO03	GPIO 03			
46	O	TRCLK	TCON - Row Driver Shift Clock	---		
	I/O	GPIO04	GPIO 04			

47	O	TCINV	TCON - Column Driver Inversion	---		
	I/O	GPIO05	GPIO 05			
48	O	TCLP	TCON - Column Driver Load Pulse	---		
	I/O	GPIO06	GPIO 06			
49	O	FPVS	Flat Panel VSYNC	---		
	O	TRSPT	TCON - Row Driver Starting Pulse (Top Start)			
	I/O	GPIO07	GPIO 07			
50	O	FPHS	Flat Panel HSYNC	---		
	O	TCSPL	TCON - Column Driver Start Pulse (Left to right scan)			
	I/O	GPIO10	GPIO 10			
51	O	FPDE	Flat Panel Data Enable	---		
	O	TROE	TCON - Row Driver Output Enable			
	I/O	GPIO11	GPIO 11			
52	O	FPCLK	Flat Panel Clock Output	---		
	O	TCCLK	Column Driver Clock			
	I/O	GPIO12	GPIO 12			
53	O	FPR0	Red Flat Panel Output bit	---		
	O	TRUDL	TCON-Up down selection (Up : high, Down : low)			
	I/O	GPIO13	GPIO 13			
54	O	FPR1	Red Flat Panel Output bit	---		
	O	TCLRL	TCON -Left Right selection (Left : high, Right : low)			
	I/O	GPIO14	GPIO 14			
57	O	FPR2	Red Flat Panel Output bit	---		
	I/O	GPIO15	GPIO 15			
58	O	FPR3	Red Flat Panel Output bit	---		
	I/O	GPIO16	GPIO 16			
59	O	FPR4	Red Flat Panel Output bit	---		
	I/O	GPIO17	GPIO 17			
60	O	FPR5	Red Flat Panel Output bit	---		
	I/O	GPIO20	GPIO 20			
61	O	FPR6	Red Flat Panel Output bit	---		
	I/O	GPIO21	GPIO 21			
62	O	FPR7	Red Flat Panel Output bit	---		
	I/O	GPIO22	GPIO 22			
63	O	FPG0	Green Flat Panel Output bit	---		
	O	TRSPB	TCON - Row Driver Starting Pulse (Bottom Start)			
	I/O	GPIO23	GPIO 23			
64	O	FPG1	Green Flat Panel Output bit	---		
	O	TCSPR	TCON - Column Driver Start Pulse (Right to left scan)			
	I/O	GPIO24	GPIO 24			
65	O	FPG2	Green Flat Panel Outputs bit	---		
	I/O	GPIO25	GPIO 25			
66	O	FPG3	Green Flat Panel Output bit	---		
	I/O	GPIO26	GPIO 26			
67	O	FPG4	Green Flat Panel Output bit	---		

	I/O	GPIO27	GPIO 27			
68	O	FPG5	Green Flat Panel Output bit	---		
	I/O	GPIO30	GPIO 30			
71	O	FPG6	Green Flat Panel Output bit	---		
	O	LVDS_DAT_P3	Positive differential LVDS 3rd data output			
72	O	FPG7	Green Flat Panel Output bit	---		
	O	LVDS_DAT_N3	Negative differential LVDS 3rd data output			
73	O	FPB0	Blue Flat Panel Output bit	---		
	O	TCPOLN	TCON – Column Driver Polarity (Negative)			
	O	LVDS_CK_P	Positive differential LVDS clock output			
74	O	FPB1	Blue Flat Panel Output bit	---		
	O	TCPOLP	TCON – Column Driver Polarity (Positive)			
	O	LVDS_CK_N	Negative differential LVDS clock output			
77	O	FPB2	Blue Flat Panel Output bit	---		
	O	LVDS_DAT_P2	Positive differential LVDS 2nd data output			
78	O	FPB3	Blue Flat Panel Output bit	---		
	O	LVDS_DAT_N2	Negative differential LVDS 2nd data output			
79	O	FPB4	Blue Flat Panel Output bit	---		
	O	LVDS_DAT_P1	Positive differential LVDS 1st data output			
80	O	FPB5	Blue Flat Panel Output bit	---		
	O	LVDS_DAT_N1	Negative differential LVDS 1st data output			
81	O	FPB6	Blue Flat Panel Output bit	---		
	O	LVDS_DAT_P0	Positive differential LVDS 0th data output			
82	O	FPB7	Blue Flat Panel Output bit	---		
	O	LVDS_DAT_N0	Negative differential LVDS 0th data output			
HOST, External OSD, DTV I/F signals						
148	I	DTVR2	DTV input	Pull down		
	I/O	TO(P3.4)	MCU Port 3.4			
	I/O	GPIO34	GPIO 34			
149	I	DTV0	DTV Input	Pull down		
	I	DTVR3	DTV Input			
	I/O	GPIO35	GPIO 35			
150	I	DTVD1	DTV Input	Pull down		
	I	DTVR4	DTV Input			
	I/O	GPIO36	GPIO 36			
151	I	DTVD2	DTV Input	Pull down		
	I	DTVR5	DTV Input			
	I/O	GPIO37	GPIO 37			
152	I	DTVD3	DTV Input	Pull down		
	I	DTVR6	DTV Input			
	I/O	GPIO40	GPIO 40			
153	I	DTVD4	DTV Input	Pull down		
	I	DTVR7	DTV Input			
	I/O	GPIO41	GPIO 41			
154	I	DTVD5	DTV Input	Pull down		
	I	DTVG2	DTV Input			
	I/O	GPIO42	GPIO 42			

155	I	DTVD6	DTV Input	Pull down		
	I	DTVG3	DTV Input			
	I/O	GPIO43	GPIO 43			
156	I	DTVD7	DTV Input	Pull down		
	I	DTVG4	DTV Input			
	I/O	GPIO44	GPIO 44			
157	I	DTVD8	DTV Input	Pull down		
	I	DTVG5	DTV Input			
	I/O	GPIO45	GPIO 45			
158	I	DTVD9	DTV Input	Pull down		
	I	DTVG6	DTV Input			
	I/O	GPIO46	GPIO 46			
159	I	DTVD10	DTV Input	Pull down		
	I	DTVG7	DTV Input			
	I/O	GPIO47	GPIO 47			
160	I	DTVB2	DTV Input	Pull down		
	I/O	P3.3	MCU Port 3.3			
	I/O	GPIO50	GPIO 50			
161	I	DTVD11	DTV Input	Pull down		
	I	DTVB3	DTV Input			
	I/O	GPIO51	GPIO 51			
164	I	DTVD12	DTV Input	Pull down		
	I	DTVB4	DTV Input			
	I/O	GPIO52	GPIO 52			
165	I	DTVD13	DTV Input	Pull down		
	I	DTVB5	DTV Input			
	I/O	GPIO53	GPIO 53			
166	I	DTVD14	DTV Input	Pull down		
	I	DTVB6	DTV Input			
	I/O	GPIO54	GPIO 54			
167	I	DTVD15	DTV input	Pull down		
	I	DTVB7	DTV Input			
	I/O	GPIO55	GPIO 55			
168	I	DTVCLK	Clock input for DTV interface	---		
169	I	DTVDE	Data valid for DTV interface or raw HSYNC for DTV interface	Pull down		
	I/O	GPIO56	GPIO 56			
170	I	DTVHS	Horizontal sync for DTV interface	Pull down		
	I/O	GPIO57	GPIO 57			
171	I	DTVVS	Data valid for DTV interface or raw HSYNC for DTV interface	Pull down		
	I/O	GPIO60	GPIO 60			
172	I	DTV16	DTV Input	Pull down		
	I	656_D0	2nd DTV Input, 656 Data 0			
	I	OSDVS	External OSD Vertical Sync Signal			
	I/O	GPIO61	GPIO 61			
173	I	DTV17	DTV Input	Pull down		

	I	656_D1	2nd DTV Input, 656 Data 1			
	I	OSDHS	External OSD Horizontal Sync Signal			
	I/O	GPIO62	GPIO 62			
174	I	DTV18	DTV Input	Pull down		
	I	656_D2	2nd DTV Input, 656 Data 2			
	I/O	OSDFB	External OSD			
	I/O	GPIO63	GPIO 63			
175	I	DTV19	DTV Input	Pull down		
	I	656_D3	2nd DTV Input, 656 Data 3			
	I	OSDAP	External OSD Alpha Blending Control Signal			
	I/O	GPIO64	GPIO 64			
176	I	DTV20	DTV Input	Pull down		
	I	656_D4	2nd DTV Input, 656 Data 4			
	I	OSDR2	External OSD R Data Input			
	I/O	GPIO65	GPIO 65			
177	I	DTV21	DTV Input	Pull down		
	I	656_D5	2nd DTV Input, 656 Data 5			
	I	OSDG2	External OSD G Data Input			
	I/O	GPIO66	GPIO 66			
178	I	DTV22	DTV Input	Pull down		
	I	656_D6	2nd DTV Input, 656 Data 6			
	I	OSDB2	External OSD B Data Input			
	I/O	GPIO67	GPIO 67			
179	I	DTV23	DTV Input	Pull down		
	I	656_D7	2nd DTV Input, 656 Data 7			
	I	OSDR3	External OSD R Data Input			
	I/O	GPIO70	GPIO 70			
180	I	656_CLK	656 Clock Signal	Pull down		
	I	OSDG3	External OSD G Data Input			
	I/O	P3.2	MCU Port 3.2			
	I/O	GPIO71	GPIO 71			
181	I	IR	IR	Pull up		
	I	OSDB3	External OSD B Data Input			
	I/O	GPIO72	GPIO 72			
186	I/O	SPI_CLK	SPI Clock Output	---		
187	I/O	SPI_SIO0	SPI IO 0	----		
188	I/O	SPI_SIO1	SPI IO 1	----		
189	I/O	SPI_SIO2	SPI IO 2	Pull up		
	I/O	GPIO73	GPIO 73			
190	I/O	SPI_SIO3	SPI IO 3	Pull up		
	I/O	GPIO74	GPIO 74			
191	I	SPI_CS	SPI CS	---		
	I	B:MCU_EN	MCU Eable			
192	I	HCS	Host Interface Chip Select Signal	Pull up		
	I	OSDCLK	External OSD Clock Input			
	I/O	T1(P3.5)	MCU Port 3.5			

	I/O	GPIO75	GPIO 75			
193	I	HAD0	Host Interface address data	Pull up		
	I	OSDR4	External OSD R Data Input			
	I/O	RXD0(P3.0)	MCU Port 3.0 (MCU RXD)			
	I/O	GPIO76	GPIO 76			
194	I	HAD1	Host Interface address data	Pull up		
	I	OSDR5	External OSD R Data Input			
	I	TXD0(P3.1)	MCU Port 3.1 (MCU TXD)			
	I/O	GPIO77	GPIO 77			
195	I	HAD2	Host Interface address data	Pull up		
	I	OSDR6	External OSD R Data Input			
	I	INT00(P1.0)	MCU Port 1.0			
	I/O	GPIO80	GPIO 80			
196	I	HAD3	Host Interface address data	Pull up		
	I	OSDR7	External OSD R Data Input			
	I/O	INT01(P1.1)	MCU Port 1.1			
	I/O	GPIO81	GPIO 81			
197	I	HAD4	Host Interface address data	Pull up		
	I	OSDG4	External OSD G Data Input			
	I/O	INT02(P1.2)	MCU Port 1.2			
	I/O	GPIO82	GPIO 82			
198	I	HAD5	Host Interface address data	Pull up		
	I	OSDG5	External OSD G Data Input			
	I/O	INT03(P1.3)	MCU Port 1.3			
	I/O	GPIO83	GPIO 83			
199	I	HAD6	Host Interface address data	Pull up		
	I	OSDG6	External OSD G Data Input			
	I/O	INT04(P1.4)	MCU Port 1.4			
	I/O	GPIO84	GPIO 84			
200	I	HAD7	Host Interface address data	Pull up		
	I	OSDG7	External OSD G Data Input			
	I/O	INT05(P1.5)	MCU Port 1.5			
	I/O	GPIO85	GPIO 85			
201	I	HRDL	Host Interface read indicate signal	Pull up		
	I	OSDB4	External OSD B Data Input			
	I/O	INT06(P1.6)	MCU Port 1.6			
	I/O	GPIO86	GPIO 86			
202	I	HWRL	Host Interface write indicate signal	Pull up		
	I	OSDB5	External OSD B Data Input			
	I/O	INT07(P1.7)	MCU Port 1.7			
	I/O	GPIO87	GPIO 87			
203	I	HALE	Host Interface address latch enable signal	Pull up		
	I	OSDB6	External OSD B Data Input			
	I/O	RXD1(P3.6)	MCU Port 3.6, RXD1			
	I/O	GPIO90	GPIO 90			
204	I	HWAIT	Host Interface Wait Signal	Pull up		

	I	OSDB7	External OSD B Data Input			
	I/O	TXD1(P3.7)	MCU Port 3.7, TXD1			
	I/O	GPIO91	GPIO 91			
207		HADC_VS	RGB VSYNC	Pull up		
	I/O	GPIO92	GPIO 92			
208		HADC_HS	RGB HSYNC	Pull up		
	I/O	GPIO93	GPIO 93			
Other I/F signals						
182	I	XTALI	Crystal terminal (if crystal is used) or Oscillator input		-	Hi-Z
183	O	XTALO	Crystal terminal (if crystal is used)			0
147	I/O	I2C_SSDAT	I2C Data	Pull up		Hi-Z
	I/O	GPIO33	GPIO 33			
146	I	I2C_SSCLK	I2C Clock	Pull up		
	I/O	GPIO32	GPIO 32			
145	O	IRQ-OUT	IRQ Output Data	---		
	I/O	GPIO31	GPIO 31			
	I	B:BOOT_SEL / HOST	Boot Select for MCU mode Parallel Host Type for Non Mcu Mode			
142	I	POWER_DN	Power down control	---		
144	I	TEST	Chip test mode selection. Connect VSS	---	-	Hi-Z
143	I	RESET	Reset Pin	Pull up		1

Digital Power						
70, 76	P	LVDS_VDD33	LVDS Power +3.3V		-	PWR
69, 75	P	LVDS_VSS33	LVDS Ground			
56, 163, 185	P	VDD33	Digital I/O Power +3.3V			
55, 162, 184	P	VSS33	Digital I/O Ground			
40, 205	P	VDD18	Digital Core Power +1.8V			
41, 206	P	VSS18	Digital Core Ground			

*1: Pull-up Resistor 38K(min), 54K(typ), 83K(max) ohm

*2: Pull-down Resistor 35K(min), 57K(typ), 107K(max) ohm

*3: " - " Need opimized treatment

Parametric Information

AC/DC Electrical Parameters

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
V_{DDA33} *(measured to V_{SSA33} *) 3.3V	VDDA33M	-	-	3.6	V
V_{DDA18}* (measured to V_{SSA18}*) 1.8V	VDDAM	-	-	1.92	V
V_{DD18}*(measured to V_{SS18}*) 1.8V	VDD18M	-	-	1.98	V
V_{DDL33} (measured to V_{SSL33}) 3.3V	VDDL33M	-	-	3.6	V
V_{DD33} (measured to V_{SS33}) 3.3V	VDD33M	-	-	3.6	V
V_{DD25}*(measured to V_{SS25}*) 2.5V (DDR)	VDD25M	-	-	2.7	V
V_{DDREF}*(measured to V_{SSREF}*) 1.25V	VDDREFM	-	-	1.35V	
Voltage on any digital signal pin (See the note below)	-	V_{SS33} – 0.5	-	5.5	V
Analog Input Voltage (supplied by 1.8V)	-	V_{SSA18} – 0.5	-	1.92	V
Analog Input Voltage (suppied by 3.3V)	-	V_{SSA33} - 0.5		3.6	V
Storage Temperature	T S	–65	-	+150	°C
Junction Temperature	T J	-	-	+125	°C
Reflow Soldering	Tpeak	255 +5/-0 (10~30 seconds)			°C

Note * :
V_{DDA33} : DAVDD1, DAVDD2, AVDD33_TSC
V_{SSA33} : DAVSS1, DAVSS2, AVSS33_TSC
V_{DDA18}: VDDA, DLL_VDD18, SSVDD, LLVDD, ALVDD
V_{SSA18}: VSSA, DLL_VSS18, SSVSS, LLVSS, ALVSS
V_{DDL33}: LVDS_VDD33
V_{SSL33} : LVDS_VSS33
V_{DD33}: VDD33
V_{SS33}VSS33
V_{DD25}: DDR_VDDP
V_{SS25}: DDR_VSSP
V_{DD18}: VDD18, DDR_VDD18
V_{SS18}: VSS18, DDR_VSS18
V_{DDREF}: DDR_VREF
V_{SSREF}: DDR_VSSREF

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 4 can induce destructive latch-up.

Table 6. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO 3.3V	V_{DD33}	3.15	3.3	3.6	V
Power Supply IO 2.5V (DDR)	V_{DD25}	2.3	2.5	2.7	V
Power Supply — Digital Core 1.8V	V_{DD18}	1.62	1.8	1.98	V
Reference Voltage Supply 1.25V	V_{DDREF}	1.15	1.25	1.35	V
Power Supply — LVDS 3.3V	V_{DDL33}	3.15	3.3	3.6	V
Power Supply — Analog 3.3V	V_{DDA33}	3.15	3.3	3.6	V
Power Supply — Analog 1.8V	V_{DDA18}	1.62	1.8	1.92	V
Ambient Operating Temperature	T_A	-40		+85	°C
Analog Supply current 3.3V	Iaa33	-	TBD	-	mA
Analog Supply current 1.8V (CVBS)	Iaa18	-	TBD	-	mA
LVDS Supply current 3.3V*	Iddl33	-	TBD	-	mA
Digital I/O Supply current 3.3V*	Idd33	-	TBD	-	mA
Digital I/O Supply current 2.5V*	Idd25	-	TBD	-	mA
Digital Core Supply Current*	Idd18	-	TBD	-	mA
Digital Reference Supply Current	Idd125	-	TBD	-	mA
* Note : Digital I/O and core power supply current measurement is base on WVGA input (40MHz clock rate) with SMPTE pattern. MCLK is set at 120MHz.					

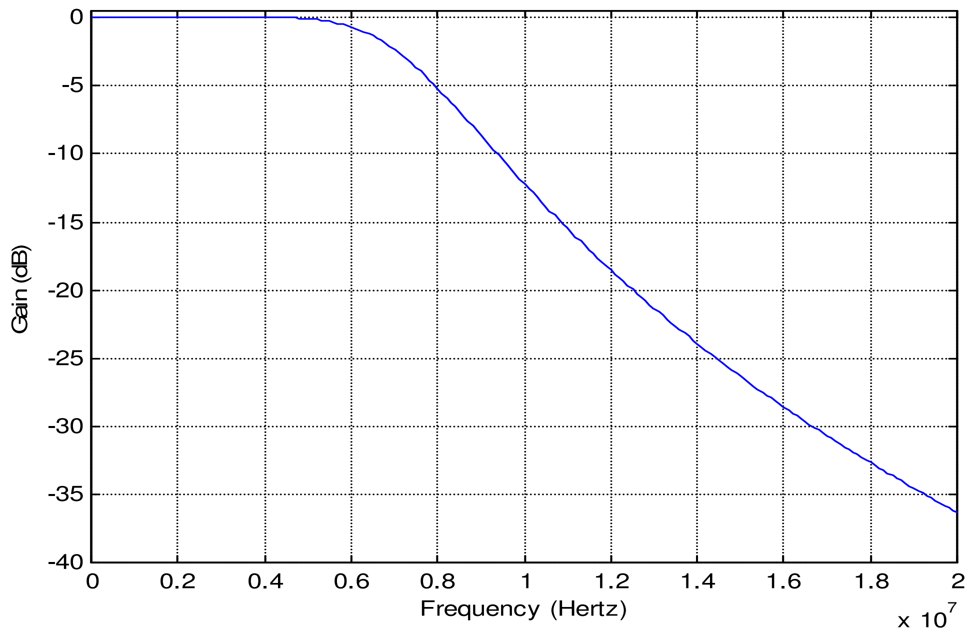
Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD33} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Voltage (DDR)	V_{IH}	V_{DDREF}+ 0.18	-	V_{DD25}+ 0.3	V
Input Low Voltage (DDR)	V_{IL}	-0.3	-	V_{DDREF}- 0.18	V
Input High Current ($V_{IN}=V_{DD}$)	I_{IH}	-	-	10	µA
Input Low Current (V_{IN}=VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	V_{DD33}	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF

Parameter	Symbol	Min	Typ	Max	Units
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
YIN0, YIN1 , YIN2 and YIN3 Input Range (AC coupling required)		0.5	1.0	2.0	Vpp
CIN0 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
RIN0, RIN1 , GIN0, GIN1, BIN0, and BIN1 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
SEN0, SEN1 DC Input Range		0.65	1.65	2.65	V
SOYIN Input Range		0.02	0.3	1.8	V
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	9	-	Bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	27	60	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz

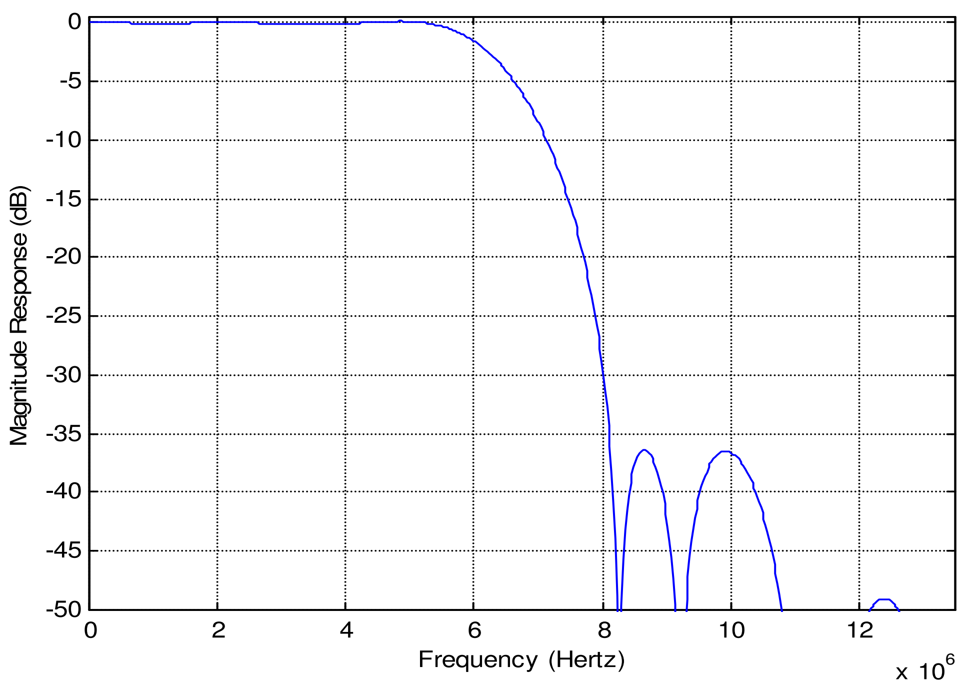
Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
Subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
Deviation		-	-	±50	ppm
Load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
*Note : Crystal Deviation crossover normal operation temperature range					

Filter Curves

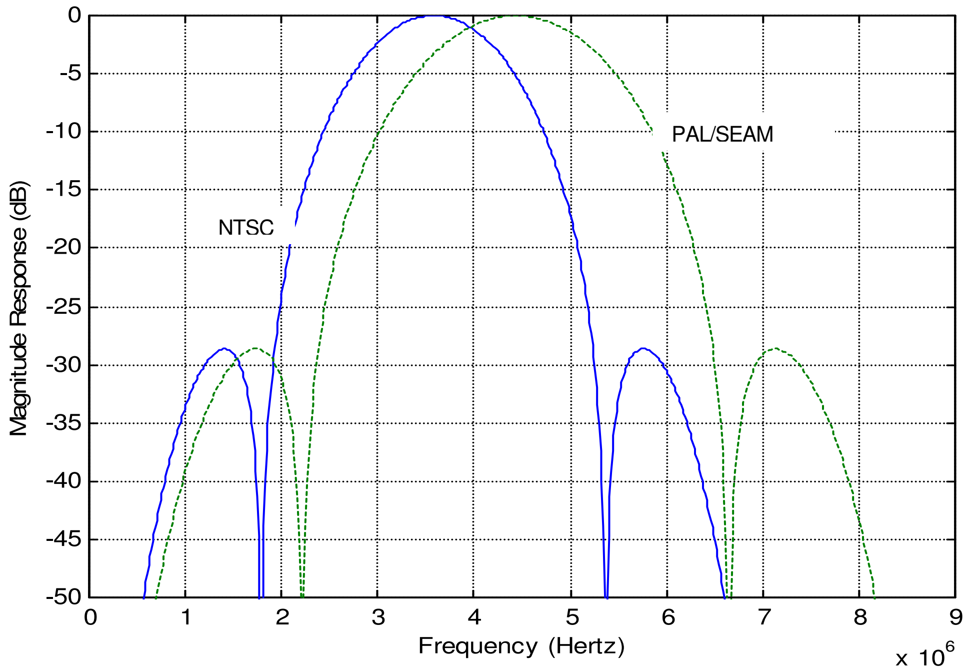
Anti-alias filter



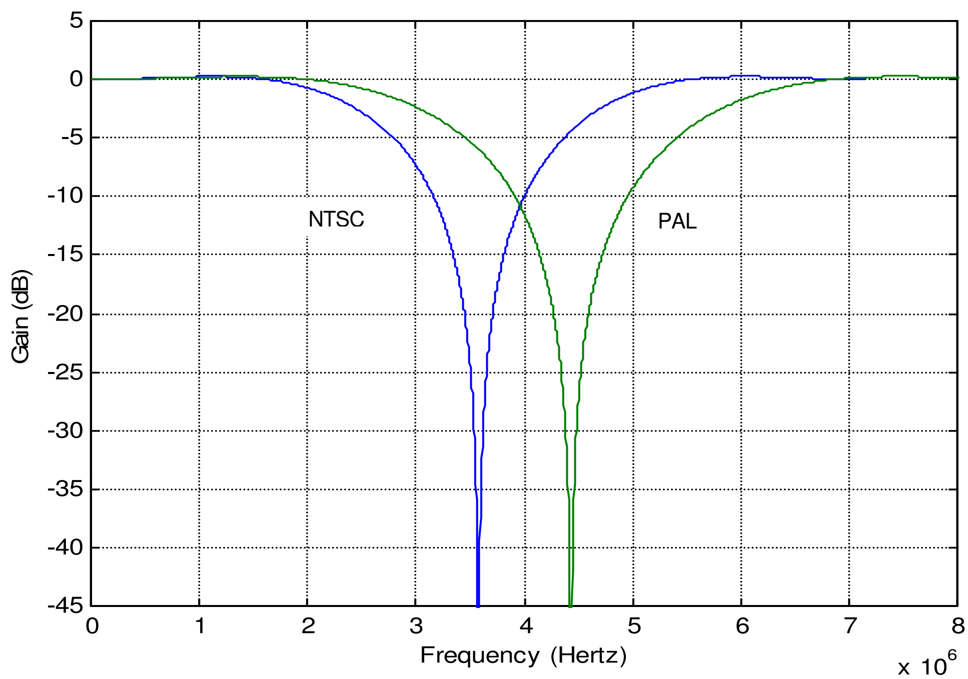
Decimation filter



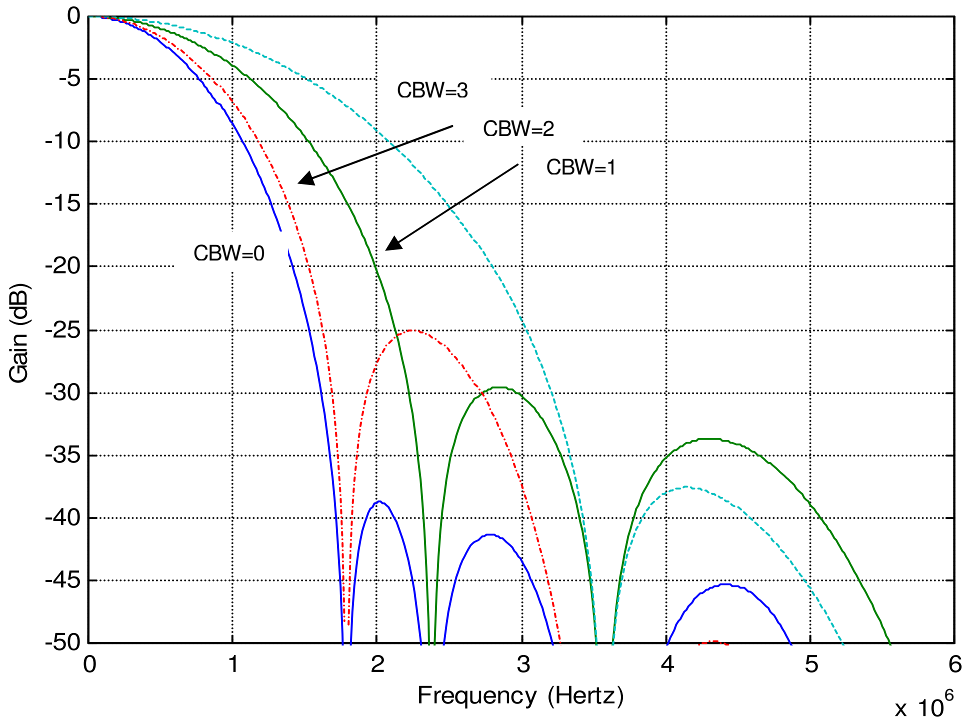
Chroma Band Pass Filter Curves



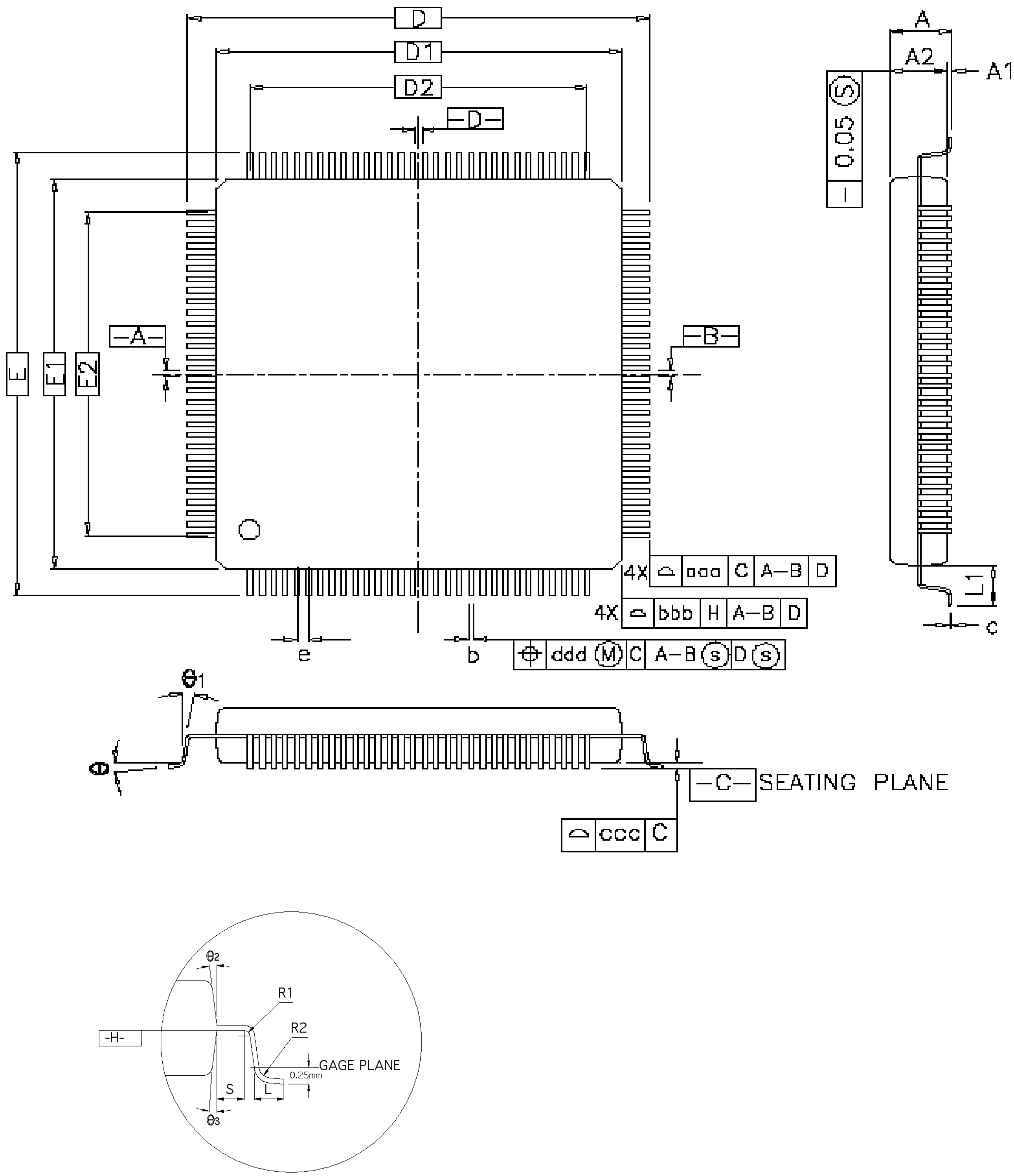
Luma Notch Filter Curve for NTSC and PAL

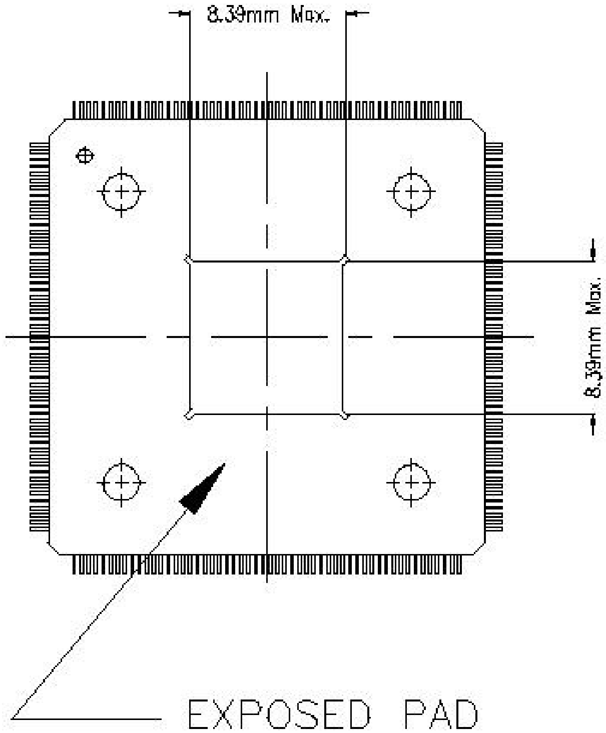


Chrominance Low-Pass Filter Curve



Mechanical Data 216 LQFP





SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	26.00 BSC.			1.024 BSC.		
D1	24.00 BSC.			0.945 BSC.		
E	26.00 BSC.			1.024 BSC.		
E1	24.00 BSC.			0.945 BSC.		
R2	0.08	---	0.20	0.003	---	0.008
R1	0.08	---	---	0.003	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	---	---	0°	---	---
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
C	0.09	---	0.20	0.004	---	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	---	---	0.008	---	---
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	21.20			0.835		
E2	21.20			0.835		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

CONTROL DIMENSIONS ARE IN MILLMETERS.

NOTES:

1. Dimensions D1 and E1 do not include mold protrusion.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.
   Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and a adjacent lead is 0.07mm.

TW8823 Register Summary

The registers are organized in functional groups in this Register Summary. A register containing different functional bits may appear more than once in different functional groups.
If a particular bit of a register is not related to that functional group, it is printed in smaller font than those related. For example, bit 7 of index 006 is classified as "General" and is printed in normal size; the other bits in this register are printed in smaller size for their functionality is not classified as "General".

General (Common for any page)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0x??FF	PAGE[7:0]								00h

TOTAL PAGES : 16 (0~F)

PAGE #	Register Group	PAGE #	Register Group	PAGE #	Register Group	PAGE #	Register Group
0	COMMON	4	SCALER	B	MEASURE	D	CCFL/TSC/ LVDS/ REMO/LOPOR /SSPLL/DAC
1	DECODER	5	IE	C	DDR/DLL/ AUX_DDR		
2	INPIF_RGB	6	PIP	F	MCU		
3	INPIF_DTV1/ INPIF_DTV2	7	OSD				
		8	EOSD				
		9	WAVER,TGA				
		A	TCON				

Global Register

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
000	ID					REV			28h
040	GPIO_EN 0[7:0]								00H
041	GPIO_EN 1[7:0]								00H
042	GPIO_EN 2[7:0]								00H
043	GPIO_EN 3[7:0]								00H
044	GPIO_EN 4[7:0]								00H
045	GPIO_EN 5[7:0]								00H
046	GPIO_EN 6[7:0]								00H
047	GPIO_EN 7[7:0]								00H
048	GPIO_EN 8[7:0]								00H
049	GPIO_EN 9[7:0]								00H
050	GPIO_OE 0[7:0]								00H
051	GPIO_OE 1[7:0]								00H
052	GPIO_OE 2[7:0]								00H
053	GPIO_OE 3[7:0]								00H
054	GPIO_OE 4[7:0]								00H
055	GPIO_OE 5[7:0]								00H
056	GPIO_OE 6[7:0]								00H
057	GPIO_OE 7[7:0]								00H
058	GPIO_OE 8[7:0]								00H
059	GPIO_OE 9[7:0]								00H
060	GPIO_ID 0[7:0]								00H
061	GPIO_ID 1[7:0]								00H
062	GPIO_ID 2[7:0]								00H
063	GPIO_ID 3[7:0]								00H
064	GPIO_ID 4[7:0]								00H
065	GPIO_ID 5[7:0]								00H
066	GPIO_ID 6[7:0]								00H
067	GPIO_ID 7[7:0]								00H
068	GPIO_ID 8[7:0]								00H
069	GPIO_ID 9[7:0]								00H
070	GPIO_OD 0[7:0]								00H
071	GPIO_OD 1[7:0]								00H
072	GPIO_OD 2[7:0]								00H
073	GPIO_OD 3[7:0]								00H
074	GPIO_OD 4[7:0]								00H
075	GPIO_OD 5[7:0]								00H
076	GPIO_OD 6[7:0]								00H
077	GPIO_OD 7[7:0]								00H
078	GPIO_OD 8[7:0]								00H
079	GPIO_OD 9[7:0]								00H
080	-	-	-	-	TESTGPO	TESTGPOSEL[2:0]			00H

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
090	PULLUD_EN_0[7:0]								FFH
091	PULLUD_EN_1[7:0]								FFH
092	PULLUD_EN_2[7:0]								FFH
093	PULLUD_EN_3[7:0]								F3H
094	PULLUD_EN_4[7:0]								FFH
095	PULLUD_EN_5[7:0]								FFH
096	PULLUD_EN_6[7:0]								FFH
097	PULLUD_EN_7[7:0]								FFH
098	PULLUD_EN_8[7:0]								FFH
099	PULLUD_EN_9[7:0]								F3H

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0A0	PWRONRSTN	I2SCS	MCUEN	HOST	BOOTSEL	HCSL	PWRDN	TEST	00H
0A1	DUALDTVMODE[1:0] (←211[7:6])		-	-	-	-	-	SACNT (←0E8[0])	00H
0AA	SELPADCLKP	SELPADCLKM	-	-	-	PCKCAP[1:0]			00H
0AB	CLOCK_POL (←213[7:0])								00H
0AC	MERGE_CN (← 20E[7])	-	-	-	-	-	CKPOL_DEC	MAINPATHCKPOL (←210[0])	00H
0AD	CLKPDALL (←0E8[7])	CLKPWRDN[6:0]							00H

Status & Interrupt

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0B0	LB_OVF	LB_UNF	V_LOS_C	H_LOS_C	VDLOS_C	V_LOSS	H_LOSS	SYNCS	00h
0B1	M_RDY	PWS_C	V_PRD_C	H_PRD_C	LBOUNF	VDC_C	VH_LOS_C	SYNCS_C	00h
0B2	IRQ_B_B17	IRQ_B_B16	IRQ_B_B15	IRQ_B_B14	IRQ_B_B13	IRQ_B_B12	IRQ_B_B11	IRQ_B_B10	FFh
0B3	-	-				IRQ_B_VD	IRQ_B_CC	IRQ_B_50	07h
0B4	-	-	P_VLOS_C	P_VLOS_C	-	P_VLOSS	P_HLOSS	P_SYNCS	00h
0B5	-	-	P_VPRD_C	P_HPRD_C	-	-	P_VHLOS C	P_SYNCS C	00h
0B6	-	-	M_VLOS_C	M_VLOS_C	-	M_VLOSS	M_HLOSS	M_SYNCS	00h
0B7	-	-	M_VPRD_C	M_HPRD_C	-	-	M_VHLOS C	M_SYNCS	00h
0B8	-		IRQ_1B5_5	IRQ_1B5_4	-	-	IRQ_1B5_1	IRQ_1B5_0	00h
0B9			IRQ_1B7_5	IRQ_1B7_4			IRQ_1B7_1	IRQ_1B7_0	00h
0BA	IRQ_OE	IRQ_AL	IRQ_STS	-	-	-	-	-	00h

Internal Test

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0C6	SEL_C	GRAYD	DATA_0	DATABLU	TLMODE		-	-	00h
0C7	BWYMIN								-
0C8	BWYMAX								-
0C9	BWFMIN								-
0CA	BWFMAX								-
0CB	BWBTILT								-
0CC	BWWTILT								-
0CD	-								
0CE	TEST_MODE								00h
0CF	-	-	-	-	-	-		-	00h
0E0	SWRST							LLBFF ?	00h

Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0101	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	-
0102	YSEL2	FC27	IFSEL		YSEL		CSEL	-	40h
0103	-								-
0104	-	CKHY		-					00h
0105	-								-
0106	DECRST	PDMIX	FBP	AGC_EN	CLKPDN	Y_PDN	C_PDN	V_PDN	03h
0107	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02h
0108	VDELAY_LO								15h
0109	VACTIVE_LO								-
010A	HDELAY_LO								-
010B	HACTIVE_LO								D0h
010C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	8Ch
010D	-	-	-	-					15h
010E	-	-	-						-
010F	-								-
0110	BRIGHTNESS								00h
0111	CONTRAST								60h
0112	SCURVE	VSF	CTI		SHARPNESS				51h
0113	SAT_U								80h
0114	SAT_V								80h
0115	HUE								00h
0116	-				-				-
0117	SHCOR				-	VSHP			30h
0118	CTCOR		CCOR		VCOR		CIF		44h
0119	-								-
011A	-	EDS_EN	CC_EN	PARITY	FF_OVF	FF_EMP	CC_EDS	LO_HI	
011B	CC_DATA								
011C	DTSTUS	STDNOW			ATREG	STANDARD			00h
011D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	00h
011E	-	CVSTD			CVFMT				08h
011F	-					VREF	IREF	SAVE	00h

Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0120	CLPEND				CLPST				50h
0121	NMGAIN				WPGAIN			AGCGAIN	42h
0122	AGCGAIN								F0h
0123	PEAKWT								D8h
0124	CLMPLD	CLMPL							BCh
0125	SYNCTD	SYNCT							B8h
0126	MISSCNT				HSWIN				44h
0127	PCLAMP								2Ah
0128	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00h
0129	BSHT			VSHT					15h
012A	CKILLMAX		CKILLMIN						A0h
012B	HTL				VTL				44h
012C	CKLM	YDLY			HFLT				30h
012D	HPLC	EVCNT	PALC	SDET	TBC_EN	BYPASS	SYOUT	HADV	14h
012E	HPM		ACCT		SPM		CBVV		A5h
012F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0h
0130	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	-
0131	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	-
0132	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								-
0133	FRM		YNR		CLMP		PSP		05h
0134	Index		NSEN/SSEN/PSEN/WKTH						1Ah
0135	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	10h
0136									00h
0137									00h
0138	-							SY_C	00h

LCDC – 3D Comb/NR Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0160	MD_TH								08h
0161	-								00h
0162	3DEN	MIXMD1	MIXMD2	-	-	TEST3D	TM_3D		00h
0163	-								80h
0164	-								53h
0165	MSTRETCH								4Ch
0166	-								4Bh
0167	TESTNR	NREN	NRGAIN		NRLEVEL				14h
0168	NONSTD	-	-	-	-	NS_LNUM	NS_LLEN	NS_FLEN	07h
0169	NSTH1								02h
016A	NSTH2								03h
016B	NSON				NSOFF				C1h
016C	-								00h
016D	-								98h
016E	-	-	-	-	-	-	-	-	00h
016F	-	-	-	-	-	-	-	-	00h

LCDC – IIRGB (Input Interface RGB)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0200	-	-	-	-	-	HS_POL	VS_POL	SDELVS	00H
0201	VSDELAY								00H
0202	-	-	-	-	-	-	-	YUV_RGB	00H
0203	OFD_STOP				OFD_START				54H
0204	RVODDP	OFDMTHD	RGB_SDFLD	SLVSFLD	-	CK_DLY			20H

LCDC : ADC/LLPLL

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
02C0	INPSELSOG		CS_INV	CS_SEL	SOG_SEL	HS_POL	HS_SEL	OUTCKSEL	00h
02C1	VS_POL	HS_POL	VS_DET	HS_DET	CS_DET	IN_SRC			
02C2	LLC_POST		LLC_VCO		-	LLC_IPMP			00h
02C3	LL_RSTVCO	LL_INSEL	LL_ICPSEL		LLC_ACKN[11:8]				03h
02C4	LLC_ACKN[7:0]								5Ah
02C5	LLC_PHA								00h
02C6	LLC_ACPL	LLC_APG			-	LLC_APZ			20h
02C7	LL_TEST	LL_BUFE	LL_VINEN	LL5PF	LLC_ACKI[11:8]				04h
02C8	LLC_ACKI[7:0]								00h
02C9	PRE_COAST								06h
02CA	POST_COAST								06h
02CB	PUSOG	PUPLL	-	SOG_TH					30h
02CC	LLCLK_DLY			PINVSSEL	HSY_SEL		VSY_POLC	HSY_POLC	00h
02CE	PINHSSEL	PDR	PDG	PDB	DTV	CLPEN	INREFI	INREFI	00h
02CF	INP_SEL_ADC		SAVE						24h
02D0	-					GAINY[8]	GAINC[8]	GAINV[8]	00h
02D1	GAINY								F0h
02D2	GAINC								F0h
02D3	GAINV								F0h
02D4	RGB_MODE	-	CL_EDGE	CKLY	CKLC	Y_CL_EN	C_CL_EN	V_CL_EN	00h
02D5	CL_START								00h
02D6	CL_END								12h
02D7	CL_LOC								70h
02D8	-	LLC_DBG_SEL			CL_TEST	ADC_TEST	CL_Y_TEST	CL_UV_TEST	00h
02D9	CL_G_VAL								10h
02DA	CL_B_VAL								80h
02DB	CL_R_VAL								80h
02DC	EDGE_SEL_LL	-	HSWID[5:0]						20h
02DD	OFFSETR								00h
02DE	OFFSETG								00h
02DF	OFFSETB								00h

LCDC – IIDTV 1 (Input Interface DTV 1)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0300	OFDM	RVODDP	SLVSFLD	DEONLY	DE_POL	HS_POL	VS_POL	-	00h
0301	-	-	EXT_HA	SELDE	-	DTVCK_DELAY			20h
0302	-	-	VSDL_65 6	UVA656	CR601	INPUT_DATA_BUS_ROUTING			04h
0303	-	-	-	-	INP_FORM				28h
0304	OFD_DET_END				OFD_DET_ST				54h
0305	SEL_HMX	-	-	-	-	-	-	-	00h
0306	VSDELAY[7:0]								00h
0307	SEQRGB_LTG[1:0]		SEQRGB_ORDER[1:0]		SEQRGB_SEL8BIT[1:0]		SEQRGB_POL	SEQRGB	00h
0310	-								00h
0311	-								00h
0312	-	-			-				00h
0313	TPG_EN	TPG_SWAP[2:0]			TPG_PAT[3:0]				00h

LCDC – IIDTV 2 (Input Interface DTV 2)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0320	OFDM	RVODDP	SLVSFLD	DEONLY	DE_POL	HS_POL	VS_POL	-	00h
0321	-	-	EXT_HA	SELDE	-	DTVCK_DELAY			20h
0322	-	-	VSDL_656	UVA656	CR601	INPUT_DATA_BUS_ROUTING			04h
0323	-	-	-	-	INP_FORM				28h
0324	OFD_DET_END				OFD_DET_ST				54h
0325	SEL_HMX	-	-	-	-	-	-	-	00h
0326	VSDELAY[7:0]								00h
0327	SEQRGB_LTG[1:0]		SEQRGB_ORDER[1:0]		SEQRGB_SEL8BIT[1:0]		SEQRGB_ POL	SEQRGB	00h
0330	-								00h
0331	-								00h
0332	-	-			-				00h
0333	TPG_EN	TPG_SWAP[2:0]			TPG_PAT[3:0]				00h

LCDC – Main Path Input Cropping

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0400	SW_RST_ SCALER	RVODDP99(DecFldInv)	LB_CE	-	-		IP_SEL		00h
0410	-	-	-	-	-	IP_HA_ST [10:0]			00h
0411	IP_HA_ST [10:0]								00h
0412	-	-	-	-	IP_HA_LEN [11:0]				02h
0413	IP_HA_LEN [11:0]								D0h
0414	-	-	-	-	-	-	IP_VA_ST_ODD [9:0]		00h
0415	IP_VA_ST_ODD [9:0]								13h
0416	EVN_OFFSET_NEG	IP_VA_ST_EVN_OFFSET [6:0]							01h
0417	-	-	-	-	IP_VA_LEN [10:0]				03h
0418	IP_VA_LEN [10:0]								00h

LCDC – Scaling

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0430	-	-	-	-	-	-	-	X_SCALE_UP [16:0]	00h
0431	X_SCALE_UP [16:0]								B4h
0432	X_SCALE_UP [16:0]								00h
0433	-	-	-	-	-	-	-	X_SCALE_DOWN [8:0]	00h
0434	X_SCALE_DOWN [8:0]								80h
0435	-	-	-	-	-	-	Y_SCALE_UP/DOWN [17:0]		00h
0436	Y_SCALE_UP/DOWN [17:0]								50h
0437	Y_SCALE_UP/DOWN [17:0]								00h
0438	X_OFFSET								00h
0439	Y_OFFSET_ODD								00h
043A	Y_OFFSET_EVEN								80h
043B	-	LNDB	PXDB	ZOOMBP	-		-	-	00h
043C	PANO_ENA	-	-	-	-	-	PANORAMA_WIDTH [9:8]		00h
043D	PANORAMA_WIDTH [7:0]								00h
043E	X_SCALE_UP_PAN (AT_THE_SIDE_FOR_PANORAMA)								00h
043F	DNSFIL_MAN	-	-	-	-	-	DNSFIL_MODE		00h

LCDC – Panel Display Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0470	RGB2BSFT_UP	DUAL_SELH	FPDATA_ZERO	-	-	-	DATA_0	DATA_BLU	00h
0471	SWAP_FPRGB	-	DEMODE	OP6B	TRIFP	-			00h
0472	-	-	-	-					05h
0473	FPHS_PERIOD [11:0]								3Ah
0474	FPHS_PW [7:0]								10h
0475	FPHS_BACK_PORCH [7:0]								1Bh
0476	-	-	-	-	-				04h
0477	FP_H_ACTIVE [10:0]								00h
0478	-	-	-	-	-				03h
0479	FPVS_PERIOD [10:0]								26h
047A	FPVS_PW [7:0]								06h
047B	FPVS_BACK_PORCH [7:0]								1Fh
047C	-	-	-	-	-				03h
047D	FP_V_ACTIVE [10:0]								00h
0480	-	-	-	-	-	-			00h
0481	THND [9:0]								00h
0482	THND2_EN	-	-	-	-	-			00h
0483	THND2 [9:0]								00h
0484	-	-	-	BLKTB [4:0]					00h
0485	BLKTB2_EN	-	-	BLKTB2 [4:0]					00h
0486	INT_DE_NO_DLY	-	-	-	FPEN_DLY[3:0]				00h
0487	-	-	-	-	FPHS_OUTPUT_DELAY [3:0]				00h
0488	-	-	-	-	DELAY FPVS [3:0]				08h
0489	UTVB	UTHB	DIST_HADH	ENA_HADJ	-	-	AUTOC	USEREG	00h
048A	-	-	EARLY_ST	-	AFRUN	FRERUN	-	TCON_DE_CON	00h
048B	LINE_VSCL	FRM_ALIN	FLD_ALIN	ALOW_QER	THRSH_VCHG [3:0]				04h
048C	LINEGONUM [7:0]								24h
048D	DISP_SNGFLD		RVF_AC	OLDTIME	-	-	EVNDLY		00h
048E	-								00h
048F	-								00h
0490	-	-	-						00h
0491	INI_CNT_ODD [12:0]								C0h
0492	-	-	-						00h
0493	INI_CNT_EVN [12:0]								C0h
0494	TGTPOS [7:0]								C0h
0495	-								00h
04C0	COUNTER_READ_BYTE_3								00h
04C1	COUNTER_READ_BYTE_2								00h
04C2	COUNTER_READ_BYTE_1								00h
04C3	COUNTER_READ_BYTE_0								00h
04C4	PCCINIA_INDEX		-	-	FRC_2F	FRC_1F	PCCINIA_SUB_INDX		00h

04C5	PCCTID		**00h**
04C6	COUNTER_READ_INDEX	-	**00h**

LCDC – Image Adjustment

<table>
<tr><th>Index (HEX)</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th>Reset value</th></tr>
<tr><td>0500</td><td>-</td><td>-</td><td colspan="6">HUE</td><td>20h</td></tr>
<tr><td>0501</td><td colspan="8">CONTRAST_R</td><td>80h</td></tr>
<tr><td>0502</td><td colspan="8">CONTRAST_G</td><td>80h</td></tr>
<tr><td>0503</td><td colspan="8">CONTRAST_B</td><td>80h</td></tr>
<tr><td>0504</td><td colspan="8">CONTRAST_Y</td><td>80h</td></tr>
<tr><td>0505</td><td colspan="8">CONTRAST_Cb</td><td>80h</td></tr>
<tr><td>0506</td><td colspan="8">CONTRAST_Cr</td><td>80h</td></tr>
<tr><td>0507</td><td colspan="8">BRIGHTNESS_R</td><td>80h</td></tr>
<tr><td>0508</td><td colspan="8">BRIGHTNESS_G</td><td>80h</td></tr>
<tr><td>0509</td><td colspan="8">BRIGHTNESS_B</td><td>80h</td></tr>
<tr><td>050A</td><td colspan="8">BRIGHTNESS_Y</td><td>80h</td></tr>
<tr><td>050B</td><td colspan="4">H_SHARP_COR</td><td colspan="4">H_SHARPNESS</td><td>3Fh</td></tr>
<tr><td>050C</td><td>H_SHARP_FREQ</td><td>-</td><td colspan="2">DYNR</td><td>-</td><td colspan="3">HFLT</td><td>00h</td></tr>
<tr><td>0510</td><td></td><td>-</td><td colspan="6">HUE2</td><td>20h</td></tr>
<tr><td>0511</td><td colspan="8">CONTRAST_R2</td><td>80h</td></tr>
<tr><td>0512</td><td colspan="8">CONTRAST_G2</td><td>80h</td></tr>
<tr><td>0513</td><td colspan="8">CONTRAST_B2</td><td>80h</td></tr>
<tr><td>0514</td><td colspan="8">CONTRAST_Y2</td><td>80h</td></tr>
<tr><td>0515</td><td colspan="8">CONTRAST_Cb2</td><td>80h</td></tr>
<tr><td>0516</td><td colspan="8">CONTRAST_Cr2</td><td>80h</td></tr>
<tr><td>0517</td><td colspan="8">BRIGHTNESS_R2</td><td>80h</td></tr>
<tr><td>0518</td><td colspan="8">BRIGHTNESS_G2</td><td>80h</td></tr>
<tr><td>0519</td><td colspan="8">BRIGHTNESS_B2</td><td>80h</td></tr>
<tr><td>051A</td><td colspan="8">BRIGHTNESS_Y2</td><td>80h</td></tr>
<tr><td>051B</td><td colspan="4">H_SHARP_COR2</td><td colspan="4">H_SHARPNESS2</td><td>3Fh</td></tr>
<tr><td>051C</td><td>H_SHARP_FREQ2</td><td>-</td><td colspan="2">DYNR2</td><td>-</td><td colspan="3">HFLT2</td><td>00h</td></tr>
<tr><td>0520</td><td>-</td><td>-</td><td colspan="6">HUE3</td><td>20h</td></tr>
<tr><td>0521</td><td colspan="8">CONTRAST_R3</td><td>80h</td></tr>
<tr><td>0522</td><td colspan="8">CONTRAST_G3</td><td>80h</td></tr>
<tr><td>0523</td><td colspan="8">CONTRAST_B3</td><td>80h</td></tr>
<tr><td>0524</td><td colspan="8">CONTRAST_Y3</td><td>80h</td></tr>
<tr><td>0525</td><td colspan="8">CONTRAST_Cb3</td><td>80h</td></tr>
<tr><td>0526</td><td colspan="8">CONTRAST_Cr3</td><td>80h</td></tr>
<tr><td>0527</td><td colspan="8">BRIGHTNESS_R3</td><td>80h</td></tr>
<tr><td>0528</td><td colspan="8">BRIGHTNESS_G3</td><td>80h</td></tr>
<tr><td>0529</td><td colspan="8">BRIGHTNESS_B3</td><td>80h</td></tr>
<tr><td>052A</td><td colspan="8">BRIGHTNESS_Y3</td><td>80h</td></tr>
<tr><td>052B</td><td colspan="4">H_SHARP_COR3</td><td colspan="4">H_SHARPNESS3</td><td>3Fh</td></tr>
<tr><td>052C</td><td>H_SHARP_FREQ3</td><td>-</td><td colspan="2">DYNR3</td><td>-</td><td colspan="3">HFLT3</td><td>00h</td></tr>
<tr><td>0530</td><td>T_BW</td><td>-</td><td>PEDLVL</td><td>WHTLVL</td><td>-</td><td>-</td><td>BPBW</td><td>-</td><td>1Ch</td></tr>
<tr><td>0531</td><td colspan="8">BW_LINE_ST_LO</td><td>08h</td></tr>
<tr><td>0532</td><td colspan="8">BW_LINE_END_LO</td><td>F6h</td></tr>
<tr><td>0533</td><td colspan="4">-</td><td colspan="2">BW_LINE_END_HI</td><td colspan="2">BW_LINE_ST_HI</td><td>08h</td></tr>
<tr><td>0534</td><td colspan="8">BW_H_DELAY</td><td>10h</td></tr>
</table>

LCDC – Image Adjustment

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0535	-	BW_H_FILTER_GAIN							0Bh
0536	BW_BLACK_TILT								67h
0537	BW_WHITE_TILT								94h
0538	BW_BLACK_GAIN								2Ah
0539	BW_WHITE_GAIN								D0h
053A	-	BW_GAIN							02h
053B	-								10h
0550	CE_CENTER0								3Dh
0551	CE_CENTER1								C3h
0552	CE_CENTER2								FCh
0553	CE_EN	CE_SPREAD0		CE_GAIN0					00h
0554	-	CE_SPREAD1		CE_GAIN1					00h
0555	-	CE_SPREAD2		CE_GAIN2					00h
0556	-								
0558	-								
0570	TPG_EN	SWAP[2:0]			PTTN_SEL[3:0]				00h

LCDC – PIP1 Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
8200	-						PIPGW_XST[9:8]		00h
8201	PIPGW_XST[7:0]								00h
8202	-					PIPGW_WIDTH[10:8]			02h
8203	PIPGW_WIDTH[7:0]								D0h
8204	-							PIPGW_YST[8]	00h
8205	PIPGW_YST[7:0]								02h
8206	-					PIPGW_HEIGHT[10:8]			00h
8207	PIPGW_HEIGHT[7:0]								E0h
8208	PPFIL_MAN	CK_INV	PPFIL_SEL		PIP_EFDOFF		PIP_OFDOFF		00h
8209	-				PIPDNSXFAC[11:8]				01h
820A	PIPDNSXFAC[7:0]								00h
820B	-				PIPDNSYFAC[11:8]				01h
820C	PIPDNSYFAC[7:0]								00h
820D	VSOFF_EN	DNSVS_OFFSET							00h
820E	PIP_WR_BASE[23:16]								00h
820F	PIP_WR_BASE[15:8]								00h
8210	PIP_WR_BASE[7:0]								00h
8211	-					PIP_WR_WIDTH[10:8]			02h
8212	PIP_WR_WIDTH[7:0]								D0h
8213	-						PIP_WR_HEIGHT[9:8]		00h
8214	PIP_WR_HEIGHT[7:0]								E0h
8215	WREN	WCPH	MUTE_C	-				RCPH	40h
8216	RDEN	FRM_MD	PIPEN	SNGL_FD	RDFDPOL	PXDB	LNDB	MUTE_EN	00h
8217	-				PUPSXFAC[11:8]				08h
8218	PUPSXFAC[7:0]								00h
8219	-				PUPSYFAC[11:8]				08h
821A	PUPSYFAC[7:0]								00h
821B	UPSVS_OFFSET								00h
821C	-				PIPWBASEX[11:8]				00h
821D	PIPWBASEX[7:0]								00h
821E	-					PIPWBASEY[10:8]			00h
821F	PIPWBASEY[7:0]								00h
8220	PIPWYOFF				PIPWXOFF				3Ah
8221	-				PIPWWIDTH[11:8]				02h
8222	PIPWWIDTH[7:0]								D0h
8223	-					PIPWHEIGHT[10:8]			00h
8224	PIPWHEIGHT[7:0]								E0h
8225	PIP_H_POS_ADJ								F7h
8226	PIP_V_POS_ADJ								FCh
8227	-								00h

LCDC – PIP2 Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
8230	-						PIP2GW_XST[9:8]		00h
8231	PIP2GW_XST[7:0]								00h
8232	-					PIP2GW_WIDTH[10:8]			02h
8233	PIP2GW_WIDTH[7:0]								D0h
8234	-							PIP2GW_ YST[8]	00h
8235	PIP2GW_YST[7:0]								02h
8236	-					PIP2GW_HEIGHT[10:8]			00h
8237	PIPGW_HEIGHT[7:0]								E0h
8238	PPFIL_MAN	CK_INV	PPFIL_SEL		PIP2_EFDOFF		PIP2_OFDOFF		00h
8239	-				PIP2DNSXFAC[11:8]				01h
823A	PIP2DNSXFAC[7:0]								00h
823B	-				PIP2DNSYFAC[11:8]				01h
823C	PIP2DNSYFAC[7:0]								00h
823D	VSOFF_EN	DNSVS_OFFSET							00h
823E	PIP2_WR_BASE[23:16]								00h
823F	PIP2_WR_BASE[15:8]								00h
8240	PIP2_WR_BASE[7:0]								00h
8241	-					PIP2_WR_WIDTH[10:8]			02h
8242	PIP2_WR_WIDTH[7:0]								D0h
8243	-						PIP2_WR_HEIGHT[9:8]		00h
8244	PIP2_WR_HEIGHT[7:0]								E0h
8245	WREN	WCPH	MUTE_C	-				RCPH	40h
8246	RDEN	FRM_MD	PIPEN	SNGL_FD	RDFDPOL	PXDB	LNDB	MUTE_EN	00h
8247	-				P2UPSXFAC[11:8]				08h
8248	P2UPSXFAC[7:0]								00h
8249	-				P2UPSYFAC[11:8]				08h
824A	P2UPSYFAC[7:0]								00h
824B	UPSVS_OFFSET								00h
824C	-				PIP2WBASEX[11:8]				00h
824D	PIP2WBASEX[7:0]								00h
824E	-					PIP2WBASEY[10:8]			00h
824F	PIP2WBASEY[7:0]								00h
8250	PIP2WYOFF				PIP2WXOFF				3Ah
8251	-				PIP2WWIDTH[11:8]				02h
8252	PIP2WWIDTH[7:0]								D0h
8253	-					PIP2WHEIGHT[10:8]			00h
8254	PIP2WHEIGHT[7:0]								E0h
8255	PIP2_H_POS_ADJ								F7h
8256	PIP2_V_POS_ADJ								FCh
8257	-								00h

LCDC – PIP1/PIP2 common Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
8260	PIP2_MRR	PIP_BORDER_H			PIP1_MRR	PIP_BORDER_W			00h
8261	MPIP_FRMCOLOR1[7:0]								1Ch
8262	MPIP_FRMCOLOR2[7:0]								00h
8263	PIP_RSTN	-							00h

LCDC – DV, PIP1/PIP2 common Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
8270	HALF_PCK	DV_REV	PNL_DV	DV_CHKR	DV_LRSAME		PIP_SWAP	DV_EN	00h
8271	DVLDEN1	DVLDEN2	DVLDEN3	-	PIP1_INSEL		PIP2_INSEL		C0h
8272	PMX_INSEL		PMX1_EN	PMX2_EN	ALPMX2_EN	SNDPIP	PIP2W_PDN	PIP1W_PDN	F0h

LCDC – PIP Alpha Blending Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
8280	BLEND_EN	MODE565	KEY_REV	ALPHA1					10h
8281	KEYDISP	-		ALPHA2					10h
8282	RKEY								00h
8283	GKEY								00h
8284	BKEY								00h
8285	RRANG								00h
8286	GRANG								00h
8287	BRANG								00h

LCDC – OSD

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0700	OSG_MODE		MSKSEL		COLOR_CON	BPP	BEXPM		
0701	OSG_STUS	FIFO_STUS	-	-	-	-	MCUWD	OP_START	
0702	Data Por For MCU/DMA Write Operation								
0703	-	OSD_HW	-	SP8TO16	OSG16FORM			OSDSRST	
0704	-	-	-	RLC_PKTE	-	-	RLC_RESET	RLC_ENA	
0705	RLC_DCNT				RLC_CNTT				
0706	OSD TEST	-	-	-	-			OSDPDN	
070B	BitBlt Logic								
070C	BitBlt Mask (HB)								
070D	BitBlt Mask (LB)								
070E	Block Fill Color (HB)								
070F	Block Fill Color (LB)								
0710	Bit Expansion Table for 8 Bit OSD								
0711									
0712									
0713									
0714									
0715									
0716									
0717									
0718									
0719									
071A									
071B									
071C									
071D									
071E									
071F									
0720	Bit Expansion Table for 16 Bit OSD								
0721									
0722									
0723									
0724									
0725									
0726									
0727									
0728									
0729									
072A									
072B									
072C									
072D									
072E									
072F									
0730									

0731		
0732		
0733		
0734		
0735		
0736		
0737		
0738		
0739		
073A		
073B		
073C		
073D		
073E		
073F		
0740	Color Conversion Source Color # 0	
0741		
0742	Color Conversion Source Color # 1	
0743		
0744	Color Conversion Source Color # 2	
0745		
0746	Color Conversion Source Color # 3	
0747		
0748	Color Conversion Target Color # 0	
0749		
074A	Color Conversion Target Color # 1	
074B		
074C	Color Conversion Target Color # 2	
074D		
074E	Color Conversion Target Color # 3	
074F		
0750	Selective Overwrite # 0	
0751		
0752	Selective Overwrite # 1	
0753		
0754	Selective Overwrite # 2	
0755		
0756	Selective Overwrite # 3	
0757		
0760	Source Buffer Memory Starting Address [23:0]	
0761		
0762		
0763	Source Buffer Memory Horizontal Length [7:0]	
0764	- -	
0765	Transfer Source Horizontal Start [10:0]	
0766	- -	
0767	Transfer Source Vertical Start [10:0]	
0768	-	
0769	Transfer Horizontal Length [11:0]	
076A	-	
076B	Transfer Vertical Length [11:0]	
0770	Destination Buffer Memory Starting Address [23:0]	

0771									
0772									
0773	Destination Buffer Memory Horizontal Length [7:0]								
0774	-				-				
0775	Transfer Destination Horizontal Start [10:0]								
0776	-				-				
0777	Transfer Destination Vertical Start [10:0]								

OSD

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0778	BLTSEL		FLIP	MIRROR	-	-	FUPDATE	OSDUPDATE	
0779	-	-	-	-	-	OSD Gain			
077A	LooK Up Table Select		-	-	-	-	-	-	
077B	Address Pointer for 8 Bit OSD Look Up Table								
077C	Look Up Table Data Port Byte 3								
077D	Look Up Table Data Port Byte 2								
077E	Look Up Table Data Port Byte 1								
077F	Look Up Table Data Port Byte 0								
0780	-	-	WIN0_PERPIX	WIN0_ALPHA_ENA	-	-	-	WIN0_ENA	
0781	-	-	-	-	-				
0782	OSD Window 0 Horizontal Start [10:0]								
0783	-	-	-	-	-				
0784	OSD Window 0 Vertical Start [10:0]								
0785	-	-	-	-					
0786	OSD Window 0 Horizontal Length [11:0]								
0787	-	-	-	-					
0788	OSD Window 0 Vertical Length [11:0]								
0789	Window 0 Buffer Memory Starting Address [23:0]								
078A									
078B									
078C	Window 0 Buffer Memory Horizontal Length [7:0]								
078D	Window 0 Buffer Memory Vertical Length [7:0]								
078E	-	-	-	-	-				
078F	Window 0 Image Horizontal Start [10:0]								
0790	-	-	-	-	-				
0791	Window 0 Image Vertical Start [10:0]								
0792	-	Window 0 Global Alpha Value							
07A0	-	-	WIN1_PERPIX	WIN1_ALPHA_ENA	-	-	-	WIN1_ENA	
07A1	-	-	-	-	-				
07A2	OSD Window 1 Horizontal Start [10:0]								
07A3	-	-	-	-	-				
07A4	OSD Window 1 Vertical Start [10:0]								
07A5	-	-	-	-					
07A6	OSD Window 1 Horizontal Length [11:0]								
07A7	-	-	-	-					
07A8	OSD Window 1 Vertical Length [11:0]								

07A9									
07AA	Window 1 Buffer Memory Starting Address [23:0]								
07AB									
07AC	Window 1 Buffer Memory Horizontal Length [7:0]								
07AD	Window 1 Buffer Memory Vertical Length [7:0]								
07AE	-	-	-	-	-				
07AF	Window 1 Image Horizontal Start [10:0]								
07B0	-	-	-	-	-				
07B1	Window 1 Image Vertical Start [10:0]								
07B2	-	Window 1 Global Alpha Value							
07C0	REV_CBR	-	WIN4_PERPIX	WIN4_ALPHA_ENA	OSD16FORM			WIN4_ENA	
07C1	-	-	-	-	-				
07C2	OSD Window 4 Horizontal Start [10:0]								
07C3	-	-	-	-	-				
07C4	OSD Window 4 Vertical Start [10:0]								
07C5	-	-	-	-					
07C6	OSD Window 4 Horizontal Length [11:0]								
07C7	-	-	-	-					
07C8	OSD Window 4 Vertical Length [11:0]								
07C9									
07CA	Window 4 Buffer Memory Starting Address [23:0]								
07CB									
07CC	Window 4 Buffer Memory Horizontal Length [7:0]								
07CD	Window 4 Buffer Memory Vertical Length [7:0]								
07CE	-	-	-	-	-				
07CF	Window 4 Image Horizontal Start [10:0]								
07D0	-	-	-	-	-				
07D1	Window 4 Image Vertical Start [10:0]								
07D2	-	Window 4 Global Alpha Value							
07D4	Color Key # 0								
07D5									
07D6	Color Key # 1								
07D7									
07D8	Color Key # 2								
07D9									
07DA	Color Key # 3								
07DB									
07DC	-	Alpha Value for Color Key # 0							
07DD	-	Alpha Value for Color Key # 1							
07DE	-	Alpha Value for Color Key # 2							
07DF	-	Alpha Value for Color Key # 3							

OSD Interrupt Enable, Vertical Active Status

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
07F0	-	-	DISP_ATE	OSD_ATE	WIN4_AT	-	WIN1_AT	WIN0_AT	
07F1	OSD_W_ MASK0	OSD_W_ MASK1	DISP_ATE _MASK	OSD_ATE _MASK	-	-	-	-	F0h

Main/Sub Path OSD Selection

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
07F8	-	-	SUB_SEL		-	-	MAIN_SEL		

External OSD

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
08F2	EOSD_M ODE	EOSD_VS _POL	EOSD_HS _POL	EOSD_CK _POL	EOSDDELAY [2:0]			OSD_POR TEN	
08F3	EOSD_HS_PW [5:0]						EXSYNC_ SEL	EXHACT_ SEL	
08F4	-	OCKTPS			-	-	-	-	
08F5	ENA_EA_ PIN	-	-	EXT_ALPHA [4:0]					
08F6	-	EODEN_DLY [2:0]			-	-	-	-	
08F7	-	-	-		EOSD_VS_PW [3:0]				

LCDC – Gamma & Dither & Key (waver_top)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0900	GAMAE_R	GAMAE_G	GAMAE_B	-	AUTO_INC		GAMMA_RGB_INDX		**00h**
0901	GAMMA_RAM_STARTING_ADDR								**00h**
0902	-	-	-	-	-	-	GAMMA_RAM_DATA[9:8]		**00h**
0903	GAMMA_RAM_DATA[7:0]								**00h**
0910 *<- 0917*	-	DITHER_OPTION			-	DITHER_FORMAT			**00h**
0920 *<- 0928*	RDKEYPOS_X[7:0]								
0921 *<- 0929*	RDKEYPOS_Y[7:0]								
0922 *<- 092A*	-	RDKEYPOS_Y[10:8]			RDKEYPOS_X[11:8]				
0923 *<- 092B*	KEYRDR								
0924 *<- 092C*	KEYRDG								
0925 *<- 092D*	KEYRDB								

LCDC – TGA & Power Management

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0970	-	FPDEAH	FPHSAH	FPVSAH	RVFPCK	RVHILO	RVBIT	FPCLKC	**40h**
0971	-	-	-	-	-	FPCKOUTDLY			**00h**
0987	-	-	PWMEN	PWMAL	-	-			**00h**
0988	PWM_CNT [7:0]								**00h**
0989	-	-	-	-	-	-			**00h**
098A	PWM_CLK_DIV[9:0]								**00h**
098B	-	-	PWM2EN	PWM2AL	-	-			**00h**
098C	PWM2_CNT [7:0]								**00h**
098D	-	-	-	-	-	-			**00h**
098E	PWM2_CLK_DIV[9:0]								**00h**
09F5	-	-	-	-	-	ENBIAS	EFPIF	EFPWR	**00h**

LCDC – TCON

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0A00	-	TCCK_PH	ROE_EN				TCONS	DIV_CK	00h
0A01	-				REV_EN	-	INV_SEL		00h
0A02	-				TOP_BTM		LFT_RHT		03h
0A03			POL_CON	RCK_P	ROE_P	RSP_P	CLP_P	CSP_P	07h
0A04			PGM_RCK	PGM_ROE	PGM_RSP	PGM_POL	PGM_CLP	PGM_CSP	34h
0A05	-								00h
0A06						FRC_DAC_INV	REV_SEL	ANAL_LCD	02h
0A0A	KP_SEL	KP_ENA	RSP_WIDTH		-		COMPANY		02h
0A0B	REVV_REVC								4Dh
0A0C	-				V_ST[11:8]				00h
0A0D	V_ST[7:0]								00h
0A0E	-				V_ED[11:8]				02h
0A0F	V_ED[7:0]								94h
0A10					CP_SW[11:8]				00h
0A11	CP_SW[7:0]								00h
0A12	-				CLP_ST[11:8]				00h
0A13	CLP_ST[7:0]								24h
0A14	-				CLP_ED[11:8]				00h
0A15	CLP_ED[7:0]								02h
0A1A	-				CSP_ST[11:8]				00h
0A1B	CSP_ST[7:0]								3Ch
0A1C	-				CSP_ED[11:8]				00h
0A1D	CSP_ED[7:0]								01h
0A20	-				RCK_ST[11:8]				00h
0A21	RCK_ST[7:0]								64h
0A22	-				RCK_ED[11:8]				01h
0A23	RCK_ED[7:0]								F4h
0A24	-				RSP_ST[11:8]				00h
0A25	RSP_ST[7:0]								37h
0A26	-				RSP_ED[11:8]				00h
0A27	RSP_ED[7:0]								01h
0A2C	-				ROE_ST[11:8]				00h
0A2D	ROE_ST[7:0]								0Ah
0A2E	-				ROE_ED[11:8]				00h
0A2F	ROE_ED[7:0]								36h
0A34	-				SHARP_STR_H				00h
0A35	SHARP_STR_L								20h
0A36	-				SHARP_END_H				01h
0A37	SHARP_END_L								E2h
0A38	CLPFB	-	CLPW[1:0]		-	CLPSEL[2:0]			15h
0A39	-		CSPW[1:0]		-	CSPSEL[2:0]			01h
0A3A	-		POL_H_ENA	POL_H_VAL	POL_STEP[3:0]				00h
0A3D	-		TRSP_STEP[5:0]						00h

0A3F	-	LINE_CON	SYNC_CON[1:0]	DELTA_LINE_CON	DELTA_LINE_EN	**00h**

LCDC – Input Measurement

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0B00	-	-	-	-	-	MEA_WIN_H_ST [10:0]			00h
0B01	MEA_WIN_H_ST [10:0]								20h
0B02	-	-	-	-	MEA_WIN_H_LEN [11:0]				01h
0B03	MEA_WIN_H_LEN [11:0]								E0h
0B04	-	-	-	-	-	MEA_WIN_V_ST [10:0]			00h
0B05	MEA_WIN_V_ST [10:0]								20h
0B06	-	-	-	-	-	MEA_WIN_V_LEN [10:0]			00h
0B07	MEA_WIN_V_LEN [10:0]								DAh
0B08	MEAS_SEL		-		FIELD_SEL		RD_LOCK	STARTM	00h
0B09	-	NOISE_MASK [2:0]			ERR_TOLER [2:0]			ENDET	00h
0B0A	THRESHOLD_FOR_ACT_DET [3:0]				ENALU	NOFSEL [1:0]		DE_MEA	30h
0B0B	-								-
0B0C	-								-
0B0D	-								-
0B0E	-								-
0B0F	-								-
0B10	-	-	-	PHASE_R [28:0]					-
0B11	PHASE_R [28:0]								-
0B12									-
0B13									-
0B14	-	-	-	PHASE_G [28:0]					-
0B15	PHASE_G [28:0]								-
0B16									-
0B17									-
0B18	-	-	-	PHASE_B [28:0]					-
0B19	PHASE_B [28:0]								-
0B1A									-
0B1B									-
0B1C	MIN_R [7:0]								-
0B1D	MIN_G [7:0]								-
0B1E	MIN_B [7:0]								-
0B1F	MAX_R [7:0]								-
0B20	MAX_G [7:0]								-
0B21	MAX_B [7:0]								-
0B22	-	-	-	-	-	V_PERIOD [10:0]			-
0B23	V_PERIOD [10:0]								-
0B24	H_PERIOD [15:0]								-
0B25									-
0B26	-	-	-	-	H_RISE_TO_FALL [11:0]				-
0B27	H_RISE_TO_FALL [11:0]								-
0B28	-	-	-	-	H_RISE_TO_ACT_END [11:0]				-
0B29	H_RISE_TO_ACT_END [11:0]								-
0B2A	-	-	-	-	-	V_RISE_TO_FALL [10:0]			-
0B2B	V_RISE_TO_FALL [10:0]								-
0B2C	-	-	-	-	V_RISE_TO_FALL [11:0]				-
0B2D	V_RISE_TO_FALL [11:0]								-
0B2E	-	-	-	-	H_ACT_ST_MIN [11:0]				-
0B2F	H_ACT_ST_MIN [11:0]								-
0B30	-	-	-	-	H_ACT_ST_MAX [11:0]				-
0B31	H_ACT_ST_MAX [11:0]								-

0B32	-	-	-	-					-
0B33	H_ACT_END_MIN [11:0]								-
0B34	-	-	-	-					-
0B35	H_ACT_END_MAX [11:0]								-
0B36	-	-	-	-	-				-
0B37	V_ACT_ST_1 [10:0]								-
0B38	-	-	-	-	-				-
0B39	V_ACT_ST_2 [10:0]								-
0B3A	-	-	-	-	-				-
0B3B	V_ACT_END_1 [10:0]								-
0B3C	-	-	-	-	-				-
0B3D	V_ACT_END_2 [10:0]								-
0B3E	-								-
0B3F	-								-
0B40	LUM_MIN [7:0]								-
0B41	LUM_MAX [7:0]								-
0B42	LUM_AVE [7:0]								-
0B43	-	-	-						-
0B44	V_PERIOD_27MH [20:0]								-
0B45									-

LCDC – DDR Memory Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0C00	-		DDR_DQS_SEL0						00h
0C01	-		DDR_DQS_SEL1						00h
0C02	DDR_CLKO_SEL			DDR_CLK90_SEL					28h
0C03	DLL_TST_SEL				-	DLL_TST	DLL_TAP_S		00h
0C04	DLL_RSTN	-	-		-		-		00h
0C05	RD_PH	-			DDR_DQS_DLY		DDR_WRNOP		08h
0C06	DDR_T_RC				DDR_T_RAS				A7h
0C07	DDR_T_RFC				-	DDR_T_RP			B4h
0C08	-	DDR_T_RCD			-	DDR_T_WR			43h
0C09	-	DDR_REFRESH			INIT_BYP	DDR_B_LENGTH			03h
0C0A	DDR_TST	DDR_CAS_LAT			SAMSNG	-			70h
0C0B	DDR_WTR	DDR_BTYP	DDR_DVST	DLL_EN	-	DDR_SIZE			11h
0C0C	DDR_RSTN	-	-	-	-	-	-		00h
0C0D	-	-	-	-	-	-	-	-	-
0C0E	-	-	-	-	-	-	-	-	-
0C0F	-	-	-	-	-	-	-	-	-

LCDC – Aux Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0CF0	AUX_RWDATA								00h
0CF1	-								00h
0CF2	AUX_ADDR[23:16]								00h
0CF3	AUX_ADDR[15:8]								00h
0CF4	AUX_ADDR[7:0]								00h
0CF5	-					AUX_LENGTH[10:8]			00h
0CF6	AUX_LENGTH[7:0]								00h
0CF7	-	-					AUX_RD	AUX_WR	00h

CCFL and LEDC Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0D00	-	-	-	-	-	-	-	BIASCTL	00h
0D01	OVEN	OIEN	UIEN	FBEN	LOCKV	LOCKH	CCFLENB	CCFLDEN	F2h
0D02	LVT		LILT		LIT				ADh
0D03	LEDC_DIG_EN	LEDC_APDWN	CCFL_LEDC_ST	LSTP	04h				
0D04	FPWM								70h
0D05	FDIM								84h
0D06	-	DDIM[6:0]							00h
0D07	PWMTOP								04h

TSC (Touch Screen Control)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0D10	PD_TSC	RST_TSC	START_ORG	PENQST	RDYQST	A[2:0]			80h
0D11	RSYINTENB	PENINTENB	R_SEL[2:0]			TESTADC[2:0]			00h
0D12	R0_DOUT[11:4]								00h
0D13	-	-	-	-	R0_DOUT[3:0]				00h
0D14	-	-	-	-	CONTSAMP	CLKSEL[2:0]			00h

LCDC : LVDS

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0D40	CTLMAPPING			BITPERPX[1:0]		LVDS_OP	FAB_TST	LCD_TST	00h
0D41	SEL_RD_SH	SWAP_CH	MX_REV_DCB	REV_BIT	DCB_POL	DCB	DUAL	MX_SEL	00h
0D42	CP_SEL[1:0]		LP_SEL[1:0]		-	-	SEL_LVDS[1:0]		00h

LCDC : REMOCON RX

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DA0	-	REMPOL	HTREF					HTINI[8]	66h
0DA1	HTINI[7:0]								B0h
0DA2	-	-	-	-	-	-	-	REMEN	00h
0DA3	-	-	-	-	REMERROR_FLAG	UPDLINT_FLAG	UPDINT_FLAG	HTINT_FLAG	
0DA4	-	-	HTCTRL	HTSYSTEM					
0DA5	-	-	HTCOMMAND						
0DA6	UPDREG[31:24]								
0DA7	UPDREG[23:16]								
0DA8	UPDREG[15:8]								
0DA9	UPDREG[7:0]								
0DAA	-	-	-	-	-	-	-	REMPI	
0DAB	REMCLKREF[15:8]								00h
0DAC	REMCLKREF[7:0]								27h
0DAD	-	-	-	-	UPDEN	HTEN	USAMPLE[9:8]		0Ch
0DAE	USAMPLE[7:0]								1Bh
0DAF	-	-	-	-	-	-	ULLEADER[9:8]		00h
0DB0	ULLEADER[7:0]								36h
0DB1	-	-	-	-	-	-	UHLEADER[9:8]		00h
0DB2	UHLEADER[7:0]								36h

LCDC – LOPOR

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DC0	-	-	-	-	-	-	-	PD_LSO	00h
0DC1	-				LVDETLVL[1:0]		DISDLYPOR	PD_POR	00h

LCDC – PLL (Panel Clock)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DD0	IP_P[2:0]			EDGE_SEL_P	FREQ_P[19:16]				80h
0DD1	FREQ_P[15:8]								00h
0DD2	FREQ_P[7:0]								00h
0DD3	SSFREQ_P[7:0]								00h
0DD4	SSG_P[3:0]				VCO_P[1:0]		POST_P[1:0]		00h
0DD5	PD_P	-	CPX4_P		LPX4_P		LPX8_P		00h
0DD6	-	-	-	-	-	DGAIN_P[2:0]			00h

LCDC – PLL (Memory Clock)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DD8	IP_M[2:0]			EDGE_SEL_M	FREQ_ M [19:16]				80h
0DD9	FREQ_ M [15:8]								00h
0DDA	FREQ_ M [7:0]								00h
0DDB	SSFREQ_ M [7:0]								00h
0DDC	SSG_ M [3:0]				VCO_ M [1:0]		POST_ M [1:0]		00h
0DDD	PD_M	-	CPX4_ M		LPX4_ M		LPX8_ M		00h
0DDE						DGAIN_M[2:0]			00h

LCDC – DAC

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DE0	DACGAIN				DAC_VCM			DACPD	00h

MCU

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F00	-					SPI_RD_MODE			00h
0F01	-		MCU_CK_RG		-	MCU_CK_DIV_RG			06h
0F02	-		SPI_CK_RG		-	SPI_CK_DIV_RG			06h
0F03	MODE_RG								40h
0F04	-					BUSY_CHECK	DMA_MODE		00h
0F05	DMA_WAIT								80h
0F06	DMA_REG_PAGE								06h
0F07	INDEX								00h
0F08	DMA_LENGTH[15:8]								00h
0F09	DMA_LENGTH[7:0]								00h
0F0A	WR_REG1_RG								00h
0F0B	WR_REG2_RG								00h
0F0C	WR_REG3_RG								00h

0F0D	WR_REG4_RG								**00h**
0F0E	WR_REG5_RG								**00h**
0F0F	CLK_SWITCH_WAIT								**1Fh**
0F10	DEFAULT R/W BUFFER1								**00h**
0F11	DEFAULT R/W BUFFER2								**00h**
0F12	DEFAULT R/W BUFFER3								**00h**
0F13	DEFAULT R/W BUFFER4								**00h**
0F14	DEFAULT R/W BUFFER5								**00h**
0F15	DEFAULT R/W BUFFER6								**00h**
0F16	DEFAULT R/W BUFFER7								**00h**
0F17	DEFAULT R/W BUFFER8								**00h**
0F18	STATUS_CMD_RG								**05h**
0F19	-				BUSY_POL	BUSY_SEL[2:0]			**08h**
0F1A	DMA_LENGTH[23:16]								**00h**
0F20	MCU STATUS	CHIP RESET	OSD DMA	-	RG_SPI_EN	CACHE_EN_RG	BOOTSEL	MCU RESET	**08h**
0F21	ISP PASSCODE WRITE PORT								**00h**
0F22	RG_DVIDT0[15:8]								**00h**
0F23	RG_DVIDT0[7:0]								**90h**
0F24	RG_DVIDT1[15:8]								**00h**
0F25	RG_DVIDT1[7:0]								**90h**
0F26	RG_DVIDT2[15:8]								**00h**
0F27	RG_DVIDT2[7:0]								**90h**
0F28	RG_DVIDT3[15:8]								**00h**
0F29	RG_DVIDT3[7:0]								**0Ch**
0F2A	RG_DVIDT4[15:8]								**00h**
0F2B	RG_DVIDT4[7:0]								**0Ch**
0F2C	OSD_WAIT[7:0]								**02h**
Special Function Register									
0X9A	RG_PGMBASE_ADR[7:0]								**00h**
0XFA	INT14~INT7 Flag								**00h**
0XFB	INT14~INT7 Enable								**00h**
0XFC	INT14~INT7 Priority								**00h**
0XFD	INT14~INT7 Edge/Level								**00h**
0XFE	INT14~INT7 Edge/Level Polarity								**00h**
0XE2	-						RG_PDN	-	**00h**
0X80	P0								**FFh**
0X81	SP								**07h**
0X82	DPL								**00h**
0X83	DPH								**00h**
0X84	DPL1								**00h**
0X85	DPH1								**00h**
0X86	DPS								**00h**
0X87	PCON								**00h**
0X88	TCON								**00h**
0X89	TMOD								**00h**

0X8A	TL0	00h
0X8B	TL1	00h
0X8C	TH0	00h
0X8D	TH1	00h
0X8E	CKCON	07h
0X90	P1	FFh
0X91	EIF	00h
0X92	WTST	00h
0X93	DPX0	00h
0X95	DPX1	00h
0X98	SCON0	00h
0X99	SBUF0	00h
0XA0	P2	00h
0XA8	IE	00h
0XB0	P3	FFh
0XB8	IP	00h
0XC0	SCON1	00h
0XC1	SBUF1	00h
0XC2	CCL1	00h
0XC3	CCH1	00h
0XC4	CCL2	00h
0XC5	CCH2	00h
0XC6	CCL3	00h
0XC7	CCH3	00h
0XC8	T2CON	00h
0XC9	T2IF	00h
0XCA	CRCL	00h
0XCB	CRCH	00h
0XCC	TL2	00h
0XCD	TH2	00h
0XCE	CCEN	00h
0XD0	PSW	00h
0XD8	WDCON	00h
0XE0	ACC	00h
0XE8	EIE	00h
0XE9	STATUS	00h
0XEA	MXAX	00h
0XEB	TA	00h
0XF0	B	00h
0XF8	EIP	00h
0XF8	MD0	00h

Global Register

0x000 – PRODUCT ID & REVISION

Bit	Function	R/W	Description	Reset
7-2	PROD_ID	R/W	Chip ID.	010_011
1-0	REVSION	R/W	Chip Revision Number	00

GPIO Registers

0x040 ~ 0x049 – GPIO Registers

Index (hex)	Bit	Function	R/W	Description	Reset
0x040	7-0	GPIO_EN 0	R/W	Gpio Enable (Active High)	00h
0x041	7-0	GPIO_EN 1	R/W	Gpio Enable (Active High)	00h
0x042	7-0	GPIO_EN 2	R/W	Gpio Enable (Active High)	00h
0x043	7-0	GPIO_EN 3	R/W	Gpio Enable (Active High)	00h
0x044	7-0	GPIO_EN 4	R/W	Gpio Enable (Active High)	00h
0x045	7-0	GPIO_EN 5	R/W	Gpio Enable (Active High)	00h
0x046	7-0	GPIO_EN 6	R/W	Gpio Enable (Active High)	00h
0x047	7-0	GPIO_EN 7	R/W	Gpio Enable (Active High)	00h
0x048	7-0	GPIO_EN 8	R/W	Gpio Enable (Active High)	00h
0x049	7-0	GPIO_EN 9	R/W	Gpio Enable (Active High)	00h

0x050 ~ 0x059 – GPIO Registers

Index (hex)	Bit	Function	R/W	Description	Reset
0x050	7-0	GPIO_OE 0	R/W	Gpio Output Enable (Active High)	00h
0x051	7-0	GPIO_OE 1	R/W	Gpio Output Enable (Active High)	00h
0x052	7-0	GPIO_OE 2	R/W	Gpio Output Enable (Active High)	00h
0x053	7-0	GPIO_OE 3	R/W	Gpio Output Enable (Active High)	00h
0x054	7-0	GPIO_OE 4	R/W	Gpio Output Enable (Active High)	00h
0x055	7-0	GPIO_OE 5	R/W	Gpio Output Enable (Active High)	00h
0x056	7-0	GPIO_OE 6	R/W	Gpio Output Enable (Active High)	00h
0x057	7-0	GPIO_OE 7	R/W	Gpio Output Enable (Active High)	00h
0x058	7-0	GPIO_OE 8	R/W	Gpio Output Enable (Active High)	00h
0x059	7-0	GPIO_OE 9	R/W	Gpio Output Enable (Active High)	00h

0x060 ~ 0x069 – GPIO Registers

Index (hex)	Bit	Function	R/W	Description	Reset
0x060	7-0	GPIO_ID 0	RO	Gpio Input data	00h
0x061	7-0	GPIO_ID 1	RO	Gpio Input data	00h
0x062	7-0	GPIO_ID 2	RO	Gpio Input data	00h
0x063	7-0	GPIO_ID 3	RO	Gpio Input data	00h
0x064	7-0	GPIO_ID 4	RO	Gpio Input data	00h
0x065	7-0	GPIO_ID 5	RO	Gpio Input data	00h
0x066	7-0	GPIO_ID 6	RO	Gpio Input data	00h
0x067	7-0	GPIO_ID 7	RO	Gpio Input data	00h
0x068	7-0	GPIO_ID 8	RO	Gpio Input data	00h
0x069	7-0	GPIO_ID 9	RO	Gpio Input data	00h

0x070 ~ 0x079 – GPIO Registers

Index (hex)	Bit	Function	R/W	Description	Reset
0x070	7-0	GPIO_OD 0	R/W	Gpio Output data	00h
0x071	7-0	GPIO_OD 1	R/W	Gpio Output data	00h
0x072	7-0	GPIO_OD 2	R/W	Gpio Output data	00h
0x073	7-0	GPIO_OD 3	R/W	Gpio Output data	00h
0x074	7-0	GPIO_OD 4	R/W	Gpio Output data	00h
0x075	7-0	GPIO_OD 5	R/W	Gpio Output data	00h
0x076	7-0	GPIO_OD 6	R/W	Gpio Output data	00h
0x077	7-0	GPIO_OD 7	R/W	Gpio Output data	00h
0x078	7-0	GPIO_OD 8	R/W	Gpio Output data	00h
0x079	7-0	GPIO_OD 9	R/W	Gpio Output data	00h

0x080 – Test GPO

Bit	Function	R/W	Description	Reset
7-4	*	R/W	Reserved	00h
3	TGPO_EN	R/W	Test Gpo Enable for pin 202	0h
2-0	TGPO_SEL	R/W	test gpo select for signal through pin 202 0 : vdloss 1 : field 2 : pwm 3 : LSO Clock 4 : PEN IRQ 5 : osd win active 6 : osd win active 7 : MBIST Test Pass	00h

0x090 ~ 0x099 – Pull Down & Up Registers

Index (hex)	Bit	Function	R/W	Description	Reset
0x090	7-0	PULLUD_EN_0	R/W		FFh
0x091	7-0	PULLUD_EN_1	R/W		FFh
0x092	7-0	PULLUD_EN_2	R/W		FFh
0x093	7-0	PULLUD_EN_3	R/W		F3h
0x094	7-0	PULLUD_EN_4	R/W		FFh
0x095	7-0	PULLUD_EN_5	R/W		FFh
0x096	7-0	PULLUD_EN_6	R/W		FFh
0x097	7-0	PULLUD_EN_7	R/W		mcu_en 0 : 3Fh mcu_en 1 : FFh
0x098	7-0	PULLUD_EN_8	R/W		mcu_en 0 : C0h mcu_en 1 : FFh
0x099	7-0	PULLUD_EN_9	R/W		F3h

0x0A0 – Mode Status

Bit	Function	R/W	Description	Reset
7	POR	R	Reset from Low Power Detection 0: Reset 1: Normal Status	1
6	I2C_CS	R	I2C Chip Address Select 0 : I2C Chip Address → 88 1 : I2C Chip Address → 8C	Value of “pin 045” when “pin 143”(reset) is Low
7	MCU_EN	R	Mcu Enable 0: Internal mcu disable 1: Internal mcu enable	Value of “pin 191” when “pin 143”(reset) is Low
6	HOST	R	Mode for host parallel Interface 0: Intel Mode 1: Non Intel Mode	Value of “pin 145” when “pin 143”(reset) is Low
7	BOOT_SEL	R	Mcu Boot from 0: SPI 1: Internal ROM	Value of “pin 145” when “pin 143”(reset) is Low
6	H_CSL	R	Chip Select when host parallel Interface mode	Value of “pin 192”
7	PWR_DN	R	Power Down for Xtal clock from pin “PWR_DN“	Value of “pin 142”
6	TEST	R	Production Test Mode from pin “TEST”	Value of “pin 144”

0x0A1 – DTV Input Mode

Bit	Function	R/W	Description	Reset
7-6	DUAL_DTV	R/W	Dual Dtv input mode 00: Only Dtv1 - Dtv1 : 24B/16B/8B601/8B656 - Dtv2 : No used 01: Dual Dtv Mode - Dtv1 : 16B/8B601/8B656 - Dtv2 : 8B656 10: Dual Dtv Mode - Dtv1 : 565(RGB) - Dtv2 : 8B656 11: Dual Dtv Mode - Dtv1 : 666(RGB) - Dtv2 : 8B656	0
5-1	*	R/W		0
0	SACNT	R/W	I2C Index Auto-increment Enable 0: Non-auto Mode 1: Auto Mode	0

0x0AA - 0x0AD – CLOCK CONTROL

0x0AA – Clock Control Option

Bit	Function	R/W	Description	Reset
7	EXT_PCLK	R/W	External Clock Use for Panel Clock	0
6	EXT_MCLK	R/W	External Clock Use for Memory Clock	0
2-1	PCK_CAP	R/W	Panel Out Clock Pin (FPCLK) Drive Capability 00 : 8mA 01 : 4mA 10 : 12mA 11 : 12mA	0

0x0AB – Clock Polarity

Bit	Function	R/W	Description	Reset
7	CKPOL_DBL	R/W	Clock Polarity for pclk of double pixel mode	0
6	CKPOL_DTV1	R/W	Clock Polarity for dtv1 clock	0
5	CKPOL_DTV2	R/W	Clock Polarity for dtv1 clock	0
4	CKPOL_SYS	R/W	Clock Polarity for system clock	0
3	CKPOL_P	R/W	Clock Polarity for panel clock	0
2	CKPOL_PDV	R/W	Clock Polarity for panel clock of Dual View mode	0
1	CKPOL_M	R/W	Clock Polarity for memory clk	0
0	CKPOL_Z	R/W	Clock Polarity for panel clock of zoom-by-pass mode	0

0x0AC : Clock Polarity

Bit	Function	R/W	Description	Reset
7-2	*	R/W	reserved	0
1	CKPOL_DEC	R/W	Clock Polarity for decoder clock	0
0	CKPOL_MAIN	R/W	Clock Polarity for main path clock	0

0x0AD : Clock Power Down

Bit	Function	R/W	Description	Reset
7	ClkPd_ALL	R/W	Clock Power Down for All Clock	0
6	CKPD_DTV1	R/W	Clock Power Down for dtv1 clock	0
5	CKPD_DTV2	R/W	Clock Power Down for dtv1 clock	0
4	CKPD_SYS	R/W	Clock Power Down for system clock	0
3	CKPD_P	R/W	Clock Power Down for panel clock	0
2	CKPD_PDV	R/W	Clock Power Down for panel clock of Dual View mode	0
1	CKPD_M	R/W	Clock Power Down for memory clk	0
0	*	R/W	reserved	0

Status & Interrupt

0x0B0 to 0x0BA – Status and Interrupt Registers

0x0B0 – Status Register

Bit	Function	R/W	Description	Reset
7	Line buffer over flow	R	This bit is set if the FP clock count exceeds the maximum number in between two consecutive FPHS pulses for the even field, cleared by writing back a "1".	0
6	Line buffer under flow	R	This bit is set if the FP clock count exceeds the maximum number in between two consecutive FPHS pulses for the odd field, cleared by writing back a "1".	0
5	Input VSYNC Loss status changed	R	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
4	Input HSYNC Loss status changed	R	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
3	Video input status changed indication	R	Vdloss status bit change (register 1 bit 7) or det50 status bit change (register 1 bit 0) Write a one to this bit to reset.	0
2	Input VSYNC Loss	R	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	0
1	Input HSYNC Loss	R	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	0
0	SYNC detect status	R	Logic function of: Inverted “bit 1” ANDing with inverted “bit 2”	

0x0B1– Status Register

Bit	Function	R/W	Description	Reset
7	Input Measurement Data Ready	R	This bit is set when the measurement data is ready for readout, reset when a new "startm" is set.	0
6	Power State Changed	R	This bit is set when the power management state has changed, reset by writing back a "1".	0
5	Input VSYNC Period Change Detected	R	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	0
4	Input HSYNC Period Change Detected	R	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	0
3	Line buffer Overflow or Underflow	R		0
2	VDCCDET	R	High if there is a change in VDLOSS or DET50 or CCVALID	0
1	VLOSS/ HLOSS status changed	R	This bit reflects the “OR” condition of status bit index B0 bit 5 (VLOSS status changed) and index B0 bit 4 (HLOSS status changed).	0
0	"SYNC Detect Status" Changed	R	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0

0x0B2– Interrupt Control Register

Bit	Function	R/W	Description	Reset
7	IRQ_B_B17	R/W	Enable/Disable 0x0B1 bit 7 as an IRQ source 0: Enable 1: Disable	1
6	IRQ_B_B16	R/W	Enable/Disable 0x0B1 bit 6 as an IRQ source 0: Enable 1: Disable	1
5	IRQ_B_B15	R/W	Enable/Disable 0x0B1 bit 5 as an IRQ source 0: Enable 1: Disable	1
4	IRQ_B_B14	R/W	Enable/Disable 0x0B1 bit 4 as an IRQ source 0: Enable 1: Disable	1
3	IRQ_B_B13	R/W	Enable/Disable 0x0B1 bit 3 as an IRQ source 0: Enable 1: Disable	1
2	IRQ_B_B12	R/W	Enable/Disable 0x0B1 bit 2 as an IRQ source 0: Enable 1: Disable	1
1	IRQ_B_B11	R/W	Enable/Disable 0x0B1 bit 1 as an IRQ source 0: Enable 1: Disable	1
0	IRQ_B_B10	R/W	Enable/Disable 0x0B1 bit 0 as an IRQ source 0: Enable 1: Disable	1

0x0B3 – Interrupt Control Register

Bit	Function	R/W	Description	Reset
7-3	-	R/W	Reserved	00h
2	IRQ_B_BD	R/W	Enable/Disable VDLOSS as an IRQ source 0: Enable 1: Disable	1
1	IRQ_B_CC	R/W	Reserved	1
0	IRQ_B_50	R/W	Enable/Disable DET50 as an IRQ source 0: Enable 1: Disable	1

0x0B4 – Status Register

Bit	Function	R/W	Description	Reset
7	Line buffer over flow	R	Same as 0x0B0[7]	0
6	Line buffer under flow	R	Same as 0x0B0[6]	0
5	PIP Input VSYNC Loss status changed	R	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
4	PIP Input HSYNC Loss status changed	R	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
3	Video input status changed indication	R/W	Same as 0x0B0[3]	0
2	PIP Input VSYNC Loss	R	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	0
1	PIP Input HSYNC Loss	R	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	0
0	PIP SYNC detect status	R	Logic function of: Inverted “bit 1” ANDing with inverted “bit 2”	

0x0B5 – Status Register

Bit	Function	R/W	Description	Reset
7	Input Measurement Data Ready	R	Same as 0x0B1[7]	0
6	Power State Changed	R	Same as 0x0B1[6]	0
5	PIP Input VSYNC Period Change Detected	R	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	0
4	PIP Input HSYNC Period Change Detected	R	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	0
3	Line buffer Overflow or Underflow	R	Same as 0x0B1[3]	0
2	VDCCDET	R	Same as 0x0B1[2]	0
1	PIP VLOSS/ HLOSS status changed	R	This bit reflects the “OR” condition of status bit index B0 bit 5 (VLOSS status changed) and index B0 bit 4 (HLOSS status changed).	0
0	PIP "SYNC Detect Status" Changed	R	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0

0x0B6 – Status Register

Bit	Function	R/W	Description	Reset
7	Line buffer over flow	R	Same as 0x0B0[7]	0
6	Line buffer under flow	R	Same as 0x0B0[6]	0
5	MPIP Input VSYNC Loss status changed	R	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
4	MPIP Input HSYNC Loss status changed	R	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0
3	Video input status changed indication	R/W	Same as 0x0B0[3]	0
2	MPIP Input VSYNC Loss	R	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	0
1	MPIP Input HSYNC Loss	R	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	0
0	MPIP SYNC detect status	R	Logic function of: Inverted "bit 1" ANDing with inverted "bit 2"	

0x0B7 – Status Register

Bit	Function	R/W	Description	Reset
7	Input Measurement Data Ready	R	This bit is set when the measurement data is ready for readout, reset when a new "startm" is set.	0
6	Power State Changed	R	Same as 0x0B1[6]	0
5	MPIP Input VSYNC Period Change Detected	R	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	0
4	MPIP Input HSYNC Period Change Detected	R	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	0
3	Line buffer Overflow or Underflow	R	Same as 0x0B1[3]	0
2	VDCCDET	R	Same as 0x0B1[2]	0
1	MPIP VLOSS/ HLOSS status changed	R	This bit reflects the "OR" condition of status bit index B0 bit 5 (VLOSS status changed) and index B0 bit 4 (HLOSS status changed).	0
0	MPIP "SYNC Detect Status" Changed	R	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	0

0x0B8 – Interrupt Mask Register

Bit	Function	R/W	Description	Reset
7- 6	Measurement input selection	R/W	0,1: Main, 2: PIP, 3: MPIP	00
5	IRQ_1B5_5	R/W	0: Enable 0x0B5[5] as an IRQ source	0
4	IRQ_1B5_4	R/W	0: Enable 0x0B5[4] as an IRQ source	0
3 - 2	-	R/W	Reserved	00
1	IRQ_1B5_1	R/W	0: Enable 0x0B5[1] as an IRQ source	0
0	IRQ_1B5_0	R/W	0: Enable 0x0B5[0] as an IRQ source	0

0x0B9 – Interrupt Mask Register

Bit	Function	R/W	Description	Reset
7- 6	-	R/W	Reserved	00
5	IRQ_1B7_5	R/W	0: Enable 0x0B7[5] as an IRQ source	0
4	IRQ_1B7_4	R/W	0: Enable 0x0B7[4] as an IRQ source	0
3 - 2	-	R/W	Reserved	00
1	IRQ_1B7_1	R/W	0: Enable 0x0B7[1] as an IRQ source	0
0	IRQ_1B7_0	R/W	0: Enable 0x0B7[0] as an IRQ source	0

0x0BA – IRQ

Bit	Function	R/W	Description	Reset
7	IRQ_OE	R/W	Irq Output Enable	0
6	IRQ_AL	R/W	Irq Active Low	0
5	IRQ_ST	R/W	Irq Status	0
4-0	*	R/W	Reserved	00

Internal Test

0x0C6 – Internal Test Control

Bit	Function	R/W	Description	Reset
7	SELC	R/W	Select C as for test data out	0
6	*	R/W	Reserved	0
5	DATA_ZERO		Set with RGB Data all “0”	0
4-0	*	R/W	Reserved	00

0x0C7 – Test Mode

Bit	Function	R/W	Description	Reset
7-0	BWYMIN	R	BWYMIN	-

0x0C8 – Test Mode

Bit	Function	R/W	Description	Reset
7-0	BWYMAX	R	BWYMAX	-

0x0C9 – Test Mode

Bit	Function	R/W	Description	Reset
7-0	BWFMIN	R	BWFMIN	-

0x0CA – Test Mode

Bit	Function	R/W	Description	Reset
7-0	BWFMAX	R	BWFMAX	-

0x0CB – Test Mode

Bit	Function	R/W	Description	Reset
7-0	BWBTILT	R	BWBTILT	-

0x0CC – Test Mode

Bit	Function	R/W	Description	Reset
7-0	BWWTILT	R	BWWTILT	-

0x0CE – Internal Test Mode

Bit	Function	R/W	Description	Reset
7-0	TEST_ MODE	R/W	TEST_MODE This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 03h = Digital video decoder & RGB mix direct input test This test mode allows digital data to be input from DTVD[23:0] pins to the input of the digital logic of the video decoder (replaces YCADC output) as the case when the contents of this register is 04h. Besides this, the FPG1/FPB1/FPR1 pins become inputs and provide data in place of RGBADC data output. 04h = Digital video decoder direct input test This test mode allows digital data to be input from DTVD pins to the input of the digital logic of the video decoder. (Replaces ADC output) DTVD(23-16) > "Y" decoder input data, DTVD(15-8) > "U" decoder input data DTVD(7-0) > "V" decoder input data 05h = Closed caption test mode. 06h = YCADC test mode (DTVD pins become outputs) YCADC digital output is made available externally. "Y" ADC output data > DTVD(15-8), "C" & "FB" ADC output data > DTVD(7-0) Index-63-bit-7 = 1 > "C" data Index-63-bit-7 = 0 > "FB" data. 07h = Digital video decoder output test (DTVD pins become outputs) The output of the digital video decoder output is available externally. "R" decoder out data > DTVD(23-16), "G" decoder out data > DTVD(15-8) "B" decoder out data > DTVD(7-0) "Vsync" > CLAMP "Hsync" > GPIO[1] "Hactive" > GPIO[0] 08h = RGBADC test mode (DTVD pins become outputs) RGBADC digital output is made available externally. "G" ADC output data > DTVD(15-8), "B" & "R" ADC output data > DTVD(7-0) Index-63-bit-7 = 1 > "B" data Index-63-bit-7 = 0 > "R" data. 09h = DAC test mode. DTVD[7:0] inputs are routed to the DAC data input "DIN". 11h = TW88 internal node to flat panel output	00h

0x0E0 – S/W Reset

Bit	Function	R/W	Description	Reset
7	SW_RST	R/W	Chip Software Reset (Self Clear Bit)	0
6-0	*	R/W	Reserved	00

Decoder

0x0101 – Chip Status Register (CSTATUS)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in a number of consecutive video lines specified by MISSCNT register) 0 = Video detected.	-
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	-
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	-
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	-
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	-
2	Reserved	-	Reserved	-
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	-
0	DET50	R	1 = 50Hz source detected 0 = 60Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	-

0x0102 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7,3-2	YSEL[2:0]	R/W	These three bits control the Y input video selection Mux. 0 = YIN0 1 = YIN1 2 = YIN2 3 = YIN3 Others = N/A	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	0 = Composite video decoding 1 = S-video decoding 2 = Component video decoding (for 480i / 576i input only) 3 = Reserved	0
1	CSEL	R/W	This bit controls the C input source selection. 0 = CIN0 1 = CIN1	0
0	Reserved	-	Reserved	-

0x0103 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	-	Reserved	-

0x0104 – CKHY

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-5	CKHY	R/W	Color killer time constant 0 = fast 3 = slow	0
4-0	Reserved	-	Reserved	-

0x0105 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	-	Reserved	-

0x0106 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	A 1 written to this bit resets the device to its default state but all register content remains unchanged. This bit is self-resetting.	0
6	PDMIX	R/W	Power Down for Mix	0
5	FBYP	R/W	0 = Anti-alias Filter Enable 1 = Bypass	0
4	AGC_ENB	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = 27 MHz clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	0
0	V_PDN	R/W	0 =V channel ADC in normal operation. 1 = V channel ADC in power down mode.	0

0x0107 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	-
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	-
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	-
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	-

0x0108 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	15

0x0109 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	-

0x010A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These registers can be accessed using the same index address by first changing the decoding format to the corresponding standard.	-

0x010B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0x010C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	False color reduction mode for SECAM. 1 = On 0 = Off	0
5	PALSW	R/W	1 = PAL switch sensitivity low 0 = PAL switch sensitivity normal	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level 0 = The black level is the same as the blank level	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC/PAL 0 = Notch filter	1
2	HCOMP	R/W	1 = Operation mode 1 (recommended) 0 = Operation mode 0	1
1	YCOMB	R/W	Comb filter operation in monochrome mode 1 = Off 0 = On	0
0	PDLY	R/W	PAL delay line 1 = disable 0 = enable	0

0x0110 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0x0111 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CONTRAST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	60

0x0112 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	Reserved	-	Reserved	-
5-4	CTI	R/W	Color transient improvement level control. There are 4 enhancement levels with 0 being the lowest and 3 being the highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with '15' being the strongest.	1

0x0113 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x0114 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x0115 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue. They have value from +96^{o} (7Fh) to -96^{o} (80h) with an increment of 0.75^{o}. The default value is 0 (00h). This is effective for NTSC standard only.	00

0x0116 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	-	Reserved	-

0x0117 – Vertical Peaking Control I

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	2
3	Reserved	-	Reserved	-
2-0	VSHP	R/W	These bits control the vertical peaking level with '0' being the minimum and '7' being the maximum.	0

0x0118 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring function for the CTI. It has internal step size of 2.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of the vertical peaking logic. It has an internal step size of 2.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5 dB 2 = 3 dB 3 = 6 dB (SECAM)	0

0x011C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	-
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	-
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	Standard	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x011D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x011E – Component Video Format (CVFMT)

Bit	Name	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-4	CVSTD	R	Component video input format detection. 0 = 480i 1 = 576i 2 = 480p 3 = 576p	-
3-0	CVFMT	R/W	Component video format selection. 0 = 480i 1 = 576i 2 = 480p 3 = 576p 8 = Auto	8

0x011F – ADC Control Register

Bit	Name	R/W	Description	Reset
7-3	Reserved	-	Reserved	-
2	VREF	R/W	Video ADC voltage reference control. 0 = normal operation	0
1	IREF	R/W	Video ADC bias control 0 = normal operation	0
0	SAVE	R/W	Video ADC reference current control 0=normal current 1=2/3 of normal current	0

0x0120 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. This determines the clamping pulse duration together with the CLPST register.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x0121 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value. Larger value decrease the AGC response time.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN[8]	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x0122 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN[7:0]	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x0123 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	D8

0x0124– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level is preset to 60d for 60Hz field rate or 63d for 50Hz field.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0x0125– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h for 60Hz field rate or 3Bh for 50Hz field rate.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0x0126 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits set the size for the horizontal sync detection window.	4

0x0127 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	2A

0x0128 – Vertical Control Register

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 0 = vertical count down mode 1 = search mode	0
2	DETV	R/W	0 = Normal Vsync logic 1 = recommended for special switching application only	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 0 = normal 1 = long	0

0x0129 – Vertical Control II

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control. (Reserved)	0
4-0	VSHT	R/W	Vsync output delay control in the increment of half line length (Reserved)	15

0x012A – Color Killer Level Control

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	2
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	20

0x012B – Comb Filter Control

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter combing control. Factory use only.	4
3-0	VTL	R/W	Adaptive Comb filter combing control. Factory use only.	4

0x012C – Luma Delay and HSYNC Control

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode 0 = Normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by SCURVE bit.	0

0x012D – Miscellaneous Control Register I (MISC1)

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6	EVCNT	R/W	1 = Even field counter in special mode 0 = Normal operation.	0
5	Reserved	-	Reserved	-
4	SDET	R/W	ID detection sensitivity. A "1" is recommended.	1
3	Reserved	-	Reserved	-
2	BYPASS	R/W	Debug use only	1
1-0	Reserved	-	Reserved	-

0x012E – Miscellaneous Control Register II (MISC2)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 0 = slow 1 = auto1 2 = auto 3 = Fast	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. 0 = Low 1 = Medium 2 = High 3 = Extended	1

0x012F – Miscellaneous Control III (MISC3)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	1 = special output mode 0 = Normal output	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Bluer. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x0130 – Macrovision Detection

Bit	Function	R/W	Description	Reset
7	SID_FAIL	R	Secam ID detection status, 1 = failed.	-
6	PID_FAIL	R	Pal ID detection status, 1 = failed.	-
5	FSC_FAIL	R	Sub carrier frequency detection status, 1 = failed.	-
4	SLOCK_FAIL	R	Sub carrier looking detection for standard discrimination, 1 = failed.	-
3	CSBAD	R	Macrovision color strpe detection unstable, 1 = unstable.	-
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	-
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	-
0	CTYPE2	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	-

0x0131 – CSTATUS III

Bit	Function	R/W	Description	Reset
7	VCR	R	1 = VCR mode	-
6	WKAIR	R	1= Weak Signal 0 = Normal	-
5	WKAIR1	R	Weak signal indicator.	-
4	VSTD	R	1 = Standard Signal 0 = non- standard signal	-
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	-
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	-
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	-
0	CCDET	R	1 = CC data detected. 0 = Not detected.	-

0x0132 – HFREF

Bit	Function	R/W	Description	Reset
7-0	Reserved	-	Reserved	-

0x0133 – Miscellaneous Control Register

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode. 0, 1 = Auto mode 2 = 60 Hz 3 = 50 Hz	0
5-4	YNR	R/W	Y HF Noise Reduction. 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level for sync top mode. 0 = Low 1 = Medium 2 = High 3=highest	1

0x0134 – NSEN/SSEN/PSEN/WKTH

Bit	Function	R/W	Description	Reset
7-6	Index	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDS = 3 controls the weak signal detection sensitivity (WKTH).	1A

0x0135 – Clamp Cntl2

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debug use. Factory use only.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = C channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	0
3	GTEST	R/W	Factory use only. 1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control. Factory use only.	0
1	CKLY	R/W	Clamping current control for Y. Factory use only.	0
0	CKLC	R/W	Clamping current control for C/V. Factory use only.	0

0x0138 – Analog Cntl

Bit	Function	R/W	Description	Reset
7-1	Reserved	-	Reserved	-
0	SY_C	R/W	YOUT control 0 = Y 1 = Y+C	0

LCDC – IIRGB (Input Interface RGB)

LCDC : ADC/LLPLL

0x02C0 – LLPLL Input Control Register

Bit	Function	R/W	Description	Reset
7-6	INP_SEL	R/W	SOG input selection. 0 = SOG0 1 = SOG1 2 = NA 3 = NA	0
5	CS_INV	R/W	CSYNC Detection Input Polarity, active low needed. 0 = Active High 1 = Active Low	0
4	CS_SEL	R/W	PLL Input Selection 0 = Slicer or HS 1 = CS_PAS	0
3	SOG_SEL	R/W	CSYNC Detection Selection 0 = SOG Slicer 1 = HSYNC	0
2	HSY_POL	R/W	PLL Input Polarity 0 = Active Low 1 = Active High	0
1	Reserved	-	Reserved	-
0	CK_SEL	R/W	PLL Output Clock selection 0 = Select PLL clock 1 = Select oscillator clock	0

0x02C1 – LLPLL Input Detection Register

Bit	Function	R/W	Description	Reset
7	VS_POL	R	Detected VSYNC polarity 0 = Active Low 1 = Active High	-
6	HS_POL	R	Detected HSYNC polarity 0 = Active Low 1 = Active High	-
5	VS_DET	R	VSYNC detection 0 = Not detect 1 = Detect	-
4	HS_DET	R	HSYNC detection 0 = Not detect 1 = Detect	-
3	CS_DET	R	Composite Sync detection 0 = Not detect 1 = Detect	-
2-0	DET_FMT	R	Composite Sync format detection 0 = 480i 1 = 576i 2 = 480p 3 = 576p 4 = 1080i 5 = 720p 6 = 1080p 7 = none of above	-

0x02C2 – LLPLL Control Register

Bit	Function	R/W	Description	Reset
7-6	LLC_POST	R/W	PLL post divider 0 = 1 1 = ½ 2 = ¼ 3 = 1/8	0
5-4	LLC_VCO	R/W	VCO range select (MHz) 0 = 5 ~ 27 1 = 10 ~ 54 2 = 20 ~ 108 3 = 40 ~ 216	0
3	Reserved	-	Reserved	-
2-0	LLC_IPMP	R/W	Charge pump currents (uA) 0 = 1.5 1 = 2.5 2 = 5 3 = 10 4 = 20 5 = 40 6 = 80 7 = 160	0

0x02C3 – LLPLL Divider High Register

Bit	Function	R/W	Description	Reset
7	LL_RSTVCO	R/W	RST_VCO for LLPLL	0
6	LL_INSEL	R/W	PLLIN_SEL for LLPLL	0
5-4	LL_ICPSEL	R/W	ICP_SEL[1:0] for LLPLL	0
3-0	LLC_ACKN[11:8]	R/W	PLL feedback divider.	3

0x02C4 – LLPLL Divider Low Register

Bit	Function	R/W	Description	Reset
7-0	LLC_ACKN[7:0]	R/W	PLL feedback divider	5A

0x02C5 – LLPLL Clock Phase Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	-	Reserved	-
4-0	LLC_PHA	R/W	This 5bit value adjusts the sampling phase in 32 steps across on pixel time. Each step represents an 11.25 degree shift in sampling phase.	00

0x02C6 – LLPLL Loop Control Register

Bit	Function	R/W	Description	Reset
7	LLC_ACPL	R/W	PLL loop control 0 = Closed Loop 1 = Open Loop	0
6-4	LLC_APG	R/W	PLL loop gain control	2
3	Reserved	-	Reserved	-
2-0	LLC_APZ	R/W	PLL filter control	0

0x02C7 – LLPLL VCO Control Register

Bit	Function	R/W	Description	Reset
7	LL_TEST	R/W	TEST_EN for LLPLL	0
6	LL_BUFE	R/W	BUF_EN for LLPLL	0
5	LL_VINEN	R/W	VIN_EN for LLPLL	0
4	LL_5PF	R/W	LP_5PF for LLPLL	0
3-0	LLC_ACKI[11-8]	R/W	PLL VCO nominal frequency. Reserved for internal use.	4

0x02C8 – LLPLL VCO Control Register

Bit	Function	R/W	Description	Reset
7-0	LLC_ACKI[7-0]	R/W	PLL_VCO nominal frequency. Reserved for internal use.	00

0x02C9 – LLPLL Pre Coast Register

Bit	Function	R/W	Description	Reset
7-0	PRE_COAST	R/W	Sets the number of HSYNC periods that coast is active before VSYNC edge.	06

0x02CA – LLPLL Post Coast Register

Bit	Function	R/W	Description	Reset
7-0	POST_COAST	R/W	Sets the number of HSYNC periods that coast is active after VSYNC edge.	06

0x02CB – SOG Threshold Register

Bit	Function	R/W	Description	Reset
7	PUSOG	R/W	SOG power down control 0 = power down	0
6	PUPLL	R/W	PLL power down control 0 = power down	0
5	COAST_EN	R/W	PLL Coast control 1 = Enable	1
4-0	SOG_TH[4:0]	R/W	SOG slicer threshold This bits control the comparator threshold of the SOG slicer at 10mV per every step. The setting value of 5''b00000 equals 330mV and the maximum setting value is 5'11111 which equals 10mV.	10

0x02CC – Scaler Sync Selection Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	-	Reserved	-
4	VSY_SEL	R/W	Active VSYNC select 0 = Composite Sync Separation Output 1 = VSYNC input pin	0
3-2	HSY_SEL	R/W	Active HSYNC select 0 = HSYNC pin 1 = CS_PAS 2 = Sync separator output 3 = HSO	0
1	VSY_POLC	R/W	VSYNC polarity control 0 = Active High 1 = Active Low	0
0	HSY_POLC	R/W	HSYNC polarity control 0 = Active High 1 = Active Low	0

0x02CE – RGB ADC Misc. Register

Bit	Function	R/W	Description	Reset
7	PINHSSEL	R/W	External Pin Hsync Select 1 = Pin Hsync use 0 = Internal Signal use	0
6	PDR	R/W	ADC Power Down For Red Channel 1 = Power Down 0 = Normal Operation	0
5	PDG	R/W	ADC Power Down For Green Channel 1 = Power Down 0 = Normal Operation	0
4	PDB	R/W	ADC Power Down For Blue Channel 1 = Power Down 0 = Normal Operation	0
3	DTV	R/W	ADC Input mode selection 1 = DTV 0 = RGB	0
2	CLPEN	R/W	Enable Clamp Operation 1 = Internal Clamp Use 0 = External Clamp Use	0
1	INREFV	R/W	ADC Reference voltage select 1 = Internal Reference Disable 0 = Internal Reference Enable	0
0	INREFI	R/W	ADC Bias Reference current select 1 = Bias Current Boost 0 = Bias Current Normal	0

0x02CF – RGB ADC Misc2. Register

Bit	Function	R/W	Description	Reset
7-6	INP_SEL_ADC	R/W	ADC Data Input pin Select 3 = Select input #3 2 = Select input #2 1 = Select input #1 0 = Select input #0	0
5-0	SAVE	R/W	PGA/ADC Power Save Mode [5:3] = PGA bias current control : Bigger value means Smaller current setting [2:0] = ADC bias current control : Bigger value means Smaller current setting	09

0x02D0 – Clamp Gain Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	-	Reserved	-
2	GAINY[8]	R/W	Y channel gain adjust bit[8]	0
1	GAINC[8]	R/W	C channel gain adjust bit[8]	0
0	GAINV[8]	R/W	V channel gain adjust bit[8]	0

0x02D1 – Y Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINY[7-0]	R/W	Y channel gain adjust bit[7-0]	F0

0x02D2 – C Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINC[7-0]	R/W	C channel gain adjust bit[7-0]	F0

0x02D3 – V Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINV[7-0]	R/W	V channel gain adjust bit[7-0]	F0

0x02D4 – Clamp Mode Control Register

Bit	Function	R/W	Description	Reset
7	RGB_SEL	R/W	RGB or YCV selection 0 = YCV Mode 1 = RGB Mode	0
6	Reserved	-	Reserved	-
5	CL_EDGE	R/W	Clamp reference edge	0
4	CLKY	R/W	Clamping current control 1	0
3	CLKC	R/W	Clamping current control 2	0
2	CL_Y_EN	R/W	Green / Y channel clamp 0 = enable, 1 = disable	0
1	CL_C_EN	R/W	Blue / C channel clamp 0 = enable, 1 = disable	0
0	CL_V_EN	R/W	Red / V channel clamp 0 = enable, 1 = disable	0

0x02D5 – Clamp Start Position Register

Bit	Function	R/W	Description	Reset
7-0	CL_ST	R/W	This register sets programmable clamping start position. It is start count value that after the trailing edge of the HSYNC signal.	00

0x02D6 – Clamp Stop Position Register

Bit	Function	R/W	Description	Reset
7-0	CL_ED	R/W	This register sets programmable clamping stop position. Clamping duration set between start and stop position.	10

0x02D7 – Clamp Master Location Register

Bit	Function	R/W	Description	Reset
7-0	CL_LOC	R/W	This bit sets the RGB(YCV) clamp position from the H sync edge.	70

0x02D8 – ADC TEST Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-4	LLC_DBG_SEL	R/W	Debugging register for internal use	0
3	Reserved	-	Reserved	-
2	RGB_ADC_TEST	R/W	Internal Test Only	0
1	CL_TEST_Y	R/W	Programmable Green / Y select 0 = Use default value (G:0x10, U/V:0x3c) 1 = Programmable value	0
0	CL_TEST_UV	R/W	Programmable Blue and Red / U and V select 0 = Use default value (R/B:0x10, U/V:0x80) 1 = Programmable value	0

0x02D9 – G Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_G_VAL	R/W	Green channel Clamping reference level in programmable mode.	10

0x02DA – B Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_B_VAL	R/W	Blue channel Clamping reference level in programmable mode.	80

0x02DB – R Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_R_VAL	R/W	Red channel Clamping reference level in programmable mode.	80

0x02DC – HSYNC Width Register

Bit	Function	R/W	Description	Reset
7	EDGE_SEL_LL	R/W	Edge Selection for LLPLL	0
6	Reserved	R/W	Reserved (Set always to “0”)	0
5-0	HSWID	R/W	Hsync Widith. The unit of HWSID is one clock cycle.	20

0x02DD – R Channel ADC Offset Register

Bit	Function	R/W	Description	Reset
7-0	OFFSETR	R/W	R Channel ADC Offset Value.	00

0x02DE – G Channel ADC Offset Register

Bit	Function	R/W	Description	Reset
7-0	OFFSETG	R/W	G Channel ADC Offset Value.	00

0x02DF – B Channel ADC Offset Register

Bit	Function	R/W	Description	Reset
7-0	OFFSETB	R/W	B Channel ADC Offset Value.	00

LCDC – IIDTV 1 (Input Interface DTV 1)

0x0300 – DTV1 Input Control

Bit	Function	R/W	Description	Reset
7	OFDM	R/W	Field Detection Method selection, applicable to DTV1 input only 0 = Use the relationship between Vsync pulse and Hsync pulse 1 = Use the Vsync rising (or falling) edge location inside or outside of the region defined by 0x0304 register	0
6	RVODDP	R/W	Invert detected field signal, applicable to DTV1 input only	0
5	SLVSFLD	R/W	Use the rising or falling edge of Vsync for field detection, applicable to DTV1 input only 0 = Falling edge 1 = Rising edge	0
4	DEONLY	R/W	DE only selection, applicable to DTV1 only Set this bit to “1” if the input has DE but no Vsync and no Hsync.	0
3	DE_POL	R/W	Invert DE polarity, applicable to DTV1 only 0 = Active High 1 = Active Low	0
2	HS_POL	R/W	Invert HSYNC polarity, applicable to DTV1 only 0 = Active High 1 = Active Low	0
1	VS_POL	R/W	Invert VSYNC polarity, applicable to DTV1 only 0 = Active High 1 = Active Low	0
0	-	R/W	Reserved	0

0x0301 – DTV1 Input Control

Bit	Function	R/W	Description	Reset
7 – 6	-	-	Reserved	-
5	EXT_HA	R/W	Select Explicit DE (Data Enable also called HA for Horizontal Active), applicable to DTV1 only 0 = HA is asserted by each set of cropping registers (Main Path: 0x0410 ~ 0x0418, PIP1: 0x2B0 ~ 0x2B5, PIP2: 0x2CA ~ 0x2CF 1 = HA is sourced by individual video source	1
4	SELDE	R/W	For DTV1 0 = DTVDE is used as the data enable (DE). 1 = DTVDE is used as HSYNC input	0
3	Reserved	-	Reserved	-
2 – 0	DTVCK_DELAY	R/W	Input clock DTVCLK delay time selection. 0 = No delay time inserted. Each increment increases the delay by 1 ns.	0

0x0302 – DTV1, RGB Input Control

Bit	Function	R/W	Description	Reset
7 – 6	-	-	Reserved	-
5	DTV1_VSDL_656	R/W	ITU656 even field VSYNC delay, applicable to DTV1 only 0 = No delay 1 = Delay the assertion to the falling edge of "ha"	0
4	DTV1_UVA656	R/W	Enable alternative Vsync generation for ITU656 input, applicable to DTV1 only 0 = Use "F" bit in interlaced mode, and "V" bit in progressive mode 1 = Use "V" bit in interlaced mode, and "F" bit in progressive mode	0
3	DTV1_CR601	R/W	Cb/Cr data order selection, applicable to DTV1 only Set this bit to 1 in 8 bit 601 mode if the Cr data arrives before Cb data.	0
2 - 0	DTV1_PRTS	R/W	Data bus routing selection for DTV1 For 24 bit YpbPr or 24 bit RGB DTV1D[23:16] DTV1D[15:8] DTV1D[7:0] 0: Pr/B Y/R Pb/G 1: Pr/B Pb/G Y/R 2: Pb/G Y/R Pr/B 3: Pb/G Pr/B Y/R 4: Y/R Pb/G Pr/B 5: Y/R Pr/B Pb/G For 16 bit YPb/Pr: Follow the table above with Y and Pb. Example: If Y data is connected to DTV1D[23:16] and Pb/Pr data is connected DTV1D[7:0], the bus routing selection should be set to "101". If Explicit DE, Inde0x0301 bit [5], is set, the very first DTV1DE is assumed to have Pb data. On the other hand if Explicit DE is reset, Index 0x0302 bit [3] is used to select the order of Pb /Pr. For 8 bit Y/Pb/Pr: Follow the table above with Pr. Example: If Y/Pb/Pr data is connected to DTV1D[15:8], the bus routing selection can be set to "011" or "101". Use the table below for the correct data order. Explicit DE Index-0x0302-bit-3 Index 0x0301-bit-5 Data Order 1 X 0 Pb-Y-Pr-Y 1 X 1 Pr-Y-Pb-Y 0 0 0 Pb-Y-Pr-Y 0 0 1 Pr-Y-Pb-Y 0 1 0 Y-Pb-Y-Pr 0 1 1 Y-Pr-Y-Pb	4

0x0304 – DTV1 Field Detection Region

Bit	Function	R/W	Description	Reset
7 - 4	DTV1_OFD_DET_END	R/W	Field detection Horizontal Ending Locations, applicable to DTV1 only	5
3 -0	DTV1_OFD_DET_ST	R/W	Field detection Horizontal Starting Locations, applicable to DTV1 only	4
			The decimal number in the "Start" column represents the starting clock count of a horizontal clock counter. The decimal number in the "End" column represents the ending clock count. A field is distinguished by either the rising/falling edge of the Vsync falls inside or outside of the region defined by the "Start" and "End" pair.	

	Start	End
0000	32	64
0001	64	128
0010	128	256
0011	192	384
0100	256	512
0101	320	640
0110	384	768
0111	448	896

	Start	End
1000	512	1024
1001	576	1152
1010	640	1280
1011	704	1408
1100	768	1536
1101	832	1664
1110	896	1792
1111	960	1920

0x0306 – DTV1 Vsync Delay

Bit	Function	R/W	Description	Reset
7 - 0	DTV1_VSDELAY	R/W	Input Vsync delay, applicable to DTV1 only (one input hsync per increment)	0

0x0307 –

Bit	Function	R/W	Description	Reset
7-6	SEQRGB_LTG	R/W	Sequentiall RGB alternative line data based on RGB input order 3 = G->B->R 2 = R->G->B 1 = B->R->G 0 = G->B->R	0
5-4	SEQRGB_ORDER	R/W	Sequentiall RGB Input order 3 = R->G->B 2 = B->R->G 1 = G->B->R 0 = R->G->B	0
3-2	SEGRGB_SEL8BIT	R/W	Sequentiall RGB Input 8 bit selection out of [23:0] 3 = Select 8 bit for [7:0] 2 = Select 8 bit for [23:16] 1 = Select 8 bit for [15:0] 0 = Select 8 bit for [7:0]	0
1	SEQRGB_POL	R/W	0 = Sequential RGB Clock polarity disable 1 = Sequential RGB Clock polarity Inversion	0
0	SEQRGB	R/W	0 = Sequential RGB mode disable 1 Sequential RGB mode enable	0

0x0313 – Test Pattern Generator Control Register

Bit	Function	R/W	Description	Reset
7	TPG_EN	R/W	1: Test pattern generator enable, 0: Normal (DTV input)	
6-4	TPG_CSWAP	R/W	Color swap for test pattern generator 0: RGB (default) 1: GBR 2: BRG 3: RBG 4: GRB 5: BGR 6, 7: (same as 0)	
3-0	TPG_PAT	R/W	Test pattern selection 0: 100% white VGA sized border (1 dot thickness) with black inside 1: VGA border (selection 0) plus H/V cross in the middle 2: Gray scale 3: 100% blue 4: 100% blue (in RGB space) 5-F : 50% gray	

LCDC – IIDTV 2 (Input Interface DTV 2)

0x0320 – DTV2 Input Control

Bit	Function	R/W	Description	Reset
7	OFDM	R/W	Field Detection Method selection, applicable to DTV2 input only 0 = Use the relationship between Vsync pulse and Hsync pulse 1 = Use the Vsync rising (or falling) edge location inside or outside of the region defined by 0x0324 register	0
6	RVODDP	R/W	Invert detected field signal, applicable to DTV2 input only	0
5	SLVSFLD	R/W	Use the rising or falling edge of Vsync for field detection, applicable to DTV2 input only 0 = Falling edge 1 = Rising edge	0
4	DEONLY	R/W	DE only selection, applicable to DTV2 only Set this bit to “1” if the input has DE but no Vsync and no Hsync.	0
3	DE_POL	R/W	Invert DE polarity, applicable to DTV2 only 0 = Active High 1 = Active Low	0
2	HS_POL	R/W	Invert HSYNC polarity, applicable to DTV2 only 0 = Active High 1 = Active Low	0
1	VS_POL	R/W	Invert VSYNC polarity, applicable to DTV2 only 0 = Active High 1 = Active Low	0
0	-	R/W	Reserved	0

0x0321 – DTV2 Input Control

Bit	Function	R/W	Description	Reset
7 – 6	-	-	Reserved	-
5	EXT_HA	R/W	Select Explicit DE (Data Enable also called HA for Horizontal Active), applicable to DTV2 only 0 = HA is asserted by each set of cropping registers (Main Path: 0x0410 ~ 0x0418, PIP1: 0x2B0 ~ 0x2B5, PIP2: 0x2CA ~ 0x2CF 1 = HA is sourced by individual video source	1
4	SELDE	R/W	For DTV2 0 = DTVDE is used as the data enable (DE). 1 = DTVDE is used as HSYNC input	0
3	Reserved	-	Reserved	-
2 – 0	DTVCK_DELAY	R/W	Input clock DTVCLK delay time selection. 0 = No delay time inserted. Each increment increases the delay by 1 ns.	0

0x0322 – DTV2, RGB Input Control

Bit	Function	R/W	Description	Reset
7 – 6	-	-	Reserved	-
5	DTV2_VSDL_656	R/W	ITU656 even field VSYNC delay, applicable to DTV2 only 0 = No delay 1 = Delay the assertion to the falling edge of “ha”	0
4	DTV2_UVA656	R/W	Enable alternative Vsync generation for ITU656 input, applicable to DTV2 only 0 = Use “F” bit in interlaced mode, and “V” bit in progressive mode 1 = Use “V” bit in interlaced mode, and “F” bit in progressive mode	0
3	DTV2_CR601	R/W	Cb/Cr data order selection, applicable to DTV2 only Set this bit to 1 in 8 bit 601 mode if the Cr data arrives before Cb data.	0
2 - 0	DTV2_PRTS	R/W	Data bus routing selection for DTV2 For 24 bit YpbPr or 24 bit RGB DTV2D[23:16] DTV2D[15:8] DTV2D[7:0] 0: Pr/B Y/R Pb/G 1: Pr/B Pb/G Y/R 2: Pb/G Y/R Pr/B 3: Pb/G Pr/B Y/R 4: Y/R Pb/G Pr/B 5: Y/R Pr/B Pb/G For 16 bit YPb/Pr: Follow the table above with Y and Pb. Example: If Y data is connected to DTV2D[23:16] and Pb/Pr data is connected DTV2D[7:0], the bus routing selection should be set to “101”. If Explicit DE, Inde0x0321 bit [5], is set, the very first DTV2DE is assumed to have Pb data. On the other hand if Explicit DE is reset, Index 0x322 bit [3] is used to select the order of Pb /Pr. For 8 bit Y/Pb/Pr: Follow the table above with Pr. Example: If Y/Pb/Pr data is connected to DTV2D[15:8], the bus routing selection can be set to “011” or “101”. Use the table below for the correct data order. Explicit DE / Index-0x0322-bit-3 / Index 0x0321-bit-5 / Data Order 1 X 0 Pb-Y-Pr-Y 1 X 1 Pr-Y-Pb-Y 0 0 0 Pb-Y-Pr-Y 0 0 1 Pr-Y-Pb-Y 0 1 0 Y-Pb-Y-Pr 0 1 1 Y-Pr-Y-Pb	4

0x0324 – DTV2 Field Detection Region

Bit	Function	R/W	Description	Reset
7 - 4	DTV2_OFD_DET_END	R/W	Field detection Horizontal Ending Locations, applicable to DTV2 only	5
3 -0	DTV2_OFD_DET_ST	R/W	Field detection Horizontal Starting Locations, applicable to DTV2 only	4
			The decimal number in the "Start" column represents the starting clock count of a horizontal clock counter. The decimal number in the "End" column represents the ending clock count. A field is distinguished by either the rising/falling edge of the Vsync falls inside or outside of the region defined by the "Start" and "End" pair.	

	Start	End		Start	End
0000	32	64	1000	512	1024
0001	64	128	1001	576	1152
0010	128	256	1010	640	1280
0011	192	384	1011	704	1408
0100	256	512	1100	768	1536
0101	320	640	1101	832	1664
0110	384	768	1110	896	1792
0111	448	896	1111	960	1920

0x0326 – DTV2 Vsync Delay

Bit	Function	R/W	Description	Reset
7 - 0	DTV2_VSDELAY	R/W	Input Vsync delay, applicable to DTV2 only (one input hsync per increment)	0

0x0327 –

Bit	Function	R/W	Description	Reset
7-6	SEQRGB_LTG	R/W	Sequential RGB alternative line data based on RGB input order 3 = G->B->R 2 = R->G->B 1 = B->R->G 0 = G->B->R	0
5-4	SEQRGB_ORDER	R/W	Sequential RGB Input order 3 = R->G->B 2 = B->R->G 1 = G->B->R 0 = R->G->B	0
3-2	SEGRGB_SEL8BIT	R/W	Sequential RGB Input 8 bit selection out of [23:0] 3 = Select 8 bit for [7:0] 2 = Select 8 bit for [23:16] 1 = Select 8 bit for [15:0] 0 = Select 8 bit for [7:0]	0
1	SEQRGB_POL	R/W	0 = Sequential RGB Clock polarity disable 1 = Sequential RGB Clock polarity Inversion	0
0	SEQRGB	R/W	0 = Sequential RGB mode disable 1 Sequential RGB mode enable	0

0x0333 – Test Pattern Generator Control Register

Bit	Function	R/W	Description	Reset
7	TPG_EN	R/W	1: Test pattern generator enable, 0: Normal (DTV2 input)	
6-4	TPG_CSWAP	R/W	Color swap for test pattern generator 0: RGB (default) 1: GBR 2: BRG 3: RBG 4: GRB 5: BGR 6, 7: (same as 0)	
3-0	TPG_PAT	R/W	Test pattern selection 0: 100% white VGA sized border (1 dot thickness) with black inside 1: VGA border (selection 0) plus H/V cross in the middle 2: Gray scale 3: 100% blue 4: 100% blue (in RGB space) 5-F : 50% gray	

LCDC – Main Path Input Cropping

0x0400 – Main Scaler Control (soft reset, input selection, etc) Register

Bit	Function	R/W	Description	Reset
7	SW_RST_SCALER	R/W	Reset the scaler module	0
6	RVODDP99	R/W	Invert the internal decoder filed signal	0
5	LB_CE	R/W	Line buffer chip enable	0
4 – 2	Reserved	-	Reserved	0
1 – 0	IP_SEL	R/W	Scaler Input source selection; 0 = Internal analog video decoder, 1 = Analog RGB 2 = DTV1 3 = DTV2	0

0x0410 ~ 0x0411 Main Scaler Active Window Horizontal Start [10:0] Registers

0x0410 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 - 0	IP_HA_ST[10:8]	R/W	Main Path Input active window horizontal starting position - high	0

0x0411 Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	IP_HA_ST[7:0]	R/W	Main Path Input active window horizontal starting position – low One pixel per increment	0

0x0412 ~ 0x0413 Main Scaler Active Window Horizontal Length [10:0] Registers

0x0412 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 - 0	IP_HA_LEN[10:8]	R/W	Main Path Input active window horizontal length - high	2

0x0413 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	IP_HA_LEN[7:0]	R/W	Main Path Input active window horizontal length – low One pixel per increment	D0h

0x0414 ~ 0x0415 Main Scaler Active Window Vertical Start – Odd Field [10:0]

0x0414 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 - 0	IP_VA_ST_ODD[10:8]	R/W	Main Path Input active window odd field vertical starting position - high	0

0x0415 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	IP_VA_ST_ODD[7:0]	R/W	Main Path Input active window odd field vertical starting position – low One line per increment	13h

0x0416 – Main Scaler Active Window Vertical Start Offset Register – Even Field

Bit	Function	R/W	Description	Reset
7	EVN_OFFSET_NEG	R/W	Positive or negative offset of even field from odd field. 0: Positive – Even field vertical start later than odd field 1: Negative – Even field vertical start earlier than odd field	0
6 - 0	IP_VA_ST_EVN_OFFSET	R/W	Offset value of the even field vertical starting position from the odd field One line per increment	1

0x0417 ~ 0x0418 Main Scaler Active Window Vertical Length [10:0] Registers

0x0417– High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 - 0	IP_VA_LEN[10:8]	R/W	Main Path Input active window vertical length - high	3

0x0418 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	IP_VA_LEN[7:0]	R/W	Main Path Input active window vertical length – low One linel per increment	0

LCDC – Scaling

0x0430 ~ 0x0432 Horizontal Up Scaling Factor [16:0] Registers

0x0430 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 1	Reserved	-	Reserved	0
0	X_SCALE_UP[16]	R/W	Horizontal (X-Direction) Scale Up Factor - high	0

0x0431 – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	X_SCALE_UP[15:8]	R/W	Horizontal (X-Direction) Scale Up Factor - mid	B4h

0x0432 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	X_SCALE_UP[7:0]	R/W	Horizontal (X-Direction) Scale Up Factor – low Horizontal Scale Up Factor = 65536 * (Input Horizontal Active Pixel Number) / (Flat Panel Horizontal Active Pixel Number) Example: VGA 640x480 , Panel Resolution: 1024x768 65536 * 640 / 1024 = 40960 = 0A000h Example: Decoder 720x240, Panel Resolution: 1024x768 65536 * 720 / 1024 = 46080 = 0B400h	0

0x0433 ~ 0x0434 Horizontal Down Scaling Factor [8:0] Registers

0x0433 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 1	Reserved	-	Reserved	0
0	X_SCALE_DOWN_[8]	R/W	Horizontal (X-Direction) Scale Down Factor - high	0

0x0434 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	X_SCALE_DOWN_LO	R/W	Horizontal (X-Direction) Scale Down Factor - low Horizontal Scale Down Factor = 128 * (Input Horizontal Active Pixel Number) / (Flat Panel Horizontal Active Pixel Number) Example: Decoder 720x240, Panel Resolution: 640x480 128 * 720 / 640 = 144 = 090h	80h

0x0435 ~ 0x0437 Vertical Scaling Factor [17:0] Registers

0x0435 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 2	Reserved	-	Reserved	0
1 – 0	Y_SCALE_UP/ DOWN [17:16]	R/W	Vertical (Y-Direction) Scale Up/Down Factor – high	0

0x0436 – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	Y_SCALE_UP/ DOWN [15:8]	R/W	Vertical (Y-Direction) Scale Up/Down Factor – mid	50h

0x0437 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	Y_SCALE_UP/ DOWN [7:0]	R/W	Vertical (Y-Direction) Scale Up/Down Factor – low The vertical scale factor can be derived in two ways: 1. Use active line number Vertical Scale Factor = 65536 * (Input Vertical Active Line Number) / (Flat Panel Vertical Active Line Number) 2. Use total line number Vertical Scale Factor = 65536 * (Input Vertical Total Line Number) / (Flat Panel Vertical Period Line Number) Example: VGA 640x480 , Panel resolution: 1024x768 65536 * 480 / 768 = 40960 = 0A000h Example: Decoder total vertical lines in one field 262.5, Panel vertical periods: 802 65536 * 262.5 / 802 = 21450 = 053CAh	0

0x0438 – Horizontal Up Scaling Offset [7:0] Register

Bit	Function	R/W	Description	Reset
7 - 0	X_OFFSET	R/W	Horizontal (X-Direction) Scale Up Offset This offset is used to adjust the initial value for the X-Direction scale up operation.	0

0x0439 – Vertical Scaling Offset [7:0] Register (Odd Field)

Bit	Function	R/W	Description	Reset
7- 0	Y_ODD_OFFS ET	R/W	Vertical (Y-Direction) Scale Up Offset for Odd field This offset is used to adjust the initial value for the Y-Direction scale up operation.	0

0x043A – Vertical Scaling Offset [7:0] Register (Even Field)

Bit	Function	R/W	Description	Reset
7 - 0	Y_EVN_OFFS ET	R/W	Vertical (Y-Direction) Scale Up Offset for Even field This offset is used to adjust the initial value for the Y-Direction scale up operation.	80h

0x043B – Misc Scaling Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	0
6	LNDB	R/W	1 = Line doubling 0 = Normal vertical scaling	0
5	PXDB	R/W	1 = Pixel doubling 0 = Normal horizontal scaling	0
4	ZOOMBP	R/W	Set Zoom by-pass. When this bit is set, the Horizontal and Vertical scale up factors has no effects.	0
3 - 0	Reserved	-	Reserved	0

0x043C ~ 0x043D Panorama Width Registers

0x043C – High Byte Register

Bit	Function	R/W	Description	Reset
7	PANO_ENA	R/W	Enable Panorama scaling operation 1: Enable 0: Disable	0
6-2	Reserved	-	Reserved	0
1- 0	PANA_WIDTH_HI	R/W	Panorama horizontal width - high	0

0x043D – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	PANA_WIDTH_LO	R/W	Panorama horizontal width - low	0

0x043E – Horizontal Up Scaling Factor for Panorama Register

Bit	Function	R/W	Description	Reset
7 - 0	X_SCALE_UP_PAN	R/W	Horizontal scale at the side of display in panorama scaling mode.	0

0x043F – Horizontal Down Scaling Filter

Bit	Function	R/W	Description	Reset
7	DNSFIL_MAN	R/W	1 = Down scaler pre-filter manual mode 0 = Auto mode	0
6 - 2	Reserved	-	Reserved	0
1 - 0	DNSFIL_MODE	R/W	Down scaler pre-filter manual selection 0 = No filter – 3 = Strongest	0

LCDC – Panel Display Control

0x0470 – Display Control Register

Bit	Function	R/W	Description	Reset
7	RGB2BSFT-UP	R/W	RGB Output 2 bit Shift Up	0
6	DUAL_SELH	R/W	0 = Panel data output selection lower 24 of 48 bits 1 = Panel data output selection upper 24 of 48 bits	0
5	FPDATA_ZERO	R/W	FP digital data all Zero 0 = Normal 1 = Data All Zero	0
4 - 2	Reserved	-	Reserved	0
1	DATA_0	R/W	Force scaler data output to all 0's	0
0	DATA_BLU	R/W	Force scaler data output blue	0

0x0471 – Panel Output Signal Control Register

Bit	Function	R/W	Description	Reset
7	SWAP_FPRGB	R/W	Swapping Red and Blue data bus 0 = No swapping 1 = Data bus swapping red and blue	0
6	Reserved	-	Reserved	0
5	DEMODE	R/W	DE mode selection 1= FPVS and FPHS are forced to inactive state.	0
4	OP6B	R/W	FP data outputs shift down 2 bits. When set, FPR0, FPR1, FPG0, FPG1, FPB0, FPB1 bus signals are shifted down by 2 bits.	0
3	TRIFP	R/W	Tri-state all the output signals to flat panel.	0
2 - 0	Reserved	-	Reserved	0

0x0472 ~ 0x0473 Panel Output Hsync Period [11:0] Registers

0x0472 – High Byte Register

Bit	Function	R/W	Description	Reset
7 - 4	Reserved	-	Reserved	0
3 - 0	FPHS_PERIOD [7:0]	R/W	FPHS Period - High Byte	5

0x0473 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	FPHS_PERIOD [7:0]	R/W	FPHS Period - Low Byte One pixel or panel clock per increment	3Ah

0x0474 – Panel Output Hsync Pulse Width [7:0] Register

Bit	Function	R/W	Description	Reset
7 - 0	FPHS_ACTIVE_PW	R/W	FPHS Active Pulse Width This register is usually filled in with the minimum FPHS pulse width requirement from the flat panel specification	10h

0x0475 – Panel Output Hsync Back Porch [7:0] Register

Bit	Function	R/W	Description	Reset
7 - 0	FP_H_BACK_ PORCH	R/W	Flat Panel Horizontal Back Porch Width One pixel or panel clock per increment This register is usually filled in with the minimum horizontal back porch requirement from the flat panel specification. When the reg_0489[6] is set to "0", this register has no effect on horizontal back porch; an internal circuitry calculates the horizontal back porch to center the active region; reading this register returns the calculated value. If the value returned is 0xFF, the actual value can be larger than 0xFF. Refer to reg_04C0 ~ reg_04C3 for reading the calculated values	1Bh

0x0476 ~ 0x0477 Panel Output Horizontal Active Width [10:0] Registers

0x0476 – High Byte Register

Bit	Function	R/W	Description	Reset
7 - 3	Reserved	-	Reserved	0
2 - 0	FPDE_ACTIVE [10:8]	R/W	FPDE Horizontal Active Length -high	4

0x0477 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	FPDE_ACTIVE [7:0]	R/W	FPDE Horizontal Active Length -low	0

0x0478 ~ 0x479 Panel Output Vsync Period [10:0] Register

0x0478 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 – 0	FPVS_PERIO D [10:8]	R/W	FPVS Period - high	3

0x0479 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	FPVS_PERIO D [7:0]	R/W	FPVS Period - low One FPHS period per increment	26h

0x047A – Panel Output Vsync Pulse Width [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	FPVS_ACTIVE _PW	R/W	FPVS Active Pulse Width One FPHS period per increment This register is usually filled in with the minimum FPVS pulse width requirement from the flat panel specification.	06

0x047B – Panel Output Vsync Back Porch [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	FP_V_BACK_ PORCH	R/W	Flat Panel Vertical Back Porch Width One FPHS period per increment	1Fh

0x047C ~ 0x047D Panel Output Vertical Active Length [10:0] Register

0x047C – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
7 – 0	FP_V_ACTIVE [10:8]	R/W	Flat Panel Vertical Active Length - high	3

0x047D – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	FP_V_ACTIVE [7:0]	R/W	Flat Panel Vertical Active Length - low	0

0x0480 ~ 0x0481 Horizontal Non Display Width [9:0] Registers

0x0480 – High Byte Register

Bit	Function	R/W	Description	Reset
7 - 2	Reserved	-	Reserved	-
1 - 0	H_NON_DISPLAY [9:8]	R/W	Horizontal non-display pixel number applied to both left and right sides - high	0

0x0481 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	H_NON_DISPLAY [7:0]	R/W	Horizontal non-display pixel number applied to both left and right sides - low	0

0x0482 ~ 0x0483 Horizontal Non Display Width II [9:0] Independent Left/Right Selection Registers

0x0482 – High Byte Register

Bit	Function	R/W	Description	Reset
7	THND2_EN	R/W	1 = Non-display left/right independent control enable. Use 0x0480[1:0] and 0x048 only for left side and use 0x0482[1:0] and 0x0483 for right side 0 = Use 0x0480[1:0] and 0x0481 for both left and right	0
6 - 2	Reserved	-	Reserved	0
1 - 0	RI_NON_DISPLAY [9:8]	R/W	Non display width for right side - high	0

0x0483 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	RI_NON_DISPLAY [7:0]	R/W	Non display width for right side - high	0

0x0484 – Top / Bottom Display Black Out Register

Bit	Function	R/W	Description	Reset
7 - 6	Reserved	-	Reserved	0
5 - 0	BLKTB	R/W	Number of lines to be black out from top and the bottom of the display.	0

0x0485 – Bottom Display Black Out Register

Bit	Function	R/W	Description	Reset
7	BLKTB2_EN	R/W	Enable independent top and bottom black out line numbers. The top black out line number is set by reg_0484[5:0] and the bottom black out line is set by reg_0485[5:0]	0
6	Reserved	-	Reserved	0
5 - 0	BLKTB2	R/W	Blcok Bottom	0

0x0486 – FPEN Delay Adjustment Register

Bit	Function	R/W	Description	Reset
7	INT_DE_NO_DELAY	-	Disable the delay specified by 0x0486[3:0]	0
6 - 4	Reserved	-	Reserved	0
3 - 0	INT_DE_DELAY	R/W	Delay Tuning for Flat Panel Output DE	0

0x0487 – FPHS Delay Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	0
3-0	FPHS_ OUTPUT_ DELAY	R/W	Adjust the panel FPHS output delay. A non zero value effectively moves the FPHS closer to the FPDE.	0

0x0488 – FPVS Delay Adjustment Register

Bit	Function	R/W	Description	Reset
7 - 4	Reserved	-	Reserved	0
3 - 0	DELAY_FPVS	R/W	Adjust FPVS position. A higher value moves the FPVS closer to the first active display line (the first active FPDE).	8

0x0489 – Panel Adjustment Selection Register

Bit	Function	R/W	Description	Reset
7	UTVB	R/W	Disable the alignment of the first input active line to the first display output line when reg_048B[7] is set to “1” 0: Always aligned 1: The display up/down movement can be adjusted by changing reg_048C, the FPVS pulse width, or back porch	0
6	UTHB	R/W	0 = Panel horizontal back porch value is from auto calculation 1 = Panel horizontal back porch value follows the reg_8075	0
5	DIST_HADJ	R/W	Enable distributed FPHS period minor adjustment Effective when USEREG (reg_807E_[0]) is “0” and reg_807E[6] is “1”	0
4	ENA_HADJ	R/W	Enable FPHS period minor adjustment No effect if USEREG, reg_807E_[0] is “1”	0
3 - 2	Reserved	-	Reserved	0
1	AUTOC	R/W	Enable auto calculation of initial counter value. When this bit is “1”, an internal circuitry calculates the initial value of horizontal pixel counter, which in turn generates FPHS. The calculation is based on either the internal generated FPHS period or the programmed FPHS period, determined by reg_0489[0]. If this bit is “0”, the initial value is taken from reg_0490[7:0] ~ reg_0493[7:0]	0
0	USEREG	R/W	FPHS period selection: 1: The contents programmed in index reg_0472 and index reg_0473 0: Internal circuit generated value	0

0x048A – Panel Adjustment Selection Register

Bit	Function	R/W	Description	Reset
7 – 6	Reserved	-	Reserved	0
5	EARLY_ST	R/W	Early start. Start to output data earlier in non auto calculation mode.	0
4	-	R/W	Reserved	0
3	AFRUN	R/W	Enable auto free run. If the input Vsync is lost, the free run mode is automatically invoked. (The reg 0x0B09 bit 0 must set to 1 to detect the Vsync loss)	0
2	FRERUN	R/W	Force into free run mode.	0
1	Reserved	-	Reserved	0
0	TCON_DE_CON	R/W	Enable internal DE to TCON module always generated 1: Enable 0: Disable	0

0x048B – Internal Panel Timing Adjustment Register

Bit	Function	R/W	Description	Reset
7	LINE_VSCL	R/W	Use FPVS period, reg_0478 reg_0479 to generate vertical scale factor. The result is read back from vertical scale factor registers, reg_0435reg_0436, and reg_0437. 1: Enable 0: Disable	0
6	FRM_ALIN	R/W	Frame alignment 1: Vsync 0: Non Vsync	0
5	FLD_ALIN	R/W	Non Vsync Frame alignment occurs at odd filed only or both fields 1: Odd field 0: Both fields	0
4	ALOW_QER	R/W	Sampling quantization error allowance 1: No 0: Yes	0
3 - 0	THRSH_VCHG	R/W	Threshold of one frame clock count to perform new frame alignment	4

0x048C – Internal Panel Timing Adjustment Register

Bit	Function	R/W	Description	Reset
7 - 0	LINEGONUM	R/W	This register is used when the LINE_VSCL (reg_048B[7]) is “1” and the UTVB (reg_0489[7]) is “0” to move the FPVS position. A larger value moves the FPVS earlier.	24h

0x048D – Panel Adjustment Selection Register

Bit	Function	R/W	Description	Reset
7 - 6	DISP_SNGFLD	R/W	Display single field on flat panel. 0,1 = Function disabled 2 = Display odd field 3 = Display even field	0
5	RVG_AC	R/W	When set the field signal is reversed in the auto calculation circuitry.	0
4	OLDTIME	R/W	When the auto calculation bit (reg_807E[1]) is turned off and this bit is set, the vsync generation falls back to the old way.	0
3 - 0	Reserved	-	Reserved	0
1 - 0	EVNDLY	R/W	Even field vertical back porch adjustment 0 = 0 1 = +1 2 = +2 3 = -1	0

0x0490 ~ 0x0491 Pixel Counter Initialization Value [12:0] Registers (Odd Field)

0x0490 – High Byte Register

Bit	Function	R/W	Description	Reset
7 - 5	Reserved	-	Reserved	0
4 - 0	INI_CNT_ODD [12:8]	R/W	Pixel counter initialization value --high	0

0x0491 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	INI_CNT_ODD [7:0]	R/W	Pixel counter initialization value – low This register comes into effect when the “AUTOC” reg_0489[1] is set to “0”. It provides the initial value of horizontal pixel counter for the odd field.	C0h

0x0492 ~ 0x0493 Pixel Counter Initialization Value [12:0] Registers (Even Field)

0x0492 – High Byte Register

Bit	Function	R/W	Description	Reset
7 - 5	Reserved	-	Reserved	0
4 - 0	INI_CNT_EVN [12:8]	R/W	Pixel counter initialization value --high	0

0x0493 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 - 0	INI_CNT_EVN [7:0]	R/W	Pixel counter initialization value – low This register comes into effect when the “AUTOC” reg_0489[1] is set to “0”. It provides the initial value of horizontal pixel counter for the even field.	C0h

0x0494 – Line Buffer Read Start Location [7:0] Register

Bit	Function	R/W	Description	Reset
7 - 0	TGT_POS	R/W	This register comes into effect when the “AUTOC”, reg_0489[1] is set to “1”. It is used to set the internal line buffer FIFO read start time. A smaller value makes the read start later. Use only even number as percentage of one FPHS period.	C0h

0x04C0 ~ 0x04C3 Internal Counter Read Out Registers

Bit	Function	R/W	Description	Reset
7 - 0	COUNTER_READ_BYTE_3, _2,_1, _0	R	These four index addresses provide real time data read out of some internal counters. The index of these counters is set by reg_04C6[7:4].	-

Index	0x04C0	0x04C1	0x04C2	0x04C3
0	-	LVPCNT_ODD[23:16]	LVPCNT_ODD[15:8]	LVPCNT_ODD[7:0]
1	-	LVPCNT_EVN[23:16]	LVPCNT_EVN[15:8]	LVPCNT_EVN[7:0]
2	LIVCNT_EVN[15:8]	LIVCNT_EVN[7:0]	LIVCNT_ODD[11:8]	LIVCNT_ODD[7:0]
3	HCNT_ODDI[15:8]	HCNT_ODDI[7:0]	LHCNT_ODDI[11:8]	LHCNT_ODDI[7:0]
4	LBOVFC[10:8]	LBOVFC[7:0]	LHPCNT[13:8]	LHPCNT[7:0]
5	FPGO_EVN_H[12:8]	FPGO_EVN_H[7:0]	FPGO_ODD_H[12:8]	FPGO_ODD_H[7:0]
6	FPGO_EVN_V[10:8]	FPGO_EVN_V[7:0]	FPGO_ODD_V[10:8]	FPGO_ODD_V[7:0]
7	tvbm[10:8]	tvbm[7:0]	thbm[10:8]	thbm[7:0]
8	FPVPOS_EVN[11:8]	FPVPOS_EVN[7:0]	FPVPOS_ODD[11:8]	FPVPOS_ODD[7:0]

0x04C4 – Simulation Initialization Register

Bit	Function	R/W	Description	Reset
7 - 4	PCCINIA_INDEX	R/W	Index for simulation initialization of internal auto calculation counters. 0: VPCNT[23:0] Pixel counter for 1 VSYNC period 1: LVPCNT_ODD[23:0] Pixel counter for 1 Odd field VSYNC period 2: LVPCNT_EVN[23:0] Pixel counter for 1 Even field VSYNC period 3: IVCNT[11:0] Line counter for 1 VSYNC period 4: LIVCNT_ODD[11:0] Line counter for 1 Odd field VSYNC period 5: LIVCNT_EVN[11:0] Line counter for 1 Even field VSYNC period	0
3	FRC_2F	R/W	For internal use only	0
2	FRC_1F	R/W	For internal use only	0
1 - 0	PCCINIA_SUB_INDX	R/W	Sub index for the above counters, providing byte wide data read/write from/to 0x0C1. 0 = Bits [7:0] of the counter pointed by the index 1 = Bits [15:8] of the counter pointed by the index 2 = Bits [23:16] of the counter pointed by the index	0

0x04C5 – Simulation Initialization Data Port Register

Bit	Function	R/W	Description	Reset
7 - 0	PCCINID	R/W	Data port for the counters listed in 0x04C4	0

0x04C6 – Data Read Selection Register

Bit	Function	R/W	Description	Reset
7-4	RD_INDX	R/W	Index for selecting which data to read from 0x04C0 ~ 0x04C3	0
3-0	-	R/W	Reserved	0

LCDC – Image Adjustment

0x0500 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	-
5-0	HUE	R/W	Hue Adjustment for Main path. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	20

0x0501 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_R	R/W	Red Contrast Adjustment for Main path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0502 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_G	R/W	Green Contrast Adjustment for Main path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0503 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_B	R/W	Blue Contrast Adjustment for Main path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0504 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Y	R/W	Y Contrast Adjustment for Main path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0505 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cb	R/W	Cb Contrast Adjustment for Main path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0506 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cr	R/W	Cr Contrast Adjustment for Main path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0507 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_R	R/W	Red Brightness Adjustment for Main path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x0508 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_G	R/W	Green Brightness Adjustment for Main path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x0509 – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_B	R/W	Blue Brightness Adjustment for Main path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x050A – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_Y	R/W	Y Brightness Adjustment for Main path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x050B – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	H_SHARP_COR	R/W	Coring function for sharpness control of Main path.	3
3-0	H_SHARPNESS	R/W	Sharpness Adjustment for Main path	0

0x050C – Main Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	H_SHARP_FREQ	R/W	Main path Sharpness frequency select 0 = Low freq 1 = High freq	0
6	Reserved	-	Reserved	-
5-4	DYNR	R/W	Main path YNR	0
3	Reserved	-	Reserved	-
2-0	HFLT	R/W	Main path Hflt.	0

0x0510 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	-
5-0	HUE	R/W	Hue Adjustment for PIP1 path. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	20

0x0511 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_R	R/W	Red Contrast Adjustment for PIP1 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0512 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_G	R/W	Green Contrast Adjustment for PIP1 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0513 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_B	R/W	Blue Contrast Adjustment for PIP1 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0514 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Y	R/W	Y Contrast Adjustment for PIP1 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0515 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cb	R/W	Cb Contrast Adjustment for PIP1 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0516 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cr	R/W	Cr Contrast Adjustment for PIP1 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0517 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_R	R/W	Red Brightness Adjustment for PIP1 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x0518 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_G	R/W	Green Brightness Adjustment for PIP1 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x0519 – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_B	R/W	Blue Brightness Adjustment for PIP1 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x051A – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_Y	R/W	Y Brightness Adjustment for PIP1 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x051B – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	H_SHARP_COR	R/W	Coring function for sharpness control of PIP1 path.	3
3-0	H_SHARPNESS	R/W	Sharpness Adjustment for PIP1 path	0

0x051C – PIP1 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	H_SHARP_FREQ	R/W	PIP1 path Sharpness frequency select 0 = Low freq 1 = High freq	0
6	Reserved	-	Reserved	-
5-4	DYNR	R/W	PIP1 path YNR	0
3	Reserved	-	Reserved	-
2-0	HFLT	R/W	PIP1 path Hflt.	0

0x0520 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	-
5-0	HUE	R/W	Hue Adjustment for PIP2 path. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	20

0x0521 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_R	R/W	Red Contrast Adjustment for PIP2 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0522 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_G	R/W	Green Contrast Adjustment for PIP2 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0523 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_B	R/W	Blue Contrast Adjustment for PIP2 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0524 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Y	R/W	Y Contrast Adjustment for PIP2 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0525 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cb	R/W	Cb Contrast Adjustment for PIP2 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0526 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CONTRAST_Cr	R/W	Cr Contrast Adjustment for PIP2 path 80h+ = Higher contrast 80h = Neutral 80h- = Lower contrast	80

0x0527 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_R	R/W	Red Brightness Adjustment for PIP2 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x0528 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_G	R/W	Green Brightness Adjustment for PIP2 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x0529 – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_B	R/W	Blue Brightness Adjustment for PIP2 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x052A – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BRIGHTNESS_Y	R/W	Y Brightness Adjustment for PIP2 path 80h+ = Higher brightness 80h = Neutral 80h- = Lower brightness	80

0x052B – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	H_SHARP_COR	R/W	Coring function for sharpness control of PIP2 path.	3
3-0	H_SHARPNESS	R/W	Sharpness Adjustment for PIP2 path	0

0x052C – PIP2 Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	H_SHARP_FREQ	R/W	PIP2 path Sharpness frequency select 0 = Low freq 1 = High freq	0
6	Reserved	-	Reserved	-
5-4	DYNR	R/W	PIP2 path YNR	0
3	Reserved	-	Reserved	-
2-0	HFLT	R/W	PIP2 path Hflt.	0

0x0530 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	T_BW	R/W	Test BW. Should be 0 for normal operation	0
6	Reserved	-	Reserved	-
5	PEDLVL	R/W	Black level selection. 0 = 0 1 = 16d	0
4	WHTLVL	R/W	White level selection. 0 = 235d 1 = 255d	1
3-1	Reserved	-	Reserved	-
0	BW_EN	R/W	0 = BW disable 1 = BW stretch enable	0

0x0531 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_LINE_ST_LO	R/W	Black/White stretch line start for detection window, lower 8 bits (total 10 bits).	08

0x0532 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_LINE_END_LO	R/W	Black/White stretch line end for detection window, lower 8 bits (total 10 bits).	F6

0x0533 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved.	0
3-2	BW_LINE_END_HI	R/W	Black/White stretch line end for detection window, upper 2 bits.	2
1-0	BW_LINE_ST_HI	R/W	Black/White stretch line startfor detection window, upper 2 bits.	0

0x0534 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_H_DELAY	R/W	BWHDLY, Black/White stretc horizontal distance from Start/End pixel of HACTIVE.	10

0x0535 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	-
5-0	BW_H_FILTER_GAIN	R/W	Y Min/Max Horizontal filter gain.	0D

0x0536 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_BLACK_TILT	R/W	Tilt point for black stretch.	67

0x0537 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_WHITE_TILT	R/W	Tilt point for white stretch.	94

0x0538 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_BLACK_ LIMIT	R/W	Black stretch Limit	2A

0x0539 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	BW_WHITE_ LIMIT	R/W	White stretch Limit	D0

0x053A – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-0	BW_GAIN	R/W	Black/White Stretch Field recursive filter gain.	02

0x0550 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CE_CENTER0	R/W	Color Enhancement Center Color phase for color 1. The range for center color phase is –180° ~ + 180°, 2 degree per step. Color Enhancement Center is 2's complement form, default degree of CENTER 0 is 122°	3D

0x0551 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CE_CENTER1	R/W	Color Enhancement Center Color phase for color 2. The range for center color phase is –180° ~ + 180°, 2 degree per step. Color Enhancement Center is 2's complement form, default degree of CENTER 1 is –122°	C3

0x0552 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7-0	CE_CENTER2	R/W	Color Enhancement Center Color phase for color31. The range for center color phase is –180° ~ + 180°, 2 degree per step. Color Enhancement Center is 2's complement form, default degree of CENTER 2 is –8°	FC

0x0553 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	CE_EN	R/W	1= Color Enhancement Enable 0 = Disable	0
6-5	CE_SPREAD0	R/W	Color Enhancement Gain Spread Range for color 1 0 = no enhance 1 = -8° ~ +8° of center color phase 2 = -16° ~ +16° of center color phase 3 = -32° ~ + 32° of center color phase	0
4-0	CE_GAIN0	R/W	Color Enhancement Gain for color 1. The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0

0x0554 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-5	CE_SPREAD1	R/W	Color Enhancement Gain Spread Range for color 2 0 = no enhance 1 = -8° ~ +8° of center color phase 2 = -16° ~ +16° of center color phase 3 = -32° ~ + 32° of center color phase	0
4-0	CE_GAIN1	R/W	Color Enhancement Gain for color 2. The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0

0x0555 – Image Adjustment Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-5	CE_SPREAD2	R/W	Color Enhancement Gain Spread Range for color 3 0 = no enhance 1 = -8° ~ +8° of center color phase 2 = -16° ~ +16° of center color phase 3 = -32° ~ + 32° of center color phase	0
4-0	CE_GAIN2	R/W	Color Enhancement Gain for color 3. The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0

0x0570 – Test Pattern Generator Register

Bit	Function	R/W	Description	Reset
7	TPG_EN	R/W	Test pattern generator enable, 0: Normal (DTV input)	0
6-4	TPG_CSWAP	R/W	Color swap for test pattern generator 0: RGB (default) 1: GBR 2: BRG 3: RBG 4: GRB 5: BGR 6, 7: (same as 0)	0
3-0	PAT_SEL	R/W	Pattern selection. 0: Hue map 1: Hue map (fine) 2: Gray horizontal 17 steps 3: Gray vertical 17 steps 4: Gray H/V 17x17 steps 5: White rectangle 6: Vertical 1-dot stripe 7: Horizontal 1-dot stripe 8: Black/White checker board 9: RGB checker board A: Gray horizontal 17 steps + horizontal black stripes B: Mitsubishi WQVGA test pattern C: Flat 100% blue D: Ramp E, F: Flat 50% gray	0

LCDC – PIP1 Control

0x0600 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W		-
1-0	PIPGW_XST[9:8]	R/W	Horizontal input cropping start[9:8]. These bits indicate the start point of the cropping window of the PIP data which is going to be written into memory.	0

0x0601 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPGW_XST[7:0]	R/W	Horizontal input cropping start[7:0]. These bits indicate the start point of the cropping window of the PIP data which is going to be written into memory.	00

0x0602 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIPGW_WIDTH[10:8]	R/W	Horizontal input cropping window width[10:8]. These bits indicate the width of the cropping window of the PIP data which is going to be written into memory.	2

0x0603 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPGW_WIDTH[7:0]	R/W	Horizontal input cropping window width[7:0]. These bits indicate the width of the cropping window of the PIP data which is going to be written into memory.	D0

0x0604 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-1	Reserved	R/W		-
0	PIPGW_YST[8]	R/W	Vertical input cropping start[8].	0

0x0605 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPGW_YST[7:0]	R/W	Vertical input cropping start[7:0]. These bits indicate the start point of the cropping window of the PIP data which is going to be written into memory.	02

0x0606 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Vertical input cropping start[8].	0
2-0	PIPGW_HEIGHT[10:8]	R/W	Vertical input cropping window height[10:8].	0

0x0607 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPGW_HEIGHT[7:0]	R/W	Vertical input cropping window height[7:0]. These bits indicate the height of the cropping window of the PIP data which is going to be written into memory.	E0

0x0608 – PIP Control Register

Bit	Function	R/W	Description	Reset
7	PPFIL_MAN	R/W	1 = Down scaler pre-filter manual selection enable. 0 = Auto selection (default)	0
6	CKINV	R/W	1 = PIP input clock inverse 0 = Normal.	0
5-4	PPFIL_SEL	R/W	Down scaler pre-filter manual selection. 0 = No filter 1 = Weak filter 2 = Strong filter 3 = Medium filter	0
3-2	PIPEFDOFF	R/W	Even field offset for the cropping window.	0
1-0	PIPOFDOFF	R/W	Odd field offset for the cropping window.	0

0x0609 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIPDNSXFAC[11:8]	R/W	PIP horizontal down scaling ratio [11:8].	1

0x060A – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPDNSXFAC[7:0]	R/W	PIP horizontal down scaling ratio [7:0]. 100h for no down scaling.	00

0x060B – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIPDNSYFAC[11:8]	R/W	PIP vertical down scaling ratio [11:8].	1

0x060C – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPDNSYFAC[7:0]	R/W	PIP vertical down scaling ratio [7:0]. 100h for no down scaling	00

0x060D – PIP Control Register

Bit	Function	R/W	Description	Reset
7	PDOF_EN1	R/W	1 = PIP1 down scaler offset enable (Interlace input), 0 = offset disabled (Progressive input)	0
6-0	PIP_DN_OFF1	R/W	PIP1 down scaler offset (40h = half line offset)	00

0x060E – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_WR_ BASE[23:16]	R/W	PIP window write buffer base address. It defines start address of PIP memory area.	00

0x060F – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_WR_ BASE[15:8]	R/W	PIP window write buffer base address. It defines start address of PIP memory area.	00

0x0610 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_WR_ BASE[7:0]	R/W	PIP window write buffer base address. It defines start address of PIP memory area.	00

0x0611 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIP_WR_WID TH[10:8]	R/W	PIP window write width[10:8]. These bits indicate the width of the PIP window written into the memory. Maximum width is 400h.	2

0x0612 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_WR_WID TH[7:0]	R/W	PIP window write width[7:0]. These bits indicate the width of the PIP window written into the memory.	D0

0x0613 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W		-
1-0	HEIGHT[9:8]	R/W	PIP window write height[9:8].	0

0x0614 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_WR_HEIG HT[7:0]	R/W	PIP window write height[7:0]. These bits indicate the height of the PIP window written into the memory.	E0

0x0615 – PIP Control Register

Bit	Function	R/W	Description	Reset
7	PIPWREN	R/W	1 = PIP window write enable. When disabled read-out image will freeze.	0
6	WCPH	R/W	Write Data Color Phase control.	1
5	MUTE_C	R/W	PIP1 mute color selection 1 = Blue 0 = Black, Only active when 0x2BD[0] = 1	0
4-1	Reserved	R/W		-
0	PRCPH	R/W	Read Data Color Phase control	0

0x0616 – PIP Control Register

Bit	Function	R/W	Description	Reset
7	PRDEN	R/W	1 = PIP window read enable	0
6	FRM_MD	R/W	1 = PIP frame based buffer control (drop/duplicate frame) 0 = Field based (Default)	0
5	PIPEN	R/W	PIP mode enable.	0
4	SNGL_FD	R/W	1 = PIP blending single field mode 0 = Normal	0
3	RDFDPOL	R/W	PIP read buffer field polarity	0
2	PXDB	R/W	1 = Pixel doubling when up scaling 0 = Normal.	0
1	LNDB	R/W	1 = Line doubling when up scaling 0 = Normal	0
0	MUTE_EN	R/W	1 = PIP1 image mute 0 = Normal. Mute color defined by 0x2BC[5]	0

0x0617 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PUPSXFAC[11:8]	R/W	PIP horizontal Up scaling ratio [11:8].	8

0x0618 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PUPSXFAC[7:0]	R/W	PIP horizontal Up scaling ratio [7:0]. 800h for no up scaling.	00

0x0619 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PUPSYFAC[11:8]	R/W	PIP vertical Up scaling ratio [11:8].	8

0x061A – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PUPSYFAC[7:0]	R/W	PIP vertical Up scaling ratio [7:0]. 800h for no up scaling.	00

0x061B – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	UPSFDOFF	R/W	PIP1 vertical upscale field offset. Only work with interlaced input.	80

0x061C – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIPWBASEX [11:8]	R/W	PIP Window position base x start[11:8]. These bits indicate the origin of the PIP Window.	0

0x061D – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPWBASEX[7:0]	R/W	PIP Window position base x start[7:0]. These bits indicate the origin of the PIP Window.	00

0x061E – PIP Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIPWBASEY [10:8]	R/W	PIP Window position base y start[10:8]. These bits indicate the origin of the PIP Window.	0

0x061F – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPWBASEY[7:0]	R/W	PIP Window position base y start[7:0]. These bits indicate the origin of the PIP Window.	00

0x0620 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	PIPWYOFF	R/W	PIP Window position base y start offset. These bits indicate the base position of the PIP Window.	3
3-0	PIPWXOFF	R/W	PIP Window position base x start offset. These bits indicate the base position of the PIP Window.	C

0x0621 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIPWWIDTH[11:8]	R/W	PIP Window width[11:8]. These bits indicate the display width of the PIP Window.	2

0x0622 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPWWIDTH[7:0]	R/W	PIP Window width[7:0]. These bits indicate the display width of the PIP Window.	D0

0x0623 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIPWHEIGHT[10:8]	R/W	PIP Window height[10:8]. These bits indicate the display height of the PIP Window.	0

0x0624 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIPWHEIGHT[7:0]	R/W	PIP Window height[7:0]. These bits indicate the display height of the PIP Window.	E0

0x0625 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_H_POS_ADJ	R/W	PIP horizontal position offset adjustment	F4

0x0626 – PIP Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_V_POS_ADJ	R/W	PIP vertical position offset adjustment	FC

LCDC – PIP2 Control

0x0630 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W		-
1-0	PIP2GW_XST[9:8]	R/W	Horizontal input cropping start[9:8]. These bits indicate the start point of the cropping window of the PIP2 data which is going to be written into memory.	0

0x0631 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2GW_XST[7:0]	R/W	Horizontal input cropping start[7:0]. These bits indicate the start point of the cropping window of the PIP2 data which is going to be written into memory.	00

0x0632 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIP2GW_WIDTH[10:8]	R/W	Horizontal input cropping window width[10:8]. These bits indicate the width of the cropping window of the PIP2 data which is going to be written into memory.	2

0x0633 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2GW_WIDTH[7:0]	R/W	Horizontal input cropping window width[7:0]. These bits indicate the width of the cropping window of the PIP2 data which is going to be written into memory.	D0

0x0634 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-1	Reserved	R/W		-
0	PIP2GW_YST[8]	R/W	Vertical input cropping start[8].	0

0x0635 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2GW_YST[7:0]	R/W	Vertical input cropping start[7:0]. These bits indicate the start point of the cropping window of the PIP2 data which is going to be written into memory.	02

0x0636 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Vertical input cropping start[8].	0
2-0	PIP2GW_HEIGHT[10:8]	R/W	Vertical input cropping window height[10:8].	0

0x0637 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2GW_HEIGHT[7:0]	R/W	Vertical input cropping window height[7:0]. These bits indicate the height of the cropping window of the PIP2 data which is going to be written into memory.	E0

0x0638 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7	PPFIL_MAN	R/W	1 = Down scaler pre-filter manual selection enable. 0 = Auto selection (default)	0
6	CKINV	R/W	1 = PIP2 input clock inverse 0 = Normal.	0
5-4	PPFIL_SEL	R/W	Down scaler pre-filter manual selection. 0 = No filter 1 = Weak filter 2 = Strong filter 3 = Medium filter	0
3-2	PIP2EFDOFF	R/W	Even field offset for the cropping window.	0
1-0	PIP2OFDOFF	R/W	Odd field offset for the cropping window.	0

0x0639 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIP2DNSXFAC[11:8]	R/W	PIP2 horizontal down scaling ratio [11:8].	1

0x063A – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2DNSXFAC[7:0]	R/W	PIP2 horizontal down scaling ratio [7:0]. 100h for no down scaling.	00

0x063B – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIP2DNSYFAC[11:8]	R/W	PIP2 vertical down scaling ratio [11:8].	1

0x063C – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2DNSYFAC[7:0]	R/W	PIP2 vertical down scaling ratio [7:0]. 100h for no down scaling	00

0x063D – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7	PDOF_EN2	R/W	1 = PIP2 down scaler offset enable (Interlace input), 0 = offset disabled (Progressive input)	0
6-0	PIP2_DN_OFF2	R/W	PIP2 down scaler offset (40h = half line offset)	00

0x063E – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_WR_ BASE[23:16]	R/W	PIP2 window write buffer base address. It defines start address of PIP2 memory area.	00

0x063F – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_WR_ BASE[15:8]	R/W	PIP2 window write buffer base address. It defines start address of PIP2 memory area.	00

0x0640 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_WR_ BASE[7:0]	R/W	PIP2 window write buffer base address. It defines start address of PIP2 memory area.	00

0x0641 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIP2_WR_WIDTH[10:8]	R/W	PIP2 window write width[10:8]. These bits indicate the width of the PIP2 window written into the memory. Maximum width is 400h.	2

0x0642 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_WR_WIDTH[7:0]	R/W	PIP2 window write width[7:0]. These bits indicate the width of the PIP2 window written into the memory.	D0

0x0643 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W		-
1-0	HEIGHT[9:8]	R/W	PIP2 window write height[9:8].	0

0x0644 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_WR_HEIGHT[7:0]	R/W	PIP2 window write height[7:0]. These bits indicate the height of the PIP2 window written into the memory.	E0

0x0645 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7	PIP2WREN	R/W	1 = PIP2 window write enable. When disabled read-out image will freeze.	0
6	WCPH	R/W	Write Data Color Phase control.	1
5	MUTE_C	R/W	PIP2 mute color selection 1 = Blue 0 = Black, Only active when 0x2BD[0] = 1	0
4-1	Reserved	R/W		-
0	PRCPH	R/W	Read Data Color Phase control	0

0x0646 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7	PRDEN	R/W	1 = PIP2 window read enable	0
6	FRM_MD	R/W	1 = PIP2 frame based buffer control (drop/duplicate frame) 0 = Field based (Default)	0
5	PIP2EN	R/W	PIP2 mode enable.	0
4	SNGL_FD	R/W	1 = PIP2 blending single field mode 0 = Normal	0
3	RDFDPOL	R/W	PIP2 read buffer field polarity	0
2	PXDB	R/W	1 = Pixel doubling when up scaling 0 = Normal.	0
1	LNDB	R/W	1 = Line doubling when up scaling 0 = Normal	0
0	MUTE_EN	R/W	1 = PIP2 image mute 0 = Normal. Mute color defined by 0x2BC[5]	0

0x0647 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PUPSXFAC[11:8]	R/W	PIP2 horizontal Up scaling ratio [11:8].	8

0x0648 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PUPSXFAC[7:0]	R/W	PIP2 horizontal Up scaling ratio [7:0]. 800h for no up scaling.	00

0x0649 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PUPSYFAC[11:8]	R/W	PIP2 vertical Up scaling ratio [11:8].	8

0x064A – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PUPSYFAC[7:0]	R/W	PIP2 vertical Up scaling ratio [7:0]. 800h for no up scaling.	00

0x064B – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	UPSFDOFF	R/W	PIP2 vertical upscale field offset. Only work with interlaced input.	80

0x064C – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIP2WBASEX [11:8]	R/W	PIP2 Window position base x start[11:8]. These bits indicate the origin of the PIP2 Window.	0

0x064D – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2WBASEX[7:0]	R/W	PIP2 Window position base x start[7:0]. These bits indicate the origin of the PIP2 Window.	00

0x064E – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIP2WBASEY [10:8]	R/W	PIP2 Window position base y start[10:8]. These bits indicate the origin of the PIP2 Window.	0

0x064F – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2WBASEY[7:0]	R/W	PIP2 Window position base y start[7:0]. These bits indicate the origin of the PIP2 Window.	00

0x0650 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	PIP2WYOFF	R/W	PIP2 Window position base y start offset. These bits indicate the base position of the PIP2 Window.	3
3-0	PIP2WXOFF	R/W	PIP2 Window position base x start offset. These bits indicate the base position of the PIP2 Window.	C

0x0651 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W		-
3-0	PIP2WWIDTH[11:8]	R/W	PIP2 Window width[11:8]. These bits indicate the display width of the PIP2 Window.	2

0x0652 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2WWIDTH[7:0]	R/W	PIP2 Window width[7:0]. These bits indicate the display width of the PIP2 Window.	D0

0x0653 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2-0	PIP2WHEIGHT[10:8]	R/W	PIP2 Window height[10:8]. These bits indicate the display height of the PIP2 Window.	0

0x0654 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2WHEIGHT[7:0]	R/W	PIP2 Window height[7:0]. These bits indicate the display height of the PIP2 Window.	E0

0x0655 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_H_POS_ADJ	R/W	PIP2 horizontal position offset adjustment	F4

0x0656 – PIP2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP2_V_POS_ADJ	R/W	PIP2 vertical position offset adjustment	FC

LCDC – PIP1/PIP2 Common Control

0x0660 – PIP1/2 Control Register

Bit	Function	R/W	Description	Reset
7	PIP2_MRR	R/W	1: PIP2 image mirroring, 0: Normal	0
6-4	PIP_BORDER H[2:0]	R/W	PIP1/PIP2 vertical border width [2:0] (0 line – 7 lines)	0
3	PIP1_MRR	R/W	1: PIP1 image mirroring, 0: Normal	0
2-0	PIP_BORDER W[2:0]	R/W	PIP1/PIP2 horizontal border width (0 dot – 7 dots)	0

0x0661 – PIP1/2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_FRMCOL OR1	R/W	PIP1/PIP2 standard window frame color	1C

0x0662 – PIP1/2 Control Register

Bit	Function	R/W	Description	Reset
7-0	PIP_FRMCOL OR1	R/W	PIP1/PIP2 standard window frame color	1C

0x0663 – Reserved

Bit	Function	R/W	Description	Reset
7	PIP_RSTN	R/W	PIP local software reset (Auto return to 0)	0
6-0	Reserved	R/W	Reserved	00

LCDC – DV, PIP1/PIP2 Common Control

0x0670 – Dual View Control Register (Only for internal and special customer)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W		0
6	DV_REVERSE	R/W	1: Left/Right image swap, 0: Normal	0
5	Reserved	R/W		0
4	DV_CHECKER	R/W	1: Checker DV pattern, 0: Stripe barrier DV pattern	0
3-2	LR_SAME	R/W	0X: L/R show different image, 01: L/R both show PIP image, 10: L/R both show Main image	00
1	Reserved	R/W		0
0	DV_EN	R/W	1: Dual View enable, 0: disable	0

0x0671 – PIP1/2 Control Register

Bit	Function	R/W	Description	Reset
7	DTVDE1	R/W	1 = DTV1 input DE is ignored for both PIP1 and PIP2 0 = DE is used	1
6	DTVDE2	R/W	1= DTV2 input DE is ignored for both PIP1 and PIP2 0 = DE is used	1
5	DVLDEN3	R/W	1: Ignore decoder cken	0
4	Reserved	-	Reserved	-
3-2	PIP_INMX_SEL	R/W	PIP1 input selection. 0 = Decoder 1 = Analog RGB/YUV 2 = DTV1 3 = DTV2	0
1-0	PIP2_INMX_SEL	R/W	PIP2 input selection. 0 = Decoder 1 = Analog RGB/YUV 2 = DTV1 3 = DTV2	0

0x0672 – PIP1/2, Blending Control Register

Bit	Function	R/W	Description	Reset
7-6	PIPMX_IPSEL	R/W	PIP mixing mode. 0 = PIP2 over PIP1 alpha blended with Main (PIP1 is the main image and PIP2 is the sub window) 1 = PIP1 over PIP2 alpha blended with Main (PIP2 is the main image and PIP1 is the sub windiw) 2 = PIP2 over Main alpha blended with PIP1 (Main is the main image and PIP2 is the sub window) 3 = PIP1 over Main alpha blended with PIP2 (Main is the main image and PIP1 is the sub window)	3
5	PIPMX1_EN	R/W	1 = Primary path sub window enable (default) 0 = Primary path sub window disable This apply for normal panel or either one side of image of Dual View panel image. This register has priority over 0x0616[5], 0x0646[5] registers	1
4	PIPMX2_EN	R/W	1 = Secondary path sub window enable (default), 0 = Secondary path sub window disable. This bit has priority than alpha blending selection in bit 3. This apply for either one side of Dual View panel image.	1
3	ALPMX_EN	R/W	1 = Secondary path alpha blending enable 0 = Secondary path alpha blending disable (default) This apply for either one side of Dual View panel image.	0
2	2ND_PIP	R/W	1 = PIP2 border on	0
1	PIP2_WR_PWDN	R/W	1 = PIP2 write power down (image will freeze) 0 = Normal	0
0	PIP_WR_PWDN	R/W	1 = PIP1 write power down (image will freeze) 0 = Normal	0

0x0673 – Dual View Control Register (Only for internal and special customer)

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W		-
2	V_TOGGLE	R/W	1: Inversion polarity alternate every field, 0: Inversion polarity stay the same for every field	0
1	H_PHASE	R/W	1: 2-dot inversion start with same polarity for first 2 pixels, 0: 2-dot inversion polarity changes between first and second pixel (default)	0
0	TPO_MODE	R/W	1: 2-dot + Line inversion operation for TPO panel, 0: Normal	0

LCDC – PIP Alpha Blending Control

0x0680 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7	BLEND_EN	R/W	1 = PIP alpha blending enable 0 = Disable	0
6	MODE565	R/W	1 = 565 mode (4:4:4 color space) for PIP 0 = 888 mode (4:2:2 color space) Default	0
5	KEY_REV	R/W	1 = PIP alpha blending key detection reverse 0 = Normal	0
4-0	ALPHA1	R/W	Alpha1 of PIP alpha blending (Main/Sub mixing ratio), 2 = Full PIP – 0 = Full Main	10

0x0681 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7	KEYDISP	R/W	1 = PIP overlay key color position display for Test.	0
6-5	Reserved	-	Reserved	-
4-0	ALPHA2	R/W	Alpha2 of PIP alpha blending (Main dimming) 2 = Full Main – 0 = Black	10

0x0682 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7-0	RKEY	R/W	Red key color level for PIP alpha blending	00

0x0683 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7-0	GKEY	R/W	Green key color level for PIP alpha blending	00

0x0684 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7-0	BKEY	R/W	Blue key color level for PIP alpha blending	00

0x0685 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7-0	RRANGE	R/W	Key color range for Red	00

0x0686 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7-0	GRANGE	R/W	Key color range for Green	00

0x0687 – PIP Alpha Blending Register

Bit	Function	R/W	Description	Reset
7-0	BRANGE	R/W	Key color range for Blue	00

LCDC – OSD

0x0700 – 0SG Control Register

Bit	Function	R/W	Description	Reset
7 – 6	OSGMODE	R/W	OSG write operation mode 00: MCU/DMA write operation 01: Block transfer (no bit expansion, 0x0700[1:0] should be "00") 10: Block Fill (no bit expansion, 0x0700[1:0] should be "00") 11: Block transfer with source linear addressing	00
5 – 4	MSKSEL	R/W	Bitblt function select 00: Selective overwrite 01: Mask from source word 10: Mask from Bitblt mask register 11: No Bitblt function (unprocessed source pixel is written to destination location)	00
3	COLOR_CON	R/W	Enable color conversion When this bit is set and the source pixel value matches the value specified by the Color Conversion Source Color register (0x0740 ~ 0x0747), the pixel is converted to the corresponding Color Conversion Target Color register value (0x0748 ~ 0x074F)	0
2	BPP	R/W	Pixel unit selection 0: 2 bytes per pixel (16 bit) 1: 1 byte per pixel (8bit)	0
1 - 0	BEXPM	R/W	Bit expansion selection. When expanding to 8 bit (1 byte per pixel), the "8 Bit Expansion Table" is used. When expanding to 16 bit (2 bytes per pixel), the "16 Bit Expansion Table" is used. To invoke the Special 8 to 16 bit expansion, the 0x0703[4] needs to be set to "1" 00: No bit expansion 01: Expand 1 bit to 8/16 bit 10: Expand 2 bit to 8/16 bit 11: Expand 4 bit to 8/16 bit, or special 8 to16 bit	000

0x0701 – OSG Control Register

Bit	Function	R/W	Description	Reset
7	OSG_STUS		OSG operation status: a "1" indicates the operation is busy and a "0" means the operation is done.	0
6	FIFO_STUS		When OSDMODE=00 (MCU/DMA write), this bit indicates the FIFO full status. A "1" means FIFO is full and cannot accept new data. If the OSDMODE is not "00", this bit is always "0" but the FIFO is not accessible.	0
5 - 2			Reserved	0
1	MCUWD	R/W	MCU data write done. This bit is used for MCU write operation (OSDMODE=2'b00 and 0x0703[6]=0) only. Normally, if the amount of data is enough to cover the transfer destination region, defined by Transfer Horizontal Length (0x0768, 0x0769) and Transfer Vertical Length (ox76A,0x076B), the OSG busy status bit , 0x0701[7], will be de-asserted after the transfer is done. There is no need to set this bit. If the amount of data is not enough, one can write this bit to "1" after the MCU has written all the data. Once this bit is set, additional data will be padded until the transfer destination region is fully filled. The OSG busy status will be de-asserted afterwards.	0
0	OP_START	R/W	Write "1" to start OSG operation; and "0" to stop the operation. Operation sequence for Block Fill and Block Transfer: After setting all the other registers, write a "1" to start operation, then read back bit [7] to check the status. If the status returns "0", write a "0" to finish the operation. If without writing a "0", the subsequent write "1" has no effect. Operation sequence for MC/DMA write: Similar to Block Fill and Block Transfer except that after writing a "1" to this bit the operation does not start until 64 bytes data is written to the Data Port for MCU/DMA Write (0x0702). If more data are required, continue to write to the Data Port with additional 64 bytes chunks. When all writes are done and the bit [7] status returns "0", write a "0" to end the operation.	0

0x0702 – Data Port for MCU Write Register

Bit	Function	R/W	Description	Reset
7 – 0	-	W	Data port	-

0x0703 – OSD/OSG Control Register

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved	0
6	OSD_HW	R/W	Enable OSD hardware handshake with internal MCU. Set this bit to 1, when the SPI DMA is used to source the write data. 1: Enable 0: Disable	0
5 - 4	-	R/W	Reserved	-
4	SP8TO16	R/W	Special OSG 8 bit expansion to 16 bit operation. . The special operation mode requires setting this bit to “1”, the 0x0700[2:0] = 3’b011, and the 0x0703[3:1] a valid RGB format code. In the Special 8 to 16 bit expansion, the Entry 0 in the 16 Bit Expansion Table is always used as the expanded source pixel which is blended with the target pixel. The (alpha) blending value comes from the content of the original 8 bit source. The lower the alpha value, the less the expanded source pixel is shown. In this special 8 to 16 bit expansion mode, the color conversion, bitblt, and the selective over write functions are disabled.	0
3 - 1	OSG16FORM	--	Format selection for destination 16 bit type during the special OSG 8 bit to 16 bit operation 001: RGB565 (R 5, G 6, B 5) Data[15:0] = {R[4:0],G[5:4],G[3:0],B[4:0]} 010: RGB4444 (alpha 4, R 4, G 4, B 4) Data[15:0] = {A[3:0],R[3:0],G[3:0],B[3:0]} 011: RGB1555 (blink 1, R 5, G 5, B 5) Data[15:0] = {BL, R[4:0],G[4:0],B[4:0]}	0
0	OSDSRST	R/W	Soft reset for OSD section	0

0x0704 ~ 0x0705 OSD RLC Registers

0x0704 – OSD RLC Register

Bit	Function	R/W	Description	Reset
7 - 5	Reserved	-	Reserved	-
4	RLC_PKTE	R/W	RLC packet enable 0: Disable 1: Enable	0
3 - 2	Reserved	-	Reserved	-
1	RLC_RESET	R/W	RLC reset 0: Normal 1: Reset	0
0	RLC_ENA	R/W	RLC function enable 0: Disable 1: Enable	0

0x0705 – OSD RLC Register

Bit	Function	R/W	Description	Reset
7 – 4	RLC_DCNT	R/W	RLC data count bit	0
3 - 0	RLC_CNTT	R/W	RLC counter count bit	0

0x0706 – OSD/OSG Control Register

Bit	Function	R/W	Description	Reset
7	OSDTEST	R/W	OSD test	0
6 - 1	-	R/W	Reserved	-
0	OSDPDN	R/W	Power down OSD module	0

0x070B – BitBlt Logic Register

Bit	Function	R/W	Description	Reset
7 – 0	BBLTMEM	R/W	BitBlt logic operation register The content of this register specifies the bit wise logic operation of BitBlt Mask Register, Destination pixel, and Source pixel. For each bit wise index "i", the three bit combination of BitBlt_Mask_Register[i], Destination_pixel[i], and Source_pixel[i] uniquely points to one bit location in BitBlt Logic Register. This BitBlt Logic Register (BBLR) bit content specifies the resulting bit wise logic operation. The following truth table is used in establishing the default content of BBLR. This default value provides the logic operation of 1) if Mask bit is "1", the outcome follows the Destination pixel, 2) if Mask bit is "0", the outcome follows the Source pixel	1100 1010

BitBlt_Mask_Register[i]	Destination_pixel[i]	Source_pixel[i]	Result (BBLR content)	BBLR bit position
1	1	1	1	7
1	1	0	1	6
1	0	1	0	5
1	0	0	0	4
0	1	1	1	3
0	1	0	0	2
0	0	1	1	1
0	0	0	0	0

0x070C ~ 0x070D BitBlt Mask Register

0x070C – High byte Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	BitBlt Mask, high byte; not used for 8 bit color	0

0x070D – Low byte Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	BitBlt Mask, low byte	0

0x070E ~ 0x070F Block Fill Color

0x070E – High byte Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Fill color register for Block Fill operation, high byte for 16 bit color; not used for 8 bit color	0

0x070F – Low byte Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Fill color register for Block Fill operation, low byte for 16 bit color	0

0x0710 ~ 0x071F 8 Bit Color Expansion Table

0x0710 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 8 bit color	0

0x0711 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 8 bit color	0

0x071F – Entry 15 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 8 bit color	0

0x0720 ~ 0x073F 16 Bit Color Expansion Table

0x0720 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 16 bit color high byte	0

0x0721 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 16 bit color low byte	0

0x0722 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 16 bit color high byte	0

0x0723 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 16 bit color low byte	0

0x073E – Entry 15 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 16 bit color high byte	0

0x073F – Entry 15 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Data for bit expansion to 16 bit color low byte	0

0x0740 ~ 0x0747 Color Conversion Source Color

0x0740 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, high byte for 16 bit color; not used for 8 bit color	0

0x0741 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, low byte for 16 bit color Source pixel that matches this entry is converted to the corresponding target color	0

0x0742 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, high byte for 16 bit color; not used for 8 bit color	0

0x0743 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, low byte for 16 bit color Source pixel that matches this entry is converted to the corresponding target color	0

0x0744 – Entry 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, high byte for 16 bit color; not used for 8 bit color	0

0x0745 – Entry 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, low byte for 16 bit color Source pixel that matches this entry is converted to the corresponding target color	0

0x0746 – Entry 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, high byte for 16 bit color; not used for 8 bit color	0

0x0747 – Entry 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Source color comparison register, low byte for 16 bit color Source pixel that matches this entry is converted to the corresponding target color	0

0x0748 ~ 0x074F Color Conversion Target Color

0x0748 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 0, high byte for 16 bit color; not used for 8 bit color	0

0x0749 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 0, low byte for 16 bit color	0

0x074A – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 1, high byte for 16 bit color; not used for 8 bit color	0

0x074B – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 1, low byte for 16 bit color	0

0x074C – Entry 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 2, high byte for 16 bit color; not used for 8 bit color	0

0x074D – Entry 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 2, low byte for 16 bit color	0

0x074E – Entry 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 3, high byte for 16 bit color; not used for 8 bit color	0

0x074F – Entry 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Target color register corresponding to the source color entry 3, low byte for 16 bit color	0

0x0750 ~ 0x0757 Selective Overwrite

0x0750 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 0, high byte for 16 bit color; not used for 8 bit color Selective Overwrite function is invoked when the MSKSEL (0x0700_bit[5:4]) is set to "00". Source pixel after source color conversion is compared against this Selective Overwrite register. If there is a comparison match, the pixel is further processed by BitBlt logic. If the BBLR (0x070B) has the default reset value, then the comparison match will result in the destination keeping the original content; while the mismatch will result in the destination replaced by the color-conversion-processed source pixel.	0

0x0751 – Entry 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 0, low byte for 16 bit color	0

0x0752 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 1, high byte for 16 bit color; not used for 8 bit color	0

0x0753 – Entry 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 1, low byte for 16 bit color (See description on entry 0)	0

0x0754 – Entry 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 2, high byte for 16 bit color; not used for 8 bit color	0

0x0755 – Entry 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 2, low byte for 16 bit color (See description on entry 0)	0

0x0756 – Entry 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 3, high byte for 16 bit color; not used for 8 bit color	0

0x0757 – Entry 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	-	R/W	Overwrite comparison register entry 3, low byte for 16 bit color (See description on entry 0)	0

0x0760 ~ 0x0762 Source Buffer Memory Starting Address[23:0] Registers

0x0760 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCBFM0_AST_HB	R/W	This register defines the Source Buffer Memory starting address for OSD block transfer; four bytes per increment. This register also serves as the memory starting address in linear block transfer.	0

0x0761 – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCBFM0_AST_MB	R/W	Source Buffer Memory starting address for OSD block transfer	0

0x0762 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCBFM0_AST_LB	R/W	Source Buffer Memory starting address for OSD block transfer	0

0x0763 – Source Buffer Memory Horizontal Length [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCBFM0_HL	R/W	Define the Source Buffer Memory horizontal wrap around length (64 pixels per increment; min length: 64 pixels; max length 2048 pixels)	0

0x0764 ~ 0x0765 Transfer Source Horizontal Start [10:0] Registers

0x0764 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	SRCSH_HB	R/W	Define the horizontal offset from the Source Buffer Memory starting location. (one pixel per increment). This register and the Transfer Source Vertical Start register together specify the starting pixel location inside the Source Buffer Memory for the block transfer operation	0

0x0765 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCSH_LB	R/W	(See description above)	0

0x0766 ~ 0x0767 Transfer Source Vertical Start [10:0] Registers

0x0766 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	SRCSV_HB	R/W	Define the vertical offset from the Source Buffer Memory starting location. (one line per increment)	0

0x0767 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCSV_LB	R/W	(See description above)	0

0x0768 ~ 0x0769 Transfer Horizontal Length[11:0] Registers

0x0768 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 4	-	--	Reserved.	-
3 – 0	SRCHL_HB	R/W	Define the horizontal block length in block transfer, block fill, or MCU/DMA write operations. Low byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x0769 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCHL_LB	R/W	(See description above)	0

0x076A ~ 0x076B Transfer Vertical Length[11:0] Registers

0x076A – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 4	-	--	Reserved.	-
3 – 0	SRCVL_HB	R/W	Define the vertical block length in block transfer, block fill, or MCU/DMA write operations. Low byte (one line per increment, minimum is 1, maximum is 2048)	0

0x076B – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	SRCVL_LB	R/W	(See description above)	0

0x0770 ~ 0x0772 Destination Buffer Memory Starting Address[23:0] Registers

0x0770 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	DSTBFM0_AST_HB	R/W	Destination buffer memory starting address for block transfer, block fill or MCU/DMA write; four bytes per increment	0

0x0771 – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	DSTBFM0_AST_MB	R/W	(See description above)	0

0x0772 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	DSTBFM0_AST_LB	R/W	(See description above)	0

0x0773 – Destination Buffer Memory Horizontal Length[7:0] Registers

Bit	Function	R/W	Description	Reset
7 – 0	DSTBFM0_HL	R/W	Define the Destination Buffer Memory horizontal wrap around length (64 pixels per increment; min length: 64 pixels; max length 2048 pixels)	0

0x0774 ~ 0x0775 Transfer Destination Horizontal Start[10:0] Registers

0x0774 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	DSTSH_HB	R/W	Define the horizontal offset from the Destination Buffer Memory starting location. (one pixel per increment). This register and the Transfer Destination Vertical Start register together specify the starting pixel location inside the Destination Buffer Memory for the block transfer, block fill, or MCU/DMA write operations.	0

0x0775 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	DSTSH_LB	R/W	(See description above)	0

0x0776 ~ 0x0777 Transfer Destination Vertical Start[10:0] Registers

0x0776 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	DSTSV_HB	R/W	Define the vertical offset from the Destination Buffer Memory starting location. (one line per increment)	0

0x0777 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	DSTSV_LB	R/W	(See description above)	0

0x0778 – OSD Control Register

Bit	Function	R/W	Description	Reset
7 - 6	BLTSEL	R/W	Blink timer interval selection 00: 32 frames 01: 16 frames 10: 8 frames 11: 4 frames	0
5	FLIP	R/W	Enable OSD flip (upside down) display	0
4	MIRROR	R/W	Enable OSD mirror display	0
3 - 2	-	R/W	Reserved.	
1	FUPDATE	R/W	Update OSD Window registers straight through Set this bit to one and the register write operation of OSD Window 0, Window 1, and Window 4 takes effect right away	0
0	OSDUPDATE	R/W	Update OSD Window registers on Panel Vsync After writing new values to OSD Window 0, Window 1, and Window4 registers and then write this bit to "1", the values of those register are updated on the next Panel Vsync Self cleared to "0' after update is done	0

0x0779 – OSD Gain Control Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved	0000 0
2 – 0	OSDGAIN	R/W	OSD gain value control for the blended OSD 000: 1.0 100: 0.797 001: 0.953 101: 0.750 010: 0.906 110: 0.703 011: 0.859 111: 0.656	000

8 Bit and 16 Bit OSD Window

Each 8 bit OSD window is associated with a look up table

Each table is organized as 256 x 32 bits

Bit composition: [31]: Blink [30-24] : Alpha value [23-16]: R [15-8]: G [7-0]: B

Window 0 and Window 1 are designated as 8 bit OSD

Window 0 does not blend with Window 1

Window 0 has higher priority over Window 1

Window 4 is designated as 16 bit OSD

8 bit OSD blends with 16 bit OSD

0x077A – 8 Bit OSD Look Up Table Access Control Register

Bit	Function	R/W	Description	Reset
7 - 6	LUTWIN	R/W	This bit selects which look up table to access 00: Look up table for window 0 01: Look up table for window 1 1X: Reserved	0
5 - 0	-	R/W	Reserved.	-

0x077B – 8 Bit OSD Look Up Table Address[7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	LUTADDR	R/W	Address pointer to the 256 x 32 look up table	0

0x077C ~ 0x077F 8 Bit OSD Look Up Table Data Port[31:0] Register

0x077C – Byte 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	LUTDIN	R/W	Write data to the look up table bit [31:24]	-

0x077D – Byte 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	LUTDIN	R/W	Write data to the look up table bit [23:16]	-

0x077E – Byte 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	LUTDIN	R/W	Write data to the look up table bit [15:8]	-

0x077F – Byte 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	LUTDIN	R/W	Write data to the look up table bit [7:0]	-

0x0780 – OSD Window 0 Enable Register

Bit	Function	R/W	Description	Reset
7 – 6	-	--	Reserved.	-
5	WIN0_PERPIX	R/W	OSD window 0 alpha blending selection 0: Global window 0 alpha 1: Per pixel alpha	0
4	WIN0_ALPHA_ENA	R/W	OSD window 0 alpha blending enable	0
3 - 1	-	--	Reserved.	-
0	WIN0_ENA	R/W	OSD window 0 (8 bit) enable; priority is higher than OSD window 1	0

0x0781 ~ 0x0782 OSD Window 0 Horizontal Start [10:0] Registers

0x0781 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN0_HS_HB	R/W	OSD window 0 horizontal start (offset from the LCD display first left pixel) High byte	0

0x0782 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN0_HS_LB	R/W	OSD window 0 horizontal start (offset from the LCD display first left pixel) Low byte	0

0x0783 ~ 0x0784 OSD Window 0 Vertical Start [10:0] Register

0x0783 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN0_VS _HB	R/W	OSD window 0 Verticall start (offset from the LCD display top first line) High byte	0

0x0784 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN0_VS _LB	R/W	OSD window 0 Vertical start (offset from the LCD display top first line) Low byte	0

0x0785 ~ 0x0786 OSD Window 0 Horizontal Length [11:0] Registers

0x0785 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 4	-	--	Reserved.	-
3 – 0	WIN0_HL_ HB	R/W	OSD window 0 horizontal Length High byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x0786 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN0_HL_ LB	R/W	OSD window 0 horizontal Length Low byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x0787 ~ 0x0788 OSD Window 0 Vertical Length [11:0] Registers

0x0787 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN0_VL_ HB	R/W	OSD window 0 vertical Length High byte (one line per increment, minimum is 1, maximum is 2048)	0

0x0788 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN0_VL_ LB	R/W	OSD window 0 vertical Length Low byte (one line per increment, minimum is 1, maximum is 2048)	0

0x0789 ~ 0x078B OSD Window 0 Buffer Memory Starting Address [23:0] Register

0x0789 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM0_AST_HB	R/W	Starting address of the Buffer Memory area allocated for OSD window 0; four bytes per increment	0

0x078A – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM0_AST_MB	R/W	Starting address of the Buffer Memory area allocated for OSD window 0	0

0x078B – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM0_AST_LB	R/W	Starting address of the Buffer Memory area allocated for OSD window 0	0

0x078C – OSD Window 0 Buffer Memory Horizontal Length [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM0_HL	R/W	Define the Window 0 Buffer Memory horizontal wrap around length (64 pixels per increment; min length: 64 pixels; max length 2048 pixels)	0

0x078D – OSD Window 0 Buffer Memory Vertical Length [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM0_VL	R/W	Define the Window 0 Buffer Memory vertical length (64 lines per increment; min length: 64 lines; max length 2048 lines)	0

0x078E ~ 0x078F OSD Window 0 Image Horizontal Start [10:0] Registers

0x078E – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	WFM0_HS_HB	R/W	Define the horizontal offset of the OSD Window 0 image in the Buffer Memory (Referenced to the Window 0 Buffer Memory starting location; one pixel per increment)	0

0x078F – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WFM0_HS_LB	R/W	(See description above)	0

0x0790 ~ 0x0791 OSD Window 0 Image Vertical Start [10:0] Register

0x0790 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	WFM0_VS_HB	R/W	Define the vertical offset of the OSD Window 0 image in the Buffer Memory (Referenced to the Window 0 Buffer Memory starting location; one line per increment)	0

0x0791 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WFM0_VS_LB	R/W	(See description above)	0

0x0792 – OSD Window 0 Global Alpha Value [6:0] Register

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	WIN0_ALPHA	R/W	OSD window 0 global alpha blending value Min: 0x00 Max OSD window 0 shown after blending Max: 0x7F No OSD window 0 shown after blending	0

0x07A0 – OSD Window 1 Enable Register

Bit	Function	R/W	Description	Reset
7 – 6	-	--	Reserved.	-
5	WIN1_PERPIX	R/W	OSD window 1 alpha blending selection 0: Global window 1 alpha 1: Per pixel alpha	0
4	WIN1_ALPHA_ENA	R/W	OSD window 1 alpha blending enable	0
3 - 1	-	--	Reserved.	-
0	WIN1_ENA	R/W	OSD window 1 (8 bit) enable; priority is lower than OSD window 0	0

0x07A1 ~ 0x07A2 OSD Window 1 Horizontal Start [10:0] Registers

0x07A1 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN1_HS_HB	R/W	OSD window 1 horizontal start (offset from the LCD display first left pixel) High byte	0

0x07A2 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN1_HS_LB	R/W	OSD window 1 horizontal start (offset from the LCD display first left pixel) Low byte	0

0x07A3 ~ 0x07A4 OSD Window 1 Vertical Start [10:0] Registers

0x07A3 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN1_VS_HB	R/W	OSD window 1 Vertical start (offset from the LCD display top first line) High byte	0

0x07A4 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN1_VS_LB	R/W	OSD window 1 Vertical start (offset from the LCD display top first line) Low byte	0

0x07A5 ~ 0x07A6 OSD Window 1 Horizontal Length [11:0] Registers

0x07A5 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 4	-	--	Reserved.	-
3 – 0	WIN1_HL_HB	R/W	OSD window 1 horizontal Length High byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x07A6 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN1_HL_LB	R/W	OSD window 1 horizontal Length Low byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x07A7 ~ 0x07A8 OSD Window 1 Vertical Length [11:0] Registers

0x07A7 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN1_VL_HB	R/W	OSD window 1 vertical Length High byte (one line per increment, minimum is 1, maximum is 2048)	0

0x07A8 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WIN1_VL_LB	R/W	OSD window 1 vertical Length Low byte (one line per increment, minimum is 1, maximum is 2048)	0

0x07A9 ~ 0x07AB OSD Window 1 Buffer Memory Starting Address [23:0] Registers

0x07A9 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM1_AST_HB	R/W	Starting address of the Buffer Memory area allocated for OSD window 1; four bytes per increment	0

0x07AA – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM1_AST_MB	R/W	Starting address of the Buffer Memory area allocated for OSD window 1	0

0x07AB – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM1_AST_LB	R/W	Starting address of the Buffer Memory area allocated for OSD window 1	0

0x07AC – OSD Window 1 Buffer Memory Horizontal Length [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM1_HL	R/W	Define the Window 1 Buffer Memory horizontal wrap around length (64 pixels per increment; min length: 64 pixels; max length 2048 pixels)	0

0x07AD – OSD Window 1 Buffer Memory Vertical Length [7:0] Register

Bit	Function	R/W	Description	Reset
7 – 0	BFM1_VL	R/W	Define the Window 1 Buffer Memory vertical length (64 lines per increment; min length: 64 lines; max length 2048 lines)	0

0x07AE ~ 0x07AF OSD Window 1 Image Horizontal Start [10:0] Register

0x07AE – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	WFM1_HS_HB	R/W	Define the horizontal offset of the OSD Window 1 image in the Buffer Memory (Referenced to the Window 0 Buffer Memory starting location; one pixel per increment)	0

0x07AF – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WFM1_HS_LB	R/W	(See description above)	0

0x07B~ 0x07B1 OSD Window 1 Image Vertical Start [10:0] Registers

0x07B0 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	WFM1_VS_HB	R/W	Define the vertical offset of the OSD Window 1 image in the Buffer Memory (Referenced to the Window 0 Buffer Memory starting location; one line per increment)	0

0x07B1 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	WFM1_VS_LB	R/W	(See description above)	0

0x07B2 – OSD Window 1 Global Alpha Value [6:0] Register

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	WIN1_ALPHA	R/W	OSD window 1 global alpha blending value Min: 0x00 Max OSD window 1 shown after blending Max: 0x7F No OSD window 1 shown after blending	0

0x07C0 – OSD Window 4 Enable

Bit	Function	R/W	Description	Reset
7	REV_CBR	R/W	Interchange the position of Cb with the Cr's when the data format "OSD16FORM" is YCbCr422 or YCbCr655 0: Normal position (Y8Cb8, Y8Cr8), (Y6, Cb5, Cr5) 1: Reverse position (Y8Cr8, Y8Cb8), (Y6, Cr5, Cb5)	0
6	-	--	Reserved.	0
5	WIN4_PERPIX	R/W	OSD window 4 alpha blending selection 0: Global window 4 alpha 1: For RGB4444 this bit select individual alpha; for the other formats this bit enable the color key alpha blending	0
4	WIN4_ALPHA_ENA	R/W	OSD window 4 alpha blending enable	0
3 - 1	OSD16FORM	--	Format selection for OSD window 4: 000: YCbCr422 (Y8Cb8, Y8Cr8) Data0[15:0] = {Y1[7:0], Cb1[7:0]} Data1[15:0] = {Y2[7:0], Cr2[7:0]} 001: RGB565 (R 5, G 6, B 5) Data[15:0] = {R[4:0],G[5:4],G[3:0],B[4:0]} 010: RGB4444 (alpha 4, R 4, G 4, B 4) Data[15:0] = {A[3:0],R[3:0],G[3:0],B[3:0]} 011: RGB1555 (blink 1, R 5, G 5, B 5) Data[15:0] = {BL, R[4:0],G[4:0],B[4:0]} 100: YCbCr655 (Y 6, Cb 5, Cr 5) Data[15:0] = {Y[5:0],Cb[4:0],Cr[4:0]}	0
0	WIN4_ENA	R/W	OSD window 4 (16 bit) enable	0

0x07C1 ~ 0x07C2 OSD Window 4 Horizontal Start [10:0]

0x07C1 – High Byte

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN4_HS _HB	R/W	OSD window 4 horizontal start (offset from the LCD display first left pixel) High byte	0

0x07C2 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	WIN4_HS _LB	R/W	OSD window 4 horizontal start (offset from the LCD display first left pixel) Low byte	0

0x07C3 ~ 0x07C4 OSD Window 4 Vertical Start [10:0]

0x07C3 – High Byte

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN4_VS _HB	R/W	OSD window 4 Vertical start (offset from the LCD display top first line) High byte	0

0x07C4 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	WIN4_VS _LB	R/W	OSD window 4 Vertical start (offset from the LCD display top first line) Low byte	0

0x07C5 ~ 0x07C6 OSD Window 4 Horizontal Length [11:0]

0x07C5 – High Byte

Bit	Function	R/W	Description	Reset
7 – 4	-	--	Reserved.	-
3 – 0	WIN4_HL_ HB	R/W	OSD window 4 horizontal Length High byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x07C6 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	WIN4_HL_ LB	R/W	OSD window 4 horizontal Length Low byte (one pixel per increment, minimum is 1, maximum is 2048)	0

0x07C7 ~ 0x07C8 OSD Window 4 Vertical Length [11:0]

0x07C7 – High Byte

Bit	Function	R/W	Description	Reset
7 – 3	-	--	Reserved.	-
2 – 0	WIN4_VL_HB	R/W	OSD window 4 vertical Length High byte (one line per increment, minimum is 1, maximum is 2048)	0

0x07C8 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	WIN4_VL_LB	R/W	OSD window 4 vertical Length Low byte (one line per increment, minimum is 1, maximum is 2048)	0

0x07C9 ~ 0x07CB Window 4 Buffer Memory Starting Address [23:0]

0x07C9 – High Byte

Bit	Function	R/W	Description	Reset
7 – 0	BFM4_AST_HB	R/W	Starting address of the Buffer Memory area allocated for OSD window 4; four bytes per increment	0

0x07CA – Mid Byte

Bit	Function	R/W	Description	Reset
7 – 0	BFM4_AST_MB	R/W	Starting address of the Buffer Memory area allocated for OSD window 4	0

0x07CB – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	BFM4_AST_LB	R/W	Starting address of the Buffer Memory area allocated for OSD window 4	0

0x07CC – OSD Window 4 Buffer Memory Horizontal Length [7:0]

Bit	Function	R/W	Description	Reset
7 – 0	BFM4_HL	R/W	Define the Window 4 Buffer Memory horizontal wrap around length (64 pixels per increment; min length: 64 pixels; max length 2048 pixels)	0

0x07CD – OSD Window 4 Buffer Memory Vertical Length [7:0]

Bit	Function	R/W	Description	Reset
7 – 0	BFM4_VL	R/W	Define the Window 4 Buffer Memory vertical length (64 lines per increment; min length: 64 lines; max length 2048 lines)	0

0x07CE ~ 0x07CF OSD Window 4 Image Horizontal Start [10:0]

0x07CE – High Byte

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	WFM4_HS_HB	R/W	Define the horizontal offset of the OSD Window 4 image in the Buffer Memory (Referenced to the Window 0 Buffer Memory starting location; one pixel per increment)	0

0x07CF – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	WFM4_HS_LB	R/W	(See description above)	0

0x07D0 ~ 0x07D1 OSD Window 4 Image Vertical Start [10:0]

0x07D0 – High Byte

Bit	Function	R/W	Description	Reset
7 – 3	-	R/W	Reserved.	
2 – 0	WFM4_VS_HB	R/W	OSD window 4 buffer memory Vertical start	0

0x07D1 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	WFM4_VS_LB	R/W	Define the vertical offset of the OSD Window 4 image in the Buffer Memory (Referenced to the Window 0 Buffer Memory starting location; one line per increment)	0

0x07D2 – OSD Window 4 Global Alpha Value [6:0]

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	WIN4_ALPHA	R/W	OSD window 4 global alpha blending value Min: 0x00 Max OSD window 4 shown after blending Max: 0x7F No OSD window 4 shown after blending	0

0x07D4 ~ 0x07D5 Color Key 0 for 16 bit OSD [15:0]

0x07D4 – High Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY0_HB	R/W	Color key # 0 high byte	0

0x07D5 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY0_LB	R/W	Color key # 0 low byte	0

0x07D6 ~ 0x07D7 Color Key 1 for 16 bit OSD [15:0]

0x07D6 – High Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY1_HB	R/W	Color key # 1 high byte	0

0x07D7 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY1_LB	R/W	Color key # 1 low byte	0

0x07D8 ~ 0x07D9 Color Key 2 for 16 bit OSD [15:0]

0x07D8 – High Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY2_HB	R/W	Color key # 2 high byte	0

0x07D9 – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY2_LB	R/W	Color key # 2 low byte	0

0x07DA ~ 0x07DB Color Key 3 for 16 bit OSD [15:0]

0x07DA – High Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY3_HB	R/W	Color key # 3 high byte	0

0x07DB – Low Byte

Bit	Function	R/W	Description	Reset
7 – 0	CKEY3_LB	R/W	Color key # 3 low byte	0

0x07DC – Color Key 0 Alpha Value [6:0]

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	KEY_ALPHA0	R/W	Alpha blending value for color key # 0	0

0x07DD – Color Key 1 Alpha Value [6:0]

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	KEY_ALPHA1	R/W	Alpha blending value for color key # 1	0

0x07DE – Color Key 2 Alpha Value [6:0]

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	KEY_ALPHA2	R/W	Alpha blending value for color key # 2	0

0x07DF – Color Key 3 Alpha Value [6:0]

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	
6 – 0	KEY_ALPHA3	R/W	Alpha blending value for color key # 3	0

OSD Interrupt Enable, Vertical Active Status

0x07F0 – Vertical Active Status

Bit	Function	R/W	Description	Reset
7-6	-	R/W	Reserved.	0
5	DISP_ATE	R/W	Display vertical active status: Set by the display vertical active ending edge Reset by writing a "1" to this bit.	-
4	OSD_ATE	R/W	OSD window active status: Set by the OSD window active ending edge Reset by writing a "1" to this bit	-
3	WIN4_AT	R	OSD Window 4 vertical active status	-
2	-	R/W	Reserved.	-
1	WIN1_AT	R	OSD Window 1 vertical active status	-
0	WIN0_AT	R	OSD Window 0 vertical active status	-

0x07F1 – OSD Busy Interrupt Enable

Bit	Function	R/W	Description	Reset
7	OSD_W_ MASK0	R/W	Mask (disable) host interrupt by the OSG operation busy, 0x0701[7] 1: Mask on 0: Mask off	0
6	OSD_W_ MASK1	R/W	Mask (disable) host interrupt by the OSG FIFO busy, 0x0701[6] 1: Mask on 0: Mask off	0
5	DISP_ATE _MASK	R/W	Mask (disable) host interrupt by the Display active status, 0x07F0[5] 1: Mask on 0: Mask off	0
4	OSD_ATE _MASK	R/W	Mask (disable) host interrupt by the OSD active status, 0x07F0[4] 1: Mask on 0: Mask off	0
3-0	-	R/W	Reserved.	0

Main/Sub Path OSD Selection

0x07F8 – Main/Sub Path OSD Selection

Bit	Function	R/W	Description	Reset
7:6	-	R/W	Reserved	0
5:4	SUB_SEL	R/W	Sub Path (in Dual View) OSD selection 00: No OSD 01:: 8-Bit OSD 10: 16-Bit OSD 11: 8-Bit and 16-Bit OSD	0
3:2	-	R/W	Reserved	0
	MAIN_SE L	R/W	Main Path OSD selection 00: No OSD 01:: 8-Bit OSD 10: 16-Bit OSD 11: 8-Bit and 16-Bit OSD	0

External OSD

0x08F2– External OSD Control

Bit	Function	R/W	Description	Reset
7	EOSD_MODE	R/W	External OSD Clock mode 0: Clock is on all the time 1: Clock is on during the horizontal active region plus two times of 0x08F2[3:1] The horizontal active is determined by 0x08F3[0]	1
6	EOSD_VS_POL	R/W	External OSD VS polarity control 0: Active High, 1: Active Low	0
5	EOSD_HS_POL	R/W	External OSD HS polarity control 0: Active High, 1: Active Low	0
4	EOSD_CK_POL	R/W	External OSD Clock polarity control 0: Falling edge, 1: Rising edge	0
3 – 1	EOSDDELAY	R/W	External OSD Access Latency control	0
0	OSD_PORTEN	R/W	External OSD Port Enable/Disable 0: Disable, 1: Enable	0

0x08F3 – External OSD Horizontal Control

Bit	Function	R/W	Description	Reset
7 – 2	EOSD_HS_PW	--	External OSD HS Pulse Width [5:0] 0: One EOCLK 1: Two EOCLK … 63: Sixty-four EOCLK …	0
1	EXSYNC_SEL	R/W	External OSD Sync mode selection 0: External OSD pins EOVS/EOHS are derived from Vactive/Hactive The Hactive is further determined by 0x08F3[0] 1: External OSD pins EOVS/EOHS are derived from panel Vsync/Hsync	0
0	EXHACT_SEL	R/W	Horizontal active selection 0: Use internal OSD Window 0 horizontal active 1: Use panel Hactive	0

0x08F4 – External OSD Clock Output Delay

Bit	Function	R/W	Description	Reset
7	-	--	Reserved.	-
6 – 4	OCKTPS	R/W	External OSD clock EOCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	0
3 - 0	-	--	Reserved.	-

0x08F5 – External OSD Alpha Blending Level

Bit	Function	R/W	Description	Reset
7	ENA_EA_PIN	--	Enable External_Alpha_Blending pin input. 0: The blending is on 1: The blending on/off is controlled by the pin	0
6 – 5	-	--	Reserved.	-
4 – 0	EXT_ALPHA	R/W	External OSD Alpha-Blending Level Control. 0: Max External OSD shown	0

0x08F6 – External OSD Misc Control

Bit	Function	R/W	Description	Reset
7	-	R/W	Reserved.	-
6 - 4	EODEN_DLY	R/W	External OSD Input Data Enable signal Delay : 0 ~ 7 clock cycle delay	0
3 - 0	-	R/W	Reserved.	-

0x08F7 – External OSD Vsync Pulse Width

Bit	Function	R/W	Description	Reset
7:4	-	R/W	Reserve	-
3:0	EOSD_VS_PW	R/W	External OSD VS Pulse Width 0: One EOSD HS period 1: Two EOSD HS periods … 15: Sixteen EOSD HS periods	0

LCDC – Gamma & Dither & Key (waver_top)

0x0900 – LCDC Gamma Control Register

Bit	Function	R/W	Description	Reset
7	GAMAE_R	R/W	Enable Red gamma correction.	0
6	GAMAE_G	R/W	Enable Green gamma correction.	0
5	GAMAE_B	R/W	Enable Blue gamma correction.	0
4	Reserved	-	Reserved	-
3 - 2	AUTO_INC	R/W	Enable Gamma table address auto increment for reading/writing Gamma data port. 0 = Disable 1 = Read Only 2 = Write Only 3 = Read/Write	0
1 - 0	GAMMA_RGB_INDX	R/W	Gamma tables access selection: Index address 0x1F1 to 0x1F2 are used for gamma table accesses. There are 3 sets of gamma table, one table for one color, sharing the same address port and data port. These 2 bits identifies which table is accessed. 0 = RGB Gamma table 1 = Red Gamma table 2 = Green Gamma table 3 = Blue Gamma table	0

0x0901 – Gamma Table Address Port Register

Bit	Function	R/W	Description	Reset
7 - 0	GAMMA_RAM-STARTING_ADDR	R/W	Gamma table address port.	00

0x0902 – Gamma Table Data Port Register

Bit	Function	R/W	Description	Reset
7 - 2	Reserved	-	Reserved	-
1 - 0	GAMMA_RAM_DATA[9:8]	R/W	Gamma table data port (upper bits)	0

0x0903 – Gamma Table Data Port Register

Bit	Function	R/W	Description	Reset
7-0	GAMMA_RAM_DATA[7:0]	R/W	Gamma table data port (lower bits)	00

0x0910 – Dither Option Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	
6-4	DITHER_OPTION	R/W	Dither Option Code "010" is recommended for 6:6:6 output	000
3	Reserved	-	Reserved	-
2-0	DITHER_FORMAT	R/W	Dither Output Format Selection "001" is recommended for 6:6:6 output	000

Dither Output Selection and Calculations

Dither Output Format Selection	Flat Panel RGB Bit Format Output	Dither Option Code	Input LSBs Used in Dither Calculation	Dither Method
000	8:8:8	**000**	n/a	none
001	6:6:6	**001**	(3) (3) (3)	2x2
		010	(3,2) (3,2)(3,2)	2x2
		011	(3,2,1) (3,2,1)(3,2,1)	2x2
		100	(3,2,1,0) (3,2,1,0)(3,2,1,0)	4x4
010	5:6:5	**001**	(4) (3) (4)	2x2
		010	(4,3) (3,2) (4,3)	2x2
		011	(4,3,2) (3,2) (4,3,2)	2x2
		100	4,3,2,1) (3,2,1) (4,3,2,1)	4x4
011	5:5:5	**001**	(4) (4) (4)	2x2
		010	(4,3) (4,3) (4,3)	2x2
		011	(4,3,2) (4,3,2) (4,3,2)	2x2
		100	(4,3,2,1) (4,3,2,1) (4,3,2,1)	4x4
100	4:4:4	**001**	(5) (5) (5)	2x2
		010	(5,4) (5,4) (5,4)	2x2
		011	(5,4,3) (5,4,3) (5,4,3)	2x2
		100	(5,4,3,2) (5,4,3,2) (5,4,3,2)	4x4
101	3:3:3	**001**	(6) (6) (6)	2x2
		010	(6,5) (6,5) (6,5)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (6,5,4,3)	4x4
110	3:3:2	**001**	(6) (6) (7)	2x2
		010	(6,5) (6,5) (7,6)	2x2
		011	(6,5,4) (6,5,4) (6,5,4)	2x2
		100	(6,5,4,3) (6,5,4,3) (7,6,5,4)	4x4

0x0920 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RDKEYPOS_X	R/W	Color level readout position X [7:0] (LSB)	00

0x0921 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7-0	RDKEYPOS_Y	R/W	Color level readout position Y [7:0] (LSB)	00

0x0922 – RGB Level Readout Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-4	RDKEYPOS_Y[10:8]	R/W	Color level readout position Y [10:8] (MSB)	0
3-0	RDKEYPOS_X[11:8]	R/W	Color level readout position X [11:8] (MSB)	0

0x0923 – PIP Alpha Blending Red Key Register

Bit	Function	R/W	Description	Reset
7-0	KEYRDR	R/W	Red key color level for PIP alpha blending	00

0x0924 – PIP Alpha Blending Green Key Register

Bit	Function	R/W	Description	Reset
7-0	KEYRDG	R/W	Green key color level for PIP alpha blending	00

0x0925 – PIP Alpha Blending Blue Key Register

Bit	Function	R/W	Description	Reset
7-0	KEYREB	R/W	Blue key color level for PIP alpha blending	00

LCDC – TGA & Power Management

0x0970 – Panel Interface Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	0
6	FPDEAH	R/W	Set FPDE Active High 0: Active Low	1
5	FPHSAH	R/W	Set FPHS Active High 0: Active Low	0
4	FPVSAH	R/W	Set FPVS Active High 0: Active Low	0
3	RVFPCK	R/W	Invert FPCLK polarity 0: Output signals to flat panel (FPVS, FPHS, … etc.) are referenced to the falling edge of FPCLK.	0
2	Reserved	-	Reserved	0
1	RVBIT	R/W	Reverse the bit order on panel data bus. 0: MSB is on FPR0[7], FPG0[7], FPB0[7] 1: MSB is on FPR0[0], FPG0[0], FPB0[0]	0
0	Reserved	-	Reserved	0

0x0971 – Panel Clock Delay Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	
2 – 0	FPCLK_DELAY	R/W	Panel clock FPCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	0

0x0987 – PWM Control Register

Bit	Function	R/W	Description	Reset
7 – 6	Reserved	-	Reserved	0
5	PWMEN	R/W	Enable for PWM	0
4	PWMAL	R/W	Active Low for PWM	0
3 – 0	Reserved	-	Reserved	0

0x0988 – PWM Control Register

Bit	Function	R/W	Description	Reset
7 – 0	PWM_CNT	R/W	Positive pulse width of the PWM. If this register has an “N” value, the positive pulse width duration is “N+1” PWM clocks.	40h

0x0989 ~ 0x098A PWM Clock Divider Registers

0x0989 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 2	Reserved	-	Reserved	0
1 – 0	PWM_DIVNUM [9:8]	R/W	Clock divider for PWM - high	0

0x098A – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	PWM_DIVNUM [7:0]	R/W	Clock divider for PWM – low This register divides the 27 MHz clock down to drive PWM counter	0

0x098B – PWM2 Control Register

Bit	Function	R/W	Description	Reset
7 – 6	Reserved	-	Reserved	0
5	PWM2EN	R/W	Enable for PWM2	0
4	PWM2AL	R/W	Active Low for PWM2	0
3 – 0	Reserved	-	Reserved	0

0x098C – PWM2 Control Register

Bit	Function	R/W	Description	Reset
7 – 6	PWM2_CNT	R/W	Positive pulse width of the PWM2. If this register has an “N” value, the positive pulse width duration is “N+1” PWM2 clocks.	40h

0x098D ~ 0x098E PWM2 Clock Divider Registers

0x098D – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 2	Reserved	-	Reserved	0
1 – 0	PWM2_DIVNUM [9:8]	R/W	Clock divider for PWM2 - high	0

0x098E – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	PWM2_DIVNUM [7:0]	R/W	Clock divider for PWM2 – low This register divides the 27 MHz clock down to drive PWM2 counter	0

0x09F5 – Panel Power Pin Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2	FPBIAS	R/W	Set the FPBIAS pin value to high or low	0
1	EPPWR	R/W	Set the FPPWC pin value to high or low	0
0	EFPIF	R/W	Enable the output driver of the panel interface signals 1: Output enable 0: Output tristated	0

LCDC Timing Controller Configuration Registers

0x0A00 – Output Mode Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	---
6	TCCK_PH	R/W	TCCLK phase control if reg0x300[0] set is high. (Divide Clock Mode) 0 : No clock phase shift 1 : Clock phase 90 degree shift *** It's set reg0x270[3] (invert clock polarity) high and this bit set high also then TCCLK is 270 degree shift.	0
5	ROE_EN	R/W	ROE (Row Driver) Output Enable 0 : Disable 1 : Enable	0
4-2	Reserved	-	Reserved	--
1	TCONS	R/W	0 : Disable TCON 1 : Enable TCON	0
0	DIV_CK	R/W	Output mode selection 0 : One pixel data out per TCCLK 1 : Two pixel data out per TCCLK (Rising and Falling both)	0

0x0A01 – Display Control Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	---
6	Reserved	-	Reserved	0
5	Reserved	-	Reserved	0
4	Reserved	-	Reserved	0
3	REV_EN	R/W	Pixel data reverse control 0 : Data no reverse (Don't case TCREV signal) 1 : Data reverse if TCREV signal is high period	0
2	Reserved	-	Reserved	---
1-0	INV	R/W	Inversion mode selection 2'b00 : Disable 2'b01 : Disable 2'b10 : Line Inversion 2'b11 : Frame Inversion	00

0x0A02 – Display Direction Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-2	TOP_BTM	R/W	Top/Bottom display direction select 2'b00 : Top low active (Normal) 2'b01 : Top high active (Normal) 2'b10 : Bottom low active (Flip) 2'b11 : Bottom high active (Flip)	00
1-0	LFT_RHT	R/W	Left/Right display direction select 2'b00 : Left low active (Normal) 2'b01 : Left high active (Normal) 2'b10 : Right low active (Mirror) 2'b11 : Right high active (Mirror)	11

0x0A03 – Control Signal Polarity Selection Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	----
5	POL_CON	R/W	TCON Polarity Swap Control	0
4	RCK_P	R/W	Row Driver Clock signal 0 : Active low 1 : Active high	0
3	ROE_P	R/W	Row Driver Output Enable signal 0 : Active low 1 : Active high	0
2	RSP_P	R/W	Row Driver Start Pulse signal 0 : Active low 1 : Active high	1
1	CLP_P	R/W	Column Driver Latch Pulse signal 0 : Active low 1 : Active high	1
0	CSP_P	R/W	Column Driver Start Pulse signal 0 : Active low 1 : Active high	1

0x0A04 – Control Signal Generation Method Register

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6	Reserved	-	Reserved	-
5	PGM_RCK	R/W	Row Driver Clock signal	1
4	PGM_ROE	R/W	Row Driver Output Enable signal 0 : This is generate during horizontal display enable. 1 : It's generated that set TCON register address 0x32C though 0x32F. Also, this is relative to vertical active register 0x30C though 0x30F.	1
3	PGM_RSP	R/W	Row Driver Start Pulse signal 0 : This signal immediately generate and then keep one horizontal period activation received from vertical active signal. 1 : It's generated that set TCON register address 0x324 though 0x327. Also, this is relative to vertical back porch register 0x279.	0
2	PGM_POL	R/W	0 : This Signal toggles when hsync toggle. 1: It's generated that set TCON register 0x310 through 0x311	1
1	PGM_CLP	R/W	Column Driver Latch Pulse signal 0 : This signal generate after horizontal display enable done a every scan line. 1 : It's generated that set TCON register address 0x312 though 0x315.	0
0	PGM_CSP	R/W	Column Driver Start Pulse signal 0 : This signal generate after horizontal display enable. 1 : It's generated that set TCON register address 0x31A though 0x31D. Also, this is relative to horizontal back porch register 0x274.	0

0x0A06 – Panel type Select Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	-	Reserved	---
2	FRC_DAC_INV	R/W	1 : Force DAC output always inverted 0 : Normal DAC output and inversion is based on polarity signal	0
1	REV_INV	R/W	Signal output selection 0 : TCINV signal output select 1 : TCREV output select	1
0	LINE_INV	R/W	Analog panel data swapping 0 : No data inversion 1 : Every line data inversion	0

0x0A0A – Special LCD Module Control Register

Bit	Function	R/W	Description	Reset
7	KP_SEL	R/W	1 : Enable Instruction Mode, 0 : Normal Mode	0
6	KP_ENA	R/W	Enable KOPIN Mode	0
5-4	RSP_WIDTH	R/W	Row Driver Start Pulse width (period) selection 0 : One horizontal period 1 : Two horizontal period 2 : Three horizontal period 3 : Four horizontal period	00
3-2	Reserved	-	Reserved	--
1-0	COMPANY	R/W	LCD module company selection 2'b00 : LG-Philips LCD module 2'b01 : Sharp LCD module 2'b10, 2'b11 : Other companies LCD module	10

0x0A0B – REVV(TCPOLP) / REVC(TCPOLN) Control Register

Bit	Function	R/W	Description	Reset
7-0	REVV_REVC	R/W	REVV_REVC[7 :0] for Sharp	4Dh

0x0A0C – Vertical Active Start High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	V_ST[11:8]	R/W	VER_ASH[11:8]	0h

0x0A0D – Vertical Active Start Low Register

Bit	Function	R/W	Description	Reset
7-0	V_ST[7:0]	R/W	VER_ASL[7:0]	00h

0x0A0E – Vertical Active End High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	V_ED[11:8]	R/W	VER_AEH[11:8]	02h

0x0A0F – Vertical Active End Low Register

Bit	Function	R/W	Description	Reset
7-0	V_ED[7:0]	R/W	VER_AEL[7:0]	94h

Column Driver Chip Control Signals Relative Registers

0x0A10 – Polarity Control High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	CP_SW[11:8]	R/W	Programmable polarity period high[11:8] value.	0h

0x0A11 – Polarity Control Low Register

Bit	Function	R/W	Description	Reset
7-0	CP_SW[7:0]	R/W	Programmable polarity period low[7:0] value.	00h

0x0A12 – Load/Latch Pulse Start High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	CLP_ST[11:8]	R/W	LP_HSH[11:8]	00h

0x0A13 – Load/Latch Pulse Start Low Register

Bit	Function	R/W	Description	Reset
7-0	CLP_ST[7:0]	R/W	LP_HSL[7 :0]	24h

0x0A14 – Load/Latch Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	CLP_ED[11:8]	R/W	LP_HEH[11:8]	0h

0x0A15 – Load/Latch Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	CLP_ED[7:0]	R/W	LP_HEL[7:0]	02h

0x0A1A – Column Driver Start Pulse High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	CSP_ST[11:8]	R/W	SP_HSH[11:8]	0h

0x0A1B – Column Driver Start Pulse Low Register

Bit	Function	R/W	Description	Reset
7-0	CSP_ST[7:0]	R/W	SP_HSL[7 :0]	3Ch

0x0A1C – Column Driver Start Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	CSP_ED[11:8]	R/W	SP_HEH[11 :8]	0h

0x0A1D – Column Driver Start Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	CSP_ED[7:0]	R/W	SP_HEL[7 :0]	01h

Row Driver Chip Control Signals Relative Registers

0x0A20 – Clock Start Pulse High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	RCK_ST[11:8]	R/W	RCK_HSH[11:8]	0

0x0A21 – Clock Start Pulse Low Register

Bit	Function	R/W	Description	Reset
7-0	RCK_ST[7:0]	R/W	RCK_HSL[7 :0]	64h

0x0A22 – Clock Start Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	RCK_ED[11:8]	R/W	RCK_HEH[11 :8]	01h

0x0A23 – Clock Start Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	RCK_ED[7:0]	R/W	RCK_HEL[7 :0]	F4h

0x0A24 – Row Start Pulse High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	RSP_ST[11:8]	R/W	RSP_VSH[11:8]	0h

0x0A25 – Row Start Pulse Low Register

Bit	Function	R/W	Description	Reset
7-0	RSP_ST[7:0]	R/W	RSP_VSL[7 :0]	37h

0x0A26 – Row Start Pulse Width High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	RSP_ED[11:8]	R/W	RSP_VEH[11 :8]	0h

0x0A27 – Row Start Pulse Width Low Register

Bit	Function	R/W	Description	Reset
7-0	RSP_ED[7:0]	R/W	RSP_VEL[7 :0]	01h

0x0A2C – Row Output Enable High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	ROE_ST[11:8]	R/W	ROE_HSH[11:8]	0

0x0A2D – Row Output Enable Low Register

Bit	Function	R/W	Description	Reset
7-0	ROE_ST[7:0]	R/W	ROE_HSL[7 :0]	0Ah

0x0A2E – Row Output Enable Width High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	ROE_ED[11:8]	R/W	ROE_HEH[11 :8]	0

0x0A2F – Row Output Enable Width Low Register

Bit	Function	R/W	Description	Reset
7-0	ROE_ED[7:0]	R/W	ROE_HEL[7 :0]	36h

0x0A34 – Sharp Mode Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	
3-0	SHARP_STR_H	R/W	Sharp same polarity start point high bits	0h

0x0A35 – Sharp Mode Register

Bit	Function	R/W	Description	Reset
7-0	SHARP_STR_L	R/W	Sharp same polarity start point low bits	20h

0x0A36 – Sharp Mode Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	---
3-0	SHARP_END_H	R/W	Sharp same polarity end point high bits	1h

0x0A37 – Sharp Mode Register

Bit	Function	R/W	Description	Reset
7-0	SHARP_END_L	R/W	Sharp same polarity end point low bits	E2h

0x0A38 – Direct Mode TCLP Width, Position and Step Control Register

Bit	Function	R/W	Description	Reset
7	CLPFB	R/W	Direct Mode TCLP Front/Back Position Selection	0
6	Reserved	-	Reserved	---
5-4	CLPW	R/W	Direct Mode TCLP Width Control	1h
3	Reserved	-	Reserved	---
2-0	CLPSEL	R/W	Direct Mode TCLP Position Step Control	5h

0x0A39 – Direct Mode TCSP Width and Step Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	---
5-4	CSPW	R/W	Direct Mode TCSP Width Control	0
3	Reserved	-	Reserved	---
2-0	CSPSEL	R/W	Direct Mode TCSP Position Step Control	1h

0x0A3A – Polarity Special Function Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	---
5	POL_H_ENA	R/W	Enable Polarity H-inversion only mode	0
4	POL_H_VAL	R/W	Polarity H-inversion only mode initial value	0
3-0	POL_STEP	R/W	TCPOL direct mode 16 step control	0h

0x0A3D – Direct Mode TRSP Step Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	---
5-0	TRSP_STEP	R/W	Direct Mode TRSP 64 Step Control	0h

0x0A3F – Delta RGB Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	-	Reserved	---
4	LINE_CON	R/W	Delta RGB Line Control	0
3-2	SYNC_CON	R/W	Delta RGB Sync Control	0
1	DELTA_LINE_CON	R/W	0 : Odd Line Mix, 1 : Even Line Mix	0
0	DELTA_LINE_EN	R/W	Enable DELTA RGB Line Mix	0

LCDC – Input Measurement

0x0B00 ~ 0x0B01 Measurement Window Horizontal Start [10:0]

0x0B00 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 – 0	MEA_WIN_H_ST [10:8]	R/W	Input Measurement Window definition: Horizontal Start - high	0

0x0B01 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	MEA_WIN_H_ST [7:0]	R/W	Input Measurement Window definition: Horizontal Start - low	20h

0x0B02 ~ 0x0B03 Measurement Window Horizontal Length [11:0]

0x0B02 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 4	Reserved	-	Reserved	0
3 – 0	MEA_WIN_H_LEN [11:8]	R/W	Input Measurement Window definition: Horizontal Length - high	1

0x0B03 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	MEA_WIN_H_ST [7:0]	R/W	Input Measurement Window definition: Horizontal Length - low	E0h

0x0B04 ~ 0x0B05 Measurement Window Vertical Start [10:0]

0x0B04 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 – 0	MEA_WIN_V_ST [10:8]	R/W	Input Measurement Window definition: Vertical Start - high	0

0x0B05 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	MEA_WIN_V_ST [7:0]	R/W	Input Measurement Window definition: Horizontal Start - low	20h

0x0B06 ~ 0x0B07 Measurement Window Vertical Length [10:0]

0x0B06 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 3	Reserved	-	Reserved	0
2 – 0	MEA_WIN_V_LEN [10:8]	R/W	Input Measurement Window definition: Verticall Length - high	0

0x0B07 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	MEA_WIN_V_ST [7:0]	R/W	Input Measurement Window definition: Vertical Length - low	DAh

0x0B08 – Measurement Input Selection, Measurement Start Register

Bit	Function	R/W	Description	Reset
7 – 6	MEAS_SEL	R/W	Measurement input selection 0,1 = Main path 2: PIP 3: PIP2	0
5 – 4	Reserved	R/W	Reserved	0
3 – 2	FIELD_SEL	R/W	Field Select for Input Measurement 0 = Odd field only 1 = Even field only 2,3 = Disregard field	0
1	RDLOCK	R/W	Lock the data while reading out	-
0	STARTM	R/W	STARTM Start Input Measurement. This bit is self-cleared after the measurement is done.	0

0x0B09 – Measurement Option, Input Change Detection Register

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	-
6 – 4	NOISE_MASK	R/W	Noise mask bits for each of the 3 LSB input signals.	0
3 – 1	ERR_TOLER	R/W	Error Tolerance before asserting “Change Detected” status 000: Exact match 001: Up to 4 counts 0 10: Up to 8 counts 011: Up to 16 counts 100: Up to 32 counts 101: Up to 64 counts 110: Up to 128 counts 111: Up to 256 counts.	0
0	ENDET	R/W	ENDET Enable Input VSYNC, HSYNC Period Change/Loss Detection. When this bit is set, the internal circuitry will perform new measurements. The new results are compared against the results retained in the registers obtained by the most recent “startm” measurement.	0

0x0B0A – Measurement Option Register

Bit	Function	R/W	Description	Reset
7 – 4	THRESHOLD_FOR_ACT_DET	R/W	Threshold value for input active region detection. Each increment increases the threshold value by 16.	3
3	ENALU	R/W	Enable luminance measurement.	0
2 – 1	NOFSEL	R/W	Noise filter selection for luminance measurement.	0
0	DE_MEA	R/W	DE Measurement Enable.	0

0x0B10 ~ 0x0B13 Phase_R Registers

0x0B10 – Byte 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_R_B3	R/W	Phase measurement result - Red	0

0x0B11 – Byte 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_R_B2	R/W	Phase measurement result - Red	0

0x0B10 – Byte 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_R_B1	R/W	Phase measurement result - Red	0

0x0B13 – Byte 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_R_B0	R/W	Phase measurement result - Red	0

0x0B14 ~ 0x0B17 Phase_G Registers

0x0B14 – Byte 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_G_B3	R/W	Phase measurement result - Green	0

0x0B15 – Byte 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_G_B2	R/W	Phase measurement result - Green	0

0x0B16 – Byte 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_G_B1	R/W	Phase measurement result - Green	0

0x0B17 – Byte 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_G_B0	R/W	Phase measurement result - Green	0

0x0B18 ~ 0x0B1B Phase_B Registers

0x0B18 – Byte 3 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_B_B3	R/W	Phase measurement result - Blue	0

0x0B19 – Byte 2 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_B_B2	R/W	Phase measurement result - Blue	0

0x0B1A – Byte 1 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_B_B1	R/W	Phase measurement result - Blue	0

0x0B1B – Byte 0 Register

Bit	Function	R/W	Description	Reset
7 – 0	PHASE_B_B0	R/W	Phase measurement result - Blue	0

0x0B1C – Minimum_R Register

Bit	Function	R/W	Description	Reset
7 – 0	MIN_R	R/W	Minimum measured red value	0

0x0B1D – Minimum_G Register

Bit	Function	R/W	Description	Reset
7 – 0	MIN_G	R/W	Minimum measured green value	0

0x0B1E – Minimum_B Register

Bit	Function	R/W	Description	Reset
7 – 0	MIN_B	R/W	Minimum measured blue value	0

0x0B1F – Maximum_R Register

Bit	Function	R/W	Description	Reset
7 – 0	MAX_R	R/W	Maximum measured red value	0

0x0B20 – Maximum_G Register

Bit	Function	R/W	Description	Reset
7 – 0	MAX_G	R/W	Maximum measured green value	0

0x0B21 – Maximum_B Register

Bit	Function	R/W	Description	Reset
7 – 0	MAX_B	R/W	Maximum measured blue value	0

0x0B22 ~ 0x0B23 Vertical Period Registers

0x0B22 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PERIOD [15:8]	R/W	Vertical period measured	0

0x0B23 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PERIOD [7:0]	R/W	Vertical period measured (in unit of input hsync)	0

0x0B24 ~ 0x0B25 Horizontal Period Registers

0x0B24 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_PERIOD [15:8]	R/W	Horizontal period measured	0

0x0B25 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_PERIOD [7:0]	R/W	Horizontal period measured (in unit of 27 MHz clock)	0

0x0B26 ~ 0x0B27 Hsync Rise to Fall Registers

0x0B26 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_RISE_TO_FALL [15:8]	R/W	Input Hsync rising edge to falling edge	0

0x0B27 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_RISE_TO_FALL [7:0]	R/W	Input Hsync rising edge to falling edge (in unit of input clock)	0

0x0B28 ~ 0x0B29 Hsync Rise to Horizontal Active End

0x0B28 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_RISE_TO_ACT_END [15:8]	R/W	Input Hsync rising edge to input horizontal active end	0

0x0B29 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_RISE_TO_ACT_END [7:0]	R/W	Input Hsync rising edge to input horizontal active end (in unit of input clock)	0

0x0B2A ~ 0x0B2B Vsync High Width Registers

0x0B2A – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PULSEW [15:8]	R/W	Input Vsync (logic) high width	0

0x0B2B – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PULSEW [7:0]	R/W	Input Vsync (logic) high width (in unit of input hsync)	0

0x0B2C ~ 0x0B2D Vsync Rise Position Registers

0x0B2C – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_RISE_PCNT [15:8]	R/W	Input Vsync rising edge position in one input hsync period	0

0x0B2D – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_RISE_PCNT [7:0]	R/W	Input Vsync rising edge position in one input hsync period (in unit of input clock)	0

0x0B2E ~ 0x0B2F Horizontal Active Starting Pixel Position I Registers

0x0B2E – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_ST_MIN[15:8]	R/W	Horizontal active region starting position	0

0x0B2F – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_ST_MIN[7:0]	R/W	Horizontal active region starting position (in unit of input clock)	0

0x0B30 ~ 0x0B31 Horizontal Active Starting Pixel Position II Registers

0x0B30 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_ST_MAX [15:8]	R/W	Horizontal active region starting position	0

0x0B31 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_ST_MAX [7:0]	R/W	Horizontal active region starting position (in unit of input clock)	0

0x0B32 ~ 0x0B33 Horizontal Active Ending Pixel Position I Registers

0x0B32 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_END_ MIN [15:8]	R/W	Horizontal active region ending position	0

0x0B33 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_END_ MIN [7:0]	R/W	Horizontal active region ending position (in unit of input clock)	0

0x0B34 ~ 0x0B35 Horizontal Active Ending Pixel Position II Register

0x0B34 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_END_ MAX [15:8]	R/W	Horizontal active region ending position	0

0x0B35 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_ACT_END_ MAX [7:0]	R/W	Horizontal active region ending position (in unit of input clock)	0

0x0B36 ~ 0x0B37 Vertical Active Starting Line I Registers

0x0B36 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_ST_1 [15:8]	R/W	Vertical active starting line number	0

0x0B37 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_ST_! [7:0]	R/W	Vertical active starting line number (in unit of input hsync)	0

0x0B38 ~ 0x0B39 Vertical Active Starting Line II Registers

0x0B38 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_ST_2 [15:8]	R/W	Vertical active starting line number	0

0x0B39 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_ST_2 [7:0]	R/W	Vertical active starting line number (in unit of input hsync)	0

0x0B3A ~ 0x0B3B Vertical Active Ending Line I Registers

0x0B3A – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_END_1 [15:8]	R/W	Vertical active ending line number	0

0x0B3B – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_END_! [7:0]	R/W	Vertical active ending line number (in unit of input hsync)	0

0x0B3C ~ 0x0B3D Vertical Active Ending Line II Registers

0x0B3C – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_END_2 [15:8]	R/W	Vertical active ending line number	0

0x0B3D – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_ACT_END_2 [7:0]	R/W	Vertical active ending line number (in unit of input hsync)	0

0x0B3E ~ 0x0B3F FIFO Read Starting Position Registers

0x0B3E – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_PCNT_FIFO_RD_ST [15:8]	R/W	FIFO read starting position	0

0x0B3F Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	H_PCNT_FIFO_RD_ST [7:0]	R/W	FIFO read starting position	0

0x0B40 – Liminance Value – Minimum Register

Bit	Function	R/W	Description	Reset
7 – 0	LUM_MIN	R/W	Minimum measured luminance value	0

0x0B41 – Liminance Value – Maximum Register

Bit	Function	R/W	Description	Reset
7 – 0	LUM_MAX	R/W	Maximum measured luminance value	0

0x0B42 – Liminance Value – Average Register

Bit	Function	R/W	Description	Reset
7 – 0	LUM_AVE	R/W	Average measured luminance value	0

0x0B43 ~ 0x0B45 Vertical Period in 27 MHz Registers

0x0B43 – High Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PERIOD_27 MH [23:16]	R/W	Vertical period measured using 27 MHz clock	0

0x0B44 – Mid Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PERIOD_27 MH [15:8]	R/W	Vertical period measured using 27 MHz clock	0

0x0B45 – Low Byte Register

Bit	Function	R/W	Description	Reset
7 – 0	V_PERIOD_27 MH [7:0]	R/W	Vertical period measured using 27 MHz clock	0

LCDC – DDR Memory Control

0x0C00 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved			-
5	DDR_DQS_SEL0[5]	R/W	1: Select delay line for DQS delay, 0: Select DLL for DQS delay	0
4-0	DDR_DQS_SEL0[4:0]	R/W	When [5] = 1, [1:0] specify delay by delay line, 0 : 0.5ns, 1 : 0.75ns, 2 : 1.00ns, 3 : 1.25ns When [5] = 0, [4:0] specify delay by DLL. 1 unit is 1/32 phase delay.	00

0x0C01 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved			-
5	DDR_DQS_SEL1[5]	R/W	1: Select delay line for DQS delay, 0: Select DLL for DQS delay	0
5-0	DDR_DQS_SEL1[4:0]	R/W	When [5] = 1, [1:0] specify delay by delay line, 0 : 0.5ns, 1 : 0.75ns, 2 : 1.00ns, 3 : 1.25ns When [5] = 0, [4:0] specify delay by DLL. 1 unit is 1/32 phase delay.	00

0x0C02 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7-5	DDR_CLKO_SEL	R/W	Memory clock output selection (only for FPGA)	1
4-0	DDR_CLK90_SEL	R/W	Select the phase of 90 degree CLK generated by DLL. The phase is DDR_CLK90_SEL/32	08

0x0C03 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7-4	DLL_TST_SEL	R/W	Select the DLL test output signal	0
3	Reserved			-
2	DLL_TST	R/W	1: Bypass all DLL or delay line	0
1-0	DLL_TAP_S	R/W	Select the DLL TAPS	0

0x0C04 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	DLL_RSTN	R/W	Software reset only for DLL (self return to 0)	0
6-0	Reserved	R/W		-

0x0C05 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	RD_PH	R/W	Select DQS or ~DQS as read clock to latch DQ	0
6-4	Reserved			-
3-2	DDR_DQS_DLY	R/W	Select DQS valid read data cycle delay number	2
1-0	DDR_WRNOP	R/W	DDR read to write address additional NOP cycles	0

0x0C06 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7-4	DDR_T_RC	R/W	T_rc timing	A
3-0	DDR_T_RAS	R/W	T_ras timing	7

0x0C07 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7-4	DDR_T_RFC	R/W	T_rfc timing	B
3	Reserved			-
2-0	DDR_T_RP	R/W	T_rp timing	4

0x0C08 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	Reserved			-
6-4	DDR_T_RCD	R/W	T_rcd timing	4
3	Reserved			-
2-0	DDR_T_WR	R/W	T_wr timing	3

0x0C09 – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	Reserved			-
6-4	DDR_REFRESH	R/W	DDR refresh timing control	0
3	INIT_BYP		DDR initialization bypass (1: for simulation)	0
2-0	DDR_B_LENGTH	R/W	DDR burst length	3

0x0C0A – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	DDR_TST	R/W	1: Bypass all DLL or delay line	0
6-4	DDR_CAS_LAT	R/W	DDR CAS latency	7
3	SAMSNG	R/W	Internal test mode	0
2-0	Reserved	R/W		-

0x0C0B – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	DDR_WTR	R/W	1: DDR write to read turn around cycle needed, 0: No turn around cycle	0
6	DDR_BTYP	R/W	External DDR burst type (for initialization purpose)	0
5	DDR_DVST	R/W	Configure external DDR driving strength (for initialization purpose)	0
4	DLL_EN	R/W	Enable DLL in the external DDR memory (for initialization purpose)	1
3	Reserved			-
2-0	DDR_SIZE	R/W	DDR size	1

0x0C0C – DDR Memory Control Register

Bit	Function	R/W	Description	Reset
7	DDR_RSTN	R/W	Software reset only for DDR logic (Auto return to 0)	0
6-0	Reserved	R/W		-

LCDC – Aux Control

0x0CF0 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-0	AUX_RWDAT	R/W	Read/Write data to/from DDR	00

0x0CF1 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7	FIFO_RST	R/W	1: Read/Write FIFO reset, self clear	0
6-2	Reserved	R/W		-
1	FIFO_EMPTY	R	1: FIFO status is empty	1
0	FIFO_FULL	R	1: FIFO status is full	0

0x0CF2 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-0	AUX_ADDR[23:16]	R/W	Address for burst read/write to/from DDR	00

0x0CF3 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-0	AUX_ADDR[15:8]	R/W	Address for burst read/write to/from DDR	00

0x0CF4 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-0	AUX_ADDR[7:0]	R/W	Address for burst read/write to/from DDR	00

0x0CF5 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved			-
7-0	AUX_LENGTH [10:8]	R/W	Length of the burst read/write to/from DDR. The maximum length is 1024.	00

0x0CF6 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-0	AUX_LENGTH [7:0]	R/W	Length of the burst read/write to/from DDR. The maximum length is 1024.	00

0x0CF7 – DDR Direct R/W Control Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	R/W		-
1	AUX_RD	R/W	DDR read command (self cleared)	0
0	AUX_WR	R/W	DDR write command (self cleared)	0

CCFL and LEDC Control

0x0D0 – CCFL/LED Control I

Bit	Function	R/W	Description	Reset
7-1	Reserved	-	Reserved	-
0	BIASCTL	R/W		0

0x0D01 – CCFL/LED Control I

Bit	Function	R/W	Description	Reset
7	OVEN	R/W	CCFL over voltage feedback control 0 = disable 1 = enable	1
6	OIEN	R/W	CCFL over current feedback control 0 = disable 1 = enable	1
5	UIEN	R/W	CCFL under current feedback control 0 = disable 1 = enable	1
4	FBEN	R/W	CCFL feedback loop control 0 = open loop 1 = close loop	1
3	LOCKV	R/W	CCFL Dimming frequency 0 = set by FDIM 1 = locked to panel vertical sync	0
2	LOCkH	R/W	CCFL PWM frequency 0 = set by FPWM 1 = locked to panel horizontal frequency	0
1	CCFLENB	R/W	CCFL analog sense 0 = power down 1 = power up.	1
0	CCFLDEN	R/W	CCFL out 0 = disable. 1 = enable.	0

0x0D02 – CCFL Threshold and LEDC Control

Bit	Function	R/W	Description	Reset
7-6	LVT	R/W	CCFL lamp voltage threshold	2
5-4	LILT	R/W	CCFL lamp low current threshold	2
3-0	LIT / VFB_VOP	R/W	CCFL lamp normal current threshold or LEDC VFB / VOP selection When CCFL_LEDC_DEN set to 0, this is Lamp normal current threshold. When CCFL_LEDC_DEN set to 1, bits[3:2] is feedback reference voltage selection (VFB) and bits[1:0] is voltage overdrive protection selection(VOP). VFB : 00 = 0.7V, 01= 0.55V, 10= 0.4V, 11= 0.25V VOP : 00= 0.7V, 01 = 0.55V, 10= 0.4V, 11= 0.25V	D

0x0D03 – CCFL/LED Control II

Bit	Function	R/W	Description	Reset
7	LED_DIG_EN	R/W	LEDC Digital 0 = disable 1 = enable	0
6	LEDC_ APDWN	R/W	LEDC Analog Block Power Down 0 = Normal 1 = Power Down	0
5-4	CC_LED_ST	R/W	CCFL or LEDC status	0
3-0	LSTP	R/W	CCFL or LEDC feedback gain control with 1 being the smallest gain.	4

0x0D04 – CCFL/LEDC PWM

Bit	Function	R/W	Description	Reset
7-0	FPWM	R/W	CCFL PWM control frequency FPWM[7:0] : CCFL PWM (6..75MHz / Fpwm) FPWM[6:0] : LED PWM (13.5MHz / Fpwm)	70

0x0D05 – CCFL/LED Dim Frequency

Bit	Function	R/W	Description	Reset
7-0	FDIM	R/W	CCFL or LEDC Dimming frequency control. Freq = 13.18KHz / Fdim	84

0x0D06 – CCFL/LED Dim Control

Bit	Function	R/W	Description	Reset
7	Reserved	-	Reserved	-
6-0	DDIM	R/W	CCFL or LEDC Dimming control. 0 = full brightness, 7F = lowest brightness	00

0x0D07 – CCFL/LED PWMTOP

Bit	Function	R/W	Description	Reset
7-0	PWMTOP	R/W	CCFL or LEDC PWM TOP / Min out	04

0x0D10 – Control Signal Generation Method Register (Logic level: 1.8V)

Bit	Function	R/W	Description	Relative Pin	Reset
7	PD	R/W	ADC power down. Start with power down mode		1
6	RST	R/W	ADC RESET. Pusle needs to be longer than 1clk cycle		0
5	START	R/W	ADC START. Pusle needs to be longer than 1clk cycle		0
4	PEN_IRQ	R/W	Pen Interrupt Detect		0
3	RDY_IRQ	R/W	Ready Interrupt Detect		0
2:0	A<2:0>	R/W	Mode selection 000 X position measurement 001 Z1 010 Z2 011 Y position measurement 100 Auxiliary 0 101 Auxiliary 1 110 Auxiliary 2 111 Auxiliary 3		000

Touch Screen Control

0x0D11 – Control Signal Generation Method Register (Logic level: 1.8V)

Bit	Function	R/W	Description	Relative Pin	Reset
7	RDYINT_ENB	R/W	Ready Interrupt enable. To activate the interrupt, program PD=0 and RDYINT_ENB=1		0
6	PENINT_ENB	R/W	PEN Interrupt enable. To activate the interrupt, program PD=0 and PENINT_ENB=1		0
5:3	R_SEL<2:0>	R/W	R selection for touch detection sensitivity 000: 150k, 001: 130K, 010: 110k, 011: 90k 100: 70k, 101: 50K, 110: 30k, 111: 10k		000
2-0	TEST_ADC	R/W	ADC test mode control 000: disable 001: disable 010: disable 011: disable 100: buffered internal comparator input 101: vmid 110: comp out 111: regen clock		000

0x0D12 – TSC ADC Data Output

Bit	Function	R/W	Description	Relative Pin	Reset
7:0	TCS_ADOUT	R/W	TSC_OUT[11:4]		0

0x0D13 – TSC ADC Data Output

Bit	Function	R/W	Description	Relative Pin	Reset
7:4	-	-	-	-	-
3:0	TCS_ADOUT	R/W	TSC_OUT[3:0]		0

0x0D14 – TSC Start and Clock

Bit	Function	R/W	Description	Relative Pin	Reset
3	CONTi_SMP	R/W	0: Start by Register Command 1: Continuous Sample for TSC ADC regardless of register START signal		0
2:0	TCS_CKSEL	R/W	Divided Factor for TSC ADC Clock 0 : Divide by 2 1 : Divide by 4 2 : Divide by 8 3 : Divide by 16 4 : Divide by 32 5 : Divide by 64 6 : Divide by 128 7 : Divide by 256		0

0x00 –ADC Output Read Only Register (Logic level: 1.8V)

Bit	Function	R/W	Description	Relative Pin	Reset
16:4	ADC Output	R	ADC Output bit<16>: MSB, bit<4> LSB		0
3:0	Filler	R	Not used, assigned to zero		0

Note: this read only register is implemented on the top level of this analog IP. The raw data will be read and placed in this register.

LVDS Configuration Registers

0xD40 – Mode 1 Setting Register

Bit	Function	R/W	Description	Reset
7-5	CTL_MAPSEL	R/W	Control Signal Order in serial data sequence out 3'b000 : {de, vsync, hsync}; 3'b001 : {vsync, hsync, de}; 3'b010 : {hsync, de, vsync}; 3'b100 : {de, hsync, vsync}; 3'b101 : {hsync, vsync, de}; 3'b110 : {vsync, de, hsync}; default : {de, vsync, hsync};	0
4-3	BIT_PERPIX	R/W	Bit per Pixel of Data bus 00: 3bit, 01 : 4bit, 10 : 5bit, 11: reserved	0
2	LVDS_OP	R/W	LVDS operation 0 : LVDS no operation (TCON selected) 1 : LVDS operation	0
1	FAB_TST	R/W	LVDS test mode 0 : Normal operation mode 1 : LVDS test mode	0
0	LCD_TST	R/W	LCD Panel test mode 0 : Normal operation mode 1 : LCD Panel test mode	0

0xD41 – Mode 2 Setting Register

Bit	Function	R/W	Description	Reset
7	RD_SH	R/W	Road/Shift signal polarity selection 0 : active low 1 : active high	0
6	SWAP_CH	R/W	Channel Swap In Dual Channel LVDS	0
5	MX_REV_DCB	R/W	Reverse DC Balance for Maxim Mode	0
4	REV_BIT	R/W	Reversed data output 0 : Normal data output format 1 : Reversed data output format	0
3	DCB_POL	R/W	DC Balance Polarity	0
2	DC_BAL	R/W	DC Balance Enable	0
1	DUAL_CH	R/W	Dual Channel Enable	0
0	MAXIM_SEL	R/W	Output mapping 1 : Output data mapping same as Maxim or THine LVDS interface protocols. 0 : Output data mapping same as National Semiconductor interface protocols.	0

0xD42 – Mode 3 Setting Register

Bit	Function	R/W	Description	Reset
7-6	CP_SEL	R/W	Charge Pump Control	00
5-4	LP_SEL	R/W	Low Pass Filter Control	00
3	-	R/W	Reserved	0
2	-	R/W	Reserved	0
1-0	SEL_LVDS	R/W	LVDS Type Selection	00

REMOCON_RX

0xDA0 – REMOCON CONTROL0

Bit	Function	R/W	Description	Reset
6	REMPOL	R/W	Polarity inverse of IRRX pin input signal 1 : inverse 0 : non-inverse	0x1
5-1	HTREF	R/W	HT6230 type REMOCON signal clock generation reference. Typical value is 0x13 and some HT6230 type REMOCON is 0x12.	0x13
0	HTINI[8]	R/W	HT6230 data sample start timing.	0x0

0xDA1 – REMOCON CONTROL1

Bit	Function	R/W	Description	Reset
7-0	HTINI[7:0]	R/W	HT6230 data sample start timing.	0xB0

0xDA2 – REMOCON ENABLE

Bit	Function	R/W	Description	Reset
0	REMEN	R/W	REMOCON receiver enable signal 1 : enable, 0 : diabale	0x0

0xDA3 – REMOCON INTERRUPT

Bit	Function	R/W	Description	Reset
3	REMERROR_ Flag	R/W	1 : There are some errors during receiving REMOCON data or Non-supported REMOCON data received. 0 : The other case. * Cleared by writing '1'	0
2	UPDLINT_Flag	R/W	1 : uPD type REMOCON's "kept depressed" signal(keep pushing same button signal) is received without command data. 0 : The other case * Cleared by writing '1'	0
1	UPDINT_Flag	R/W	1 : uPD type REMOCON data is received. 0 : The other case. * Cleared by writing '1'	0
0	HTINT_Flag	R/W	1 : HT type REMOCON data is received. 0 : The other case. * Cleared by writing '1'	0

0xDA4 – HTSYSTEM

Bit	Function	R/W	Description	Reset
5	HTCONTROL	R	1 control bits from HT6230 type REMOCON signal input	
4-0	HTSYSTEM	R	5 system bits from HT6230 type REMOCON signal input	

0xDA5 – HTCOMMAND

Bit	Function	R/W	Description	Reset
5-0	HTCOMMAND	R	6 command bits from HT6230 type REMOCON signal input	

0xDA6 – UPDREG3

Bit	Function	R/W	Description	Reset
7-0	UPDREG[31:24]	R	4th received byte from uPD type REMOCON signal input. It is inversion data code.	

0xDA7 – UPDREG2

Bit	Function	R/W	Description	Reset
7-0	UPDREG[23:16]	R	3rd received byte from uPD type REMOCON signal input. It is data code.	

0xDA8 – UPDREG1

Bit	Function	R/W	Description	Reset
7-0	UPDREG[15:8]	R	2nd received byte from uPD type REMOCON signal input. It is custom code2.	

0xDA9 – UPDREG0

Bit	Function	R/W	Description	Reset
7-0	UPDREG[7:0]	R	1st received byte from uPD type REMOCON signal input. It is custom code.	

0xDAA – REMPI

Bit	Function	R/W	Description	Reset
0	REMPI	R	IRRX pin input signal for REMOCON receiver software.	

0xDAB – REMCLKREF

Bit	Function	R/W	Description	Reset
7-0	REMCLKREF[15:8]	R/W	Upper byte REMCLKREF	0x00

0xDAC – REMCLKREF

Bit	Function	R/W	Description	Reset
7-0	REMCLKREF[7:0]	R/W	Lower byte REMCLKREF	0x27

0xDAD – UPDHTEN

Bit	Function	R/W	Description	Reset
3	UPDEN	R/W	NEC type IR receiver enable	0x1
2	HTEN	R/W	HT type IR receiver enable	0x1
1-0	USAMPLE[9:8]	R/W	MSB 2bits of uPD REMOCON data sample timing value.	0x0

0xDAE – USAMPLE

Bit	Function	R/W	Description	Reset
7-0	USAMPLE[7:0]	R/W	LSB 8bits of uPD REMOCON data sample timing value.	0x1B

0xDAF – ULLEADER

Bit	Function	R/W	Description	Reset
1-0	ULLEADER[9:8]	R/W	MSB 2 bits of uPD REMOCON Leader code low period control value	0x0

0xDB0 – ULLEADER

Bit	Function	R/W	Description	Reset
7-0	ULLEADER[7:0]	R/W	LSB 8 bits of uPD REMOCON Leader code low period control value	0x36

0xDB1 – UHLEADER

Bit	Function	R/W	Description	Reset
1-0	UHLEADER[9:8]	R/W	MSB 2 bits of uPD REMOCON Leader code high period control value	0x0

0xDB2 – UHLEADER

Bit	Function	R/W	Description	Reset
7-0	UHLEADER[7:0]	R/W	LSB 8 bits of uPD REMOCON Leader code high period control value	0x36

LCDC – LOPOR

0xDC0 – LSO Power Down Register

Bit	Function	R/W	Description	Reset
7-1	Reserved	-	Reserved	0
0	PD_LSO	R/W	Power Down for LSO	0

0xDC1 – POR Power Down Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	-	Reserved	0
1	DIS_DLY	R/W	Disable Delay Count for POR	0
0	PD_POR	R/W	Power Down for POR	0

LCDC – PLL (Panel Clock)

0x0DD0 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 5	IP_P	R/W	Charge Pump Current Control for PCLK	4
4	EDGE_SEL_P	R/W	Edge Select for pclk SSPLL	0
3 - 0	FREQ_P[19:16]	R/W	PCLK Oscillation frequency calculation FREQ_P[19:16]. Total 20bits. PCLK PLL Oscillation frequency = 108MHz * FREQ_P / 2 ^ 17 / 2^ POST_P	0

0x0DD1 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 0	FREQ_P[15:8]	R/W	FREQ_P[15:8]	00

0x0DD2 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 0	FREQ_P[7:0]	R/W	FREQ_P[7:0]	00

0x0DD3 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 0	SSFREQ_P[7:0]	R/W	PCLK spread spectrum modulation frequency SSFREQ_P[7:0] Spread spectrum modulation frequency = 27MHz * SSFREQ_P / 2^16	00

0x0DD4 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 4	SSG_P[3:0]	R/W	PCLK variance of spread spectrum. SSG_P[3:0] Frequency Deviation Control for PCLK : The Max percentage of frequency deviation is given by following equation. DEV = 2^8 * SSG_P / 2^SSD / 2^FREQ_P * 100 %	0
3 - 2	VCO_P	R/W	PCLK VCO[1:0] 0 = 13.5 ~ 27MHz, 1 = 27 ~ 54 MHz 2 = 54 ~ 108MHz, 3 = 108 ~ 133MHz	0
1 - 0	POST_P	R/W	PCLK POST[1:0]	0

0x0DD5– PLL Control Register

Bit	Function	R/W	Description	Reset
7	PD_P	R/W	Freq. Synthesizer Power down for PCLK 0 = Normal Operation 1 = Off	0
6	Reserved	-	Reserved	-
5 - 4	CPX4_P	R/W	CP_X4 for PCLK SSPLL	0
3 - 2	LPX4_P	R/W	LP_X4 for PCLK SSPLL	0
1 - 0	LPX8_P	R/W	LP_X8 for PCLK SSPLL	0

0x0DD6– PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 6	Reserved	-	Reserved	-
5 - 3	Reserved	-	Reserved	0
2 - 0	DGAIN_P	R/W	DGain for Panel Clock PLL	0

LCDC – PLL (Memory Clock)

0x0DD8 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 5	IP_M[2:0]	R/W	Charge Pump Current Control for MCLK	0
4	EDGE_SEL_M	R/W	Edge Select for mclk SSPLL	0
3 - 0	FREQ_M[19:16]	R/W	MCLK Oscillation frequency calculation FREQ_M[19:16]. Total 20 bits. MCLK PLL Oscillation frequency = 108MHz * FREQ_M / 2 ^ 17 / 2^ POST_M	0

0x0DD9 – PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 0	FREQ_M[15:8]	R/W	FREQ_M[15:8]	00

0x0DDA– PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 0	FREQ_M[7:0]	R/W	FREQ_M[7:0]	00

0x0DDB– PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 0	SSFREQ_M[7:0]	R/W	MCLK spread spectrum modulation frequency. SSFREQ_M[7:0] Spread spectrum modulation frequency = 27MHz * SSFREQ_M / 2^16	00

0x0DDC– PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 4	SSG_M[3:0]	R/W	MCLK variance of spread spectrum. SSG_M[3:0] Frequency Deviation Control for MCLK : The Max percentage of frequency deviation is given by following equation. DEV = 2^8 * SSG_M / 2^SSD / 2^FREQ_M * 100 %	0
3 - 2	VCO_M	R/W	MCLK VCO[1:0] 0 = 13.5 ~ 27MHz, 1 = 27 ~ 54 MHz 2 = 54 ~ 108MHz, 3 = 108 ~ 133MHz	0
1 - 0	POST_M	R/W	MCLK POST[1:0]	0

0x0DDD– PLL Control Register

Bit	Function	R/W	Description	Reset
7	PD_M	R/W	Freq. Synthesizer Power down for MCLK 0 = Normal Operation 1 = Off	0
6	Reserved	-	Reserved	
5 - 4	CPX4_M	R/W	CP_X4 for MCLK SSPLL	0
3 - 2	LPX4_M	R/W	LP_X4 for MCLK SSPLL	0
1 - 0	LPX8_M	R/W	LP_X8 for MCLK SSPLL	0

0x0DDE– PLL Control Register

Bit	Function	R/W	Description	Reset
7 - 6	Reserved	-	Reserved	-
5 - 3	Reserved	-	Reserved	0
2 - 0	DGAIN_M	R/W	DGain for Memory Clock PLL	0

LCDC – DAC

0x0DE0– DAC Control Register

Bit	Function	R/W	Description	Reset
7-4	DACGAIN	R	DAC GAIN Control.	0
3-1	DAC_VCM	R/W	DAC output common mode voltage selection. 000 = 1.0 V 001 = 1.25 V 010 =1.375 V 011 = 1.625 V 100 = 2.0 V 101 = 2.50 v 110 = Not supported 111 = Not supported	0
0	DACPD	R/W	DAC Power Down	0

MCU

0x0F00 – SPI Flash Mode Control Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	-	Reserved	-
2-0	SPI_MODE	R/W	SPI Flash Read Mode 000:slow, 001:fast, 010:dual, 011:quad, 100:dual-io, 101:quad-io	000

0x0F01 – MCU Clock Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	-	Reserved	-
5-4	MCU_CK_SEL	R/W	MCU clock selection 0=system clock (27MHz) 1=internal R-C oscillator (32KHz) 2=PCLK 3=reserved	00
3	Reserved	R/W	Reserved	-
2-0	MCU_CK_DIV	R/W	PLL clock divider 0=1.0 (108MHz) 1=1.5 (72MHz) 2=2.0 (54MHz) 3=2.5 (43.2MHz) 4=3.0 (36MHz) 5=3.5 (30.8MHz) 6=4.0 (27MHz) 7=5.0 (13.5MHz)	110

0x0F02 – SPI Clock Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-4	SPI_CK_SEL	R/W	SPI clock selection 0=system clock (27MHz) 1=internal R-C oscillator (32KHz) 2=PCLK 3=reserved	00
3	Reserved	R/W	Reserved	-
2-0	SPI_CK_DIV	R/W	PLL clock divider 0=1.0 (108MHz) 1=1.5 (72MHz) 2=2.0 (54MHz) 3=2.5 (43.2MHz) 4=3.0 (36MHz) 5=3.5 (30.8MHz) 6=4.0 (27MHz) 7=5.0 (13.5MHz)	110

0x0F03 – DMA Control Register

Bit	Function	R/W	Description	Reset
7	INDEX_SEL	R/W	Read/Write data buffer source/destination 0=default (Reg0xF10) 1=assigned by buffer index	0
6	XMEM_DMA	R/W	Read/Write destination 0=MCU xdata 1=Chip Register	1
5-4	DMA_REG_MODE	R/W	Read/Write access mode 00=Increase 01=Decrease 10=Fix 11=Reserved	00
3	DMA_NONV	R/W	Start mode 0=Immediately 1=At vertical blank	0
2-0	WR_CNT_NUM	R/W	Command write byte count	0

0x0F04 – Flash Busy Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	-
3	Reserved	-	Reserved	0
2	BUSY_CHECK	R/W	Busy check 0=No busy check 1=Busy check after command. Wait until busy is cleared	0
1	WR_MODE	R/W	SPI DMA/CMD Mode 0=Read, 1=Write	0
0	DMA_STR	R/W	Start command execution. Self cleared. Write ‘1’ = Start Write ‘0’ = Stop Read ‘1’ = Busy Read ‘0’ = Ready	0

0x0F05 – Wait Control Register

Bit	Function	R/W	Description	Reset
7-4	DMA_WAIT	R/W	DMA read wait cycle	1000
3-0	SPI_WAIT	R/W	SPI read/write wait cycle	0000

0x0F06 – DMA Page Register

Bit	Function	R/W	Description	Reset
7-0	DMA_REG_PAGE	R/W	Buffer index page or memory start address high byte	06h

0x0F07 – DMA Index Register

Bit	Function	R/W	Description	Reset
7-0	INDEX	R/W	Buffer index or memory start address low byte	00h

0x0F08 – DMA Length Mid Byte Register

Bit	Function	R/W	Description	Reset
7-0	DMA_LENGTH	R/W	Read/Write data count mid byte after command	00h

0x0F09 – DMA Length Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	DMA_LENGTH	R/W	Read/Write data count low byte after command	00h

0x0F0A – DMA Command Buffer1 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG1_RG	R/W	Command buffer 1	00h

0x0F0B – DMA Command Buffer2 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG2_RG	R/W	Command buffer 2	00h

0x0F0C – DMA Command Buffer3 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG3_RG	R/W	Command buffer 3	00h

0x0F0D – DMA Command Buffer4 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG4_RG	R/W	Command buffer 4	00h

0x0F0E – DMA Command Buffer5 Register

Bit	Function	R/W	Description	Reset
7-0	WR_REG5_RG	R/W	Command buffer 5	00h

0x0F0F – Clock Switch Wait Control Register

Bit	Function	R/W	Description	Reset
7-0	CLK_SWITCH_WAIT	R/W	Clock Switch Wait Count	1Fh

0x0F10 – DMA Read/Write Buffer1 Register

Bit	Function	R/W	Description	Reset
7-0	BUF1	R/W	Default Read/write buffer 1	00h

0x0F11 – DMA Read/Write Buffer2 Register

Bit	Function	R/W	Description	Reset
7-0	BUF2	R/W	Default Read/write buffer 2	00h

0x0F12 – DMA Read/Write Buffer3 Register

Bit	Function	R/W	Description	Reset
7-0	BUF3	R/W	Default Read/write buffer 3	00h

0x0F13 – DMA Read/Write Buffer4 Register

Bit	Function	R/W	Description	Reset
7-0	BUF4	R/W	Default Read/write buffer 4	00h

0x0F14 – DMA Read/Write Buffer5 Register

Bit	Function	R/W	Description	Reset
7-0	BUF5	R/W	Default Read/write buffer 5	00h

0x0F15 – DMA Read/Write Buffer6 Register

Bit	Function	R/W	Description	Reset
7-0	BUF6	R/W	Default Read/write buffer 6	00h

0x0F16 – DMA Read/Write Buffer7 Register

Bit	Function	R/W	Description	Reset
7-0	BUF7	R/W	Default Read/write buffer 7	00h

0x0F17 – DMA Read/Write Buffer8 Register

Bit	Function	R/W	Description	Reset
7-0	BUF8	R/W	Default Read/write buffer 8	00h

0x0F18 – SPI Flash Status Command Register

Bit	Function	R/W	Description	Reset
7-0	STATUS_CMD_RG	R/W	Status command	05h

0x0F19 – SPI Flash Busy Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	-	Reserved	-
3	BUSY_POL	R/W	Busy polarity 0=Low 1=High	1
2-0	BUSY_BIT	R/W	Busy bit in status command	000

0x0F1A – DMA Length High Byte Register

Bit	Function	R/W	Description	Reset
7-0	DMA_LENGTH	R/W	Read/Write data count high byte after command	00h

0x0F20 – MCU Control Register

Bit	Function	R/W	Description	Reset
7	MCUEN	R	MCU status 0=Disabled 1=Enabled	-
6	SRST_CHIP	R/W	MCU reset Chip Register	0
5	OSD_DMA	R/W	OSD DMA Enable	0
4	Reserved	R/W	Reserved	-
3	SPI_EN	R/W	SPI Enable 1 : enable, 0 : disable	1
2	CACHE_EN	R/W	Enable MCU code cache 0=disable, 1=enable	0
1	BOOTSEL	R/W	MCU Boot Selection 0=SPI, 1=Internal ROM	0
0	SRST_MCU	R/W	Reset MCU. ISP has to be enabled before set this.	0

0x0F21 – ISP Passcode Register

Bit	Function	R/W	Description	Reset
7-0	ISPEN	R/W	Password for ISP enabling Write 0x55, 0xAA sequentially to enable ISP	00h

0x0F22 – Timer0 Divider High Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT0	R/W	Timer0 Divider High Byte	00h

0x0F23 – Timer0 Divider Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT0	R/W	Timer0 Divider Low Byte	90h

0x0F24 – Timer1 Divider High Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT1	R/W	Timer1 Divider High Byte	00h

0x0F25 – Timer1 Divider Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT1	R/W	Timer1 Divider Low Byte	90h

0x0F26 – Timer2 Divider High Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT2	R/W	Timer2 Divider High Byte	00h

0x0F27 – Timer2 Divider Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT2	R/W	Timer2 Divider Low Byte	90h

0x0F28 – Timer3 Divider High Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT3	R/W	Timer3 Divider High Byte	00h

0x0F29 – Timer3 Divider Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT3	R/W	Timer3 Divider Low Byte	0Ch

0x0F2A – Timer4 Divider High Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	Timer4 Divider High Byte	00h

0x0F2B – Timer4 Divider Low Byte Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	Timer4 Divider Low Byte	0Ch

0x0F2C – OSD DMA Busy Check Delay Register

Bit	Function	R/W	Description	Reset
7-0	OSD_WAIT	R/W	OSD DMA Busy Check Delay	02h

MCU SFR Register

0x9A – Code Bank Address Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	Program Base Address	0

0xFA – Interrupt7~14 Control Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	INT14~INT7 Flag	0

0xFB – Interrupt7~14 Control Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	INT14~INT7 Enable	0

0xFC – Interrupt7~14 Control Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	INT14~INT7 Priority	0

0xFD – Interrupt7~14 Control Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	INT14~INT7 Edge/Level	0

0xFE – Interrupt7~14 Control Register

Bit	Function	R/W	Description	Reset
7-0	RG_DVIDT4	R/W	INT14~INT7 Edge/Level Polarity	0

0xE2 – Cache Control Register

Bit	Function	R/W	Description	Reset
7-2	Reserved	-	Reserved	-
1	RG_PWDN	R/W	Power Down Cache	0
0	Reserved	-	Reserved	-

Interrupt Vector Address

```
*INT7_SUB_ADDR   = 5'b01101;    // 0x6B
*INT8_SUB_ADDR   = 5'b01110;    // 0x73
*INT9_SUB_ADDR   = 5'b01111;    // 0x7B
*INT10_SUB_ADDR  = 5'b10000;    // 0x83
*INT11_SUB_ADDR  = 5'b10001;    // 0x8B
*INT12_SUB_ADDR  = 5'b10010;    // 0x93
*INT13_SUB_ADDR  = 5'b10011;    // 0x9B
*INT14_SUB_ADDR  = 5'b10100;    // 0xA3
```

0x80 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	P0	R/W	Port 0	FFh

0x81 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	SP	R/W	Stack Pointer	07h

0x82 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPL	R/W	Data Pointer 0 Low	00h

0x83 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPH	R/W	Data Pointer 0 High	00h

0x84 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPL1	R/W	Data Pointer 1 Low	00h

0x85 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPH1	R/W	Data Pointer 1 High	00h

0x86 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPS	R/W	Data Pointers Select	00h

0x87 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	PCON	R/W	Power Control	00h

0x88 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TCON	R/W	Timer/Counter Control	00h

0x89 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TMOD	R/W	Timer Mode Control	00h

0x8A – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TL0	R/W	Timer 0, low byte	00h

0x8B – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TL1	R/W	Timer 1, low byte	00h

0x8C – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TH0	R/W	Timer 1, high byte	00h

0x8D – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TH1	R/W	Timer 1, high byte	00h

0x8E – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CKCON	R/W	Clock control	07h

0x90 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	P1	R/W	Port 1	FFh

0x91 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	EIF	R/W	Extended interrupt Flags	00h

0x92 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	WTST	R/W	Program Memory Wait-States	07h

0x93 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPX0	R/W	Data Page Pointer 0	00h

0x95 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	DPX1	R/W	Data Page Pointer 1	00h

0x98 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	SCON0	R/W	UART0 Control	00h

0x99 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	SBUF0	R/W	UART0 Buffer	00h

0xA0 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	P2	R/W	Port 2	00h

0xA8 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	IE	R/W	Interrupt Enable	00h

0xB0 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	P3	R/W	Port 3	FFh

0xB8 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	IP	R/W	Interrupt Priority	00h

0xC0 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	SCON1	R/W	UART1 Control	00h

0xC1 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	SBUF1	R/W	UART1 Buffer	00h

0xC2 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCL1	R/W	Timer2cc compare/capture 1 low byte	00h

0xC3 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCH1	R/W	Timer2cc compare/capture 1 high byte	00h

0xC4 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCL2	R/W	Timer2cc compare/capture 2 low byte	00h

0xC5 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCH2	R/W	Timer2cc compare/capture 2 high byte	00h

0xC6 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCL3	R/W	Timer2cc compare/capture 3 low byte	00h

0xC7 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCH3	R/W	Timer2cc compare/capture 3 high byte	00h

0xC8 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	T2CON	R/W	Timer2cc control	00h

0xC9 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	T2IF	R/W	Timer2cc Interrupt Flag	00h

0xCA – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CRCL	R/W	Timer2cc capture/reload low byte	00h

0xCB – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CRCH	R/W	Timer2cc capture/reload high byte	00h

0xCC – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TL2	R/W	Timer2cc low byte	00h

0xCD – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TH2	R/W	Timer2cc high byte	00h

0xCE – SFR Register

Bit	Function	R/W	Description	Reset
7-0	CCEN	R/W	Timer2cc compare/ capture enable	00h

0xD0 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	PSW	R/W	Program Status Word	00h

0xD8 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	WDCON	R/W	Watchdog Control Register	00h

0xE0 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	ACC	R/W	Accumulator	00h

0xE8 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	EIE	R/W	Extended interrupt enable	00h

0xE9 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	STATUS	R/W	Status register	00h

0xEA – SFR Register

Bit	Function	R/W	Description	Reset
7-0	MXAX	R/W	Address register for MOVX @Ri, A and MOVX A @Ri	00h

0xEB – SFR Register

Bit	Function	R/W	Description	Reset
7-0	TA	R/W	Timed Access protection register	00h

0xF0 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	B	R/W	B Register	00h

0xF8 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	EIP	R/W	Extended interrupt priority	00h

0xF9 – SFR Register

Bit	Function	R/W	Description	Reset
7-0	MD0	R/W	Multiplication / Division Register 0	00h

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Revision History

Date	Revision Note