



STB200N04

N-channel 40V - 0.0035Ω - 120A - D²PAK
Planar STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STB200N04	40V	<0.0040Ω	120A	300W

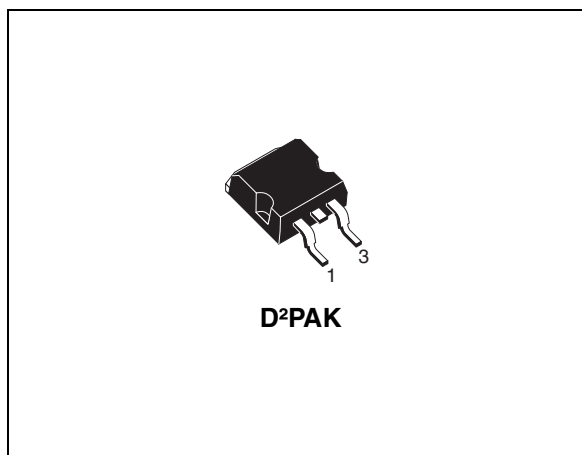
- 100% avalanche tested
- Standard threshold drive

Description

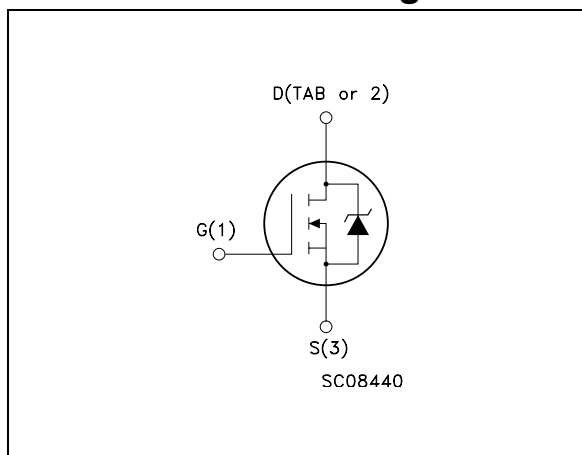
This Power MOSFET is the latest development of STMicroelectronics unique “single feature size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility. This new improved device has been specifically designed for automotive applications.

Applications

- Switching application
 - Automotive



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB200N04	B200N04	D ² PAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	862	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	4.2	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 60\text{A}$, $V_{DD} = 25\text{V}$
4. $I_{SD} \leq 60\text{A}$, $di/dt \leq 440\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.50	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board, 1inch² 2 oz Cu

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 80A$		0.0035	0.0040	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 80A$		200		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		5100 1270 37		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20V, I_D = 120A$ $V_{GS} = 10V$ (see Figure 13)		75 23 17		nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=20\text{ V}$, $I_D=60\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 12)		19 180		ns ns
$t_{d(off)}$ t_f	Off-voltage rise time Fall time	$V_{DD}=20\text{ V}$, $I_D=60\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 12)		90 65		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD}	Source-drain current				120	A
I_{SDM}	Source-drain current (pulsed)				480	A
V_{SD}	Forward on voltage	$I_{SD}=120\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=120\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 17)		67		ns
Q_{rr}	Reverse recovery charge			130		nC
I_{RRM}	Reverse recovery current			4		A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

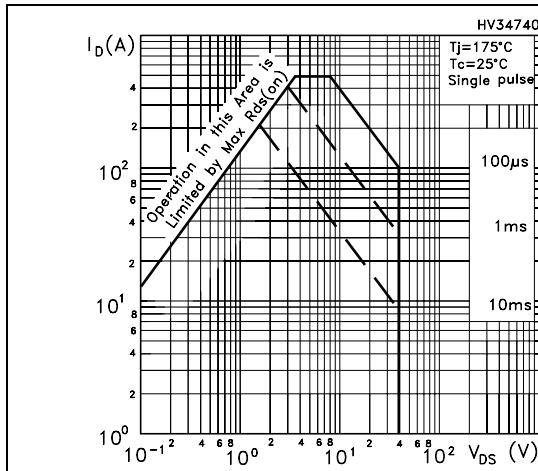


Figure 2. Thermal impedance

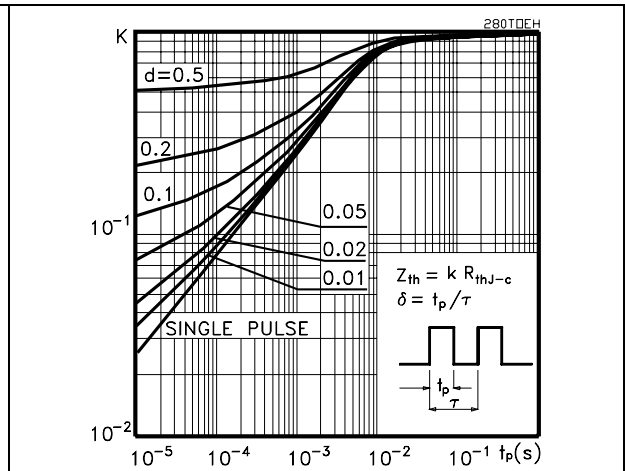


Figure 3. Output characteristics

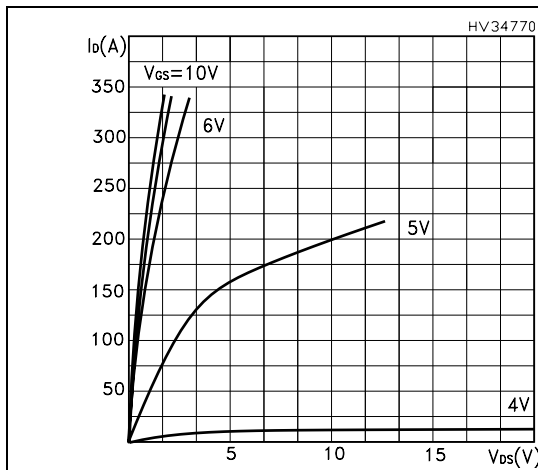


Figure 4. Transfer characteristics

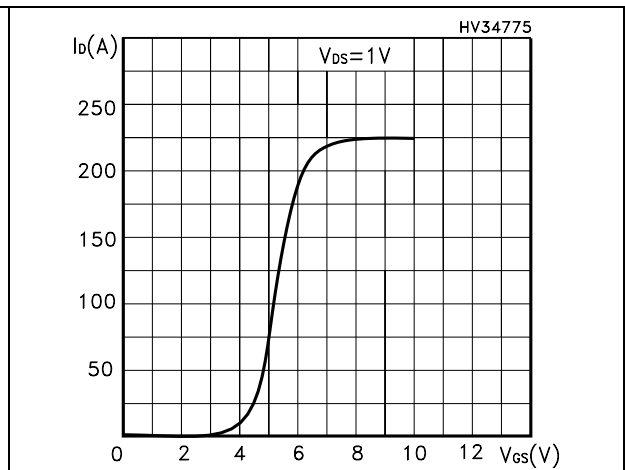


Figure 5. Normalized $B_{V_{DS}}$ vs temperature

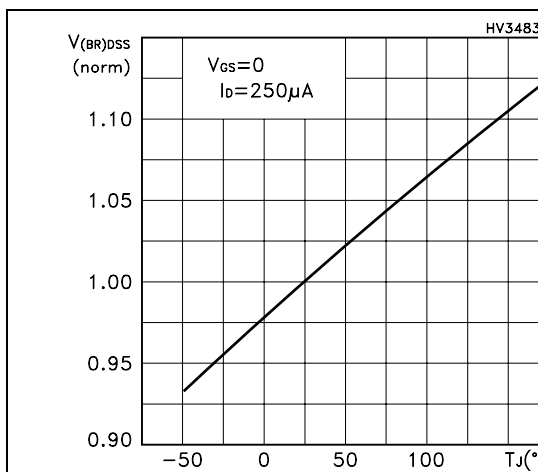


Figure 6. Static drain-source on resistance

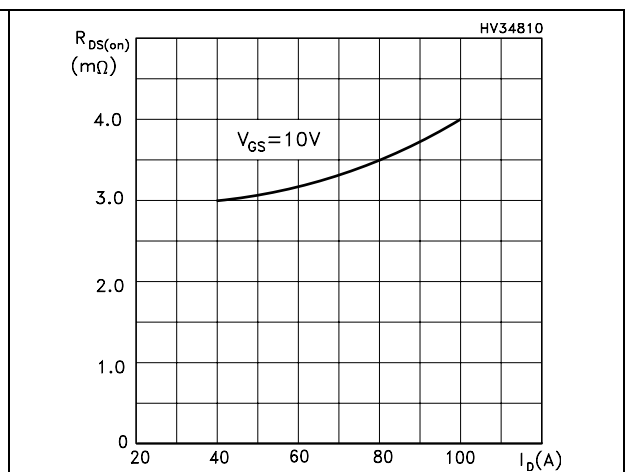


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

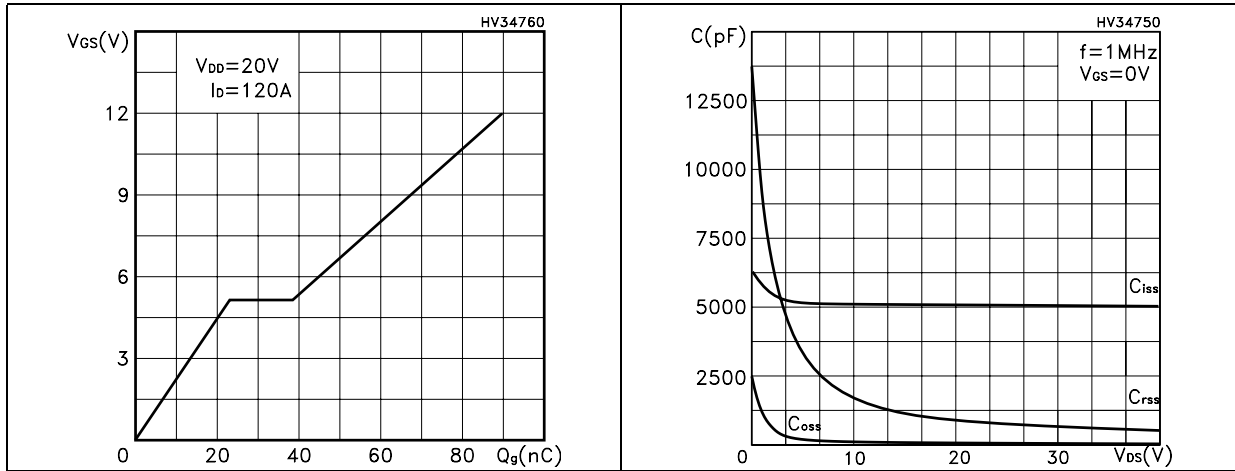


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

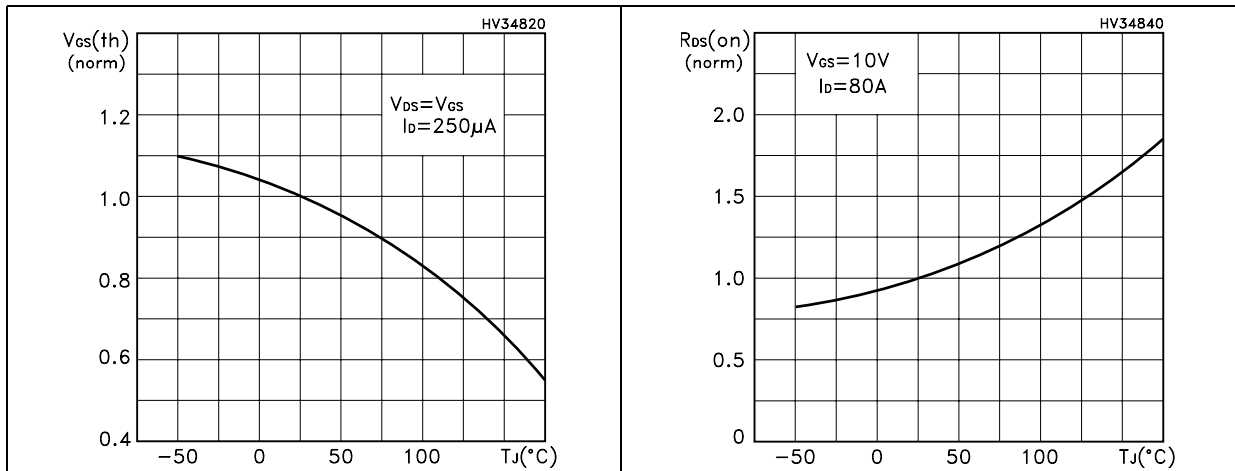
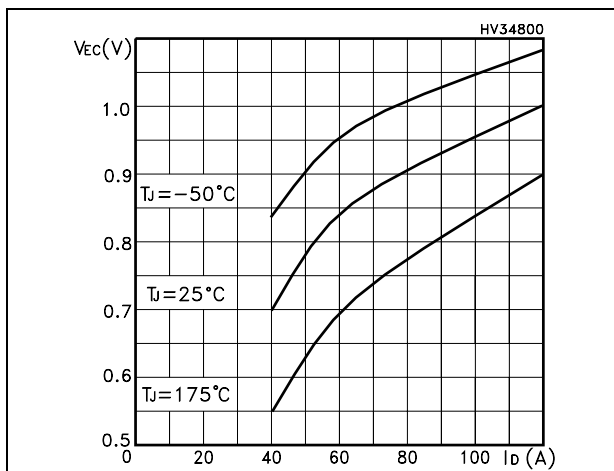


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

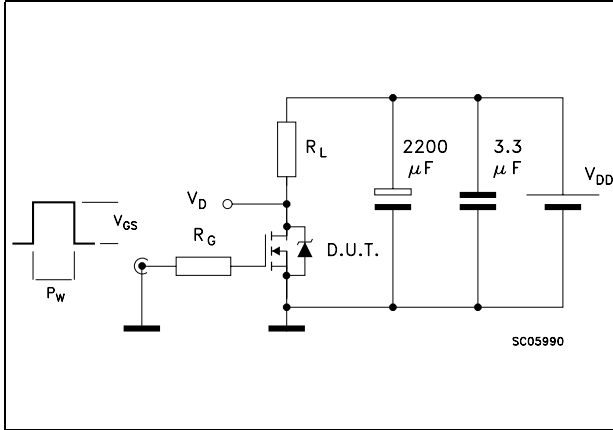


Figure 13. Gate charge test circuit

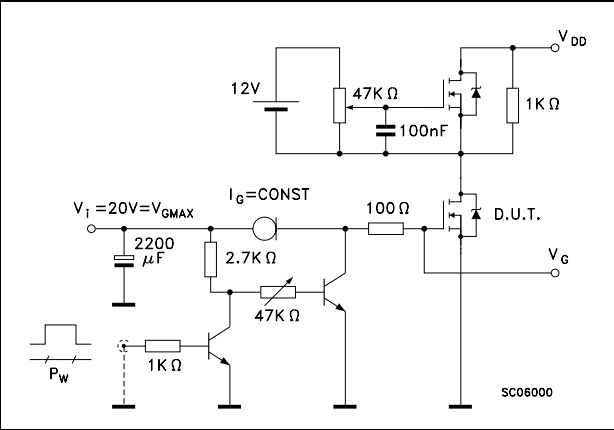


Figure 14. Test circuit for inductive load switching and diode recovery times

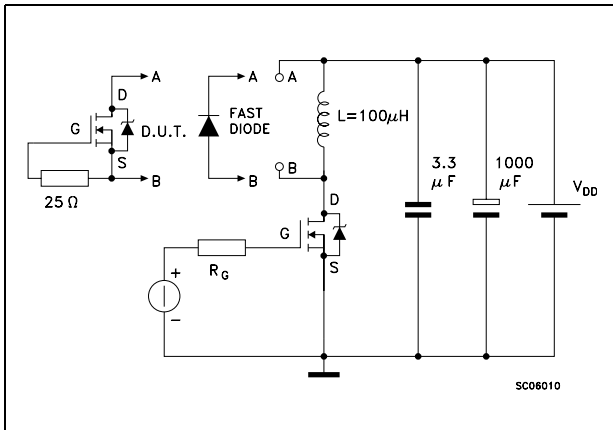


Figure 15. Unclamped Inductive load test circuit

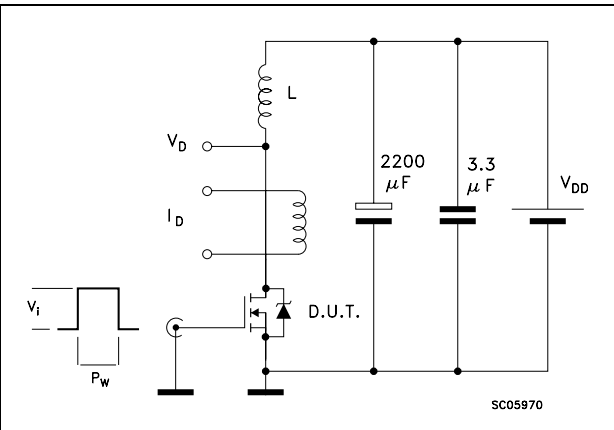


Figure 16. Unclamped inductive waveform

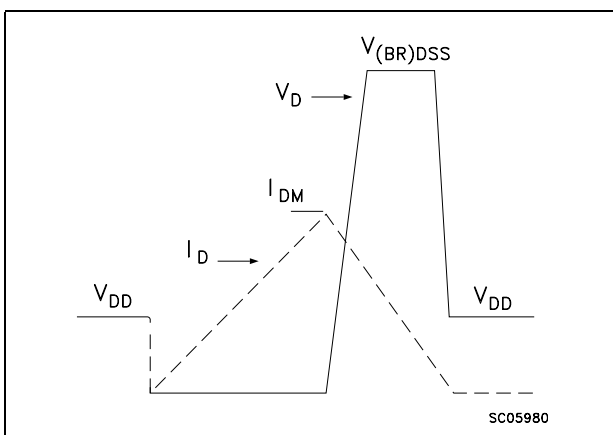
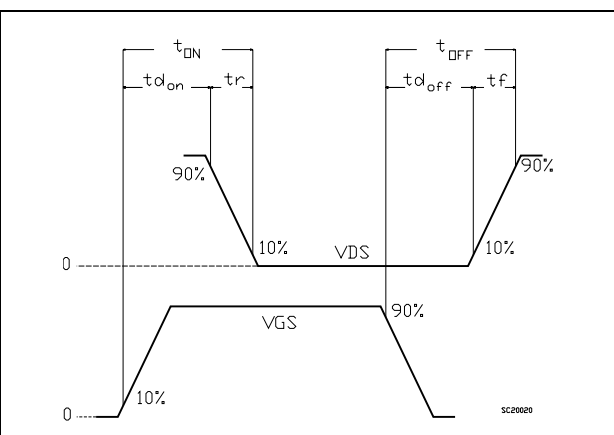


Figure 17. Switching time waveform

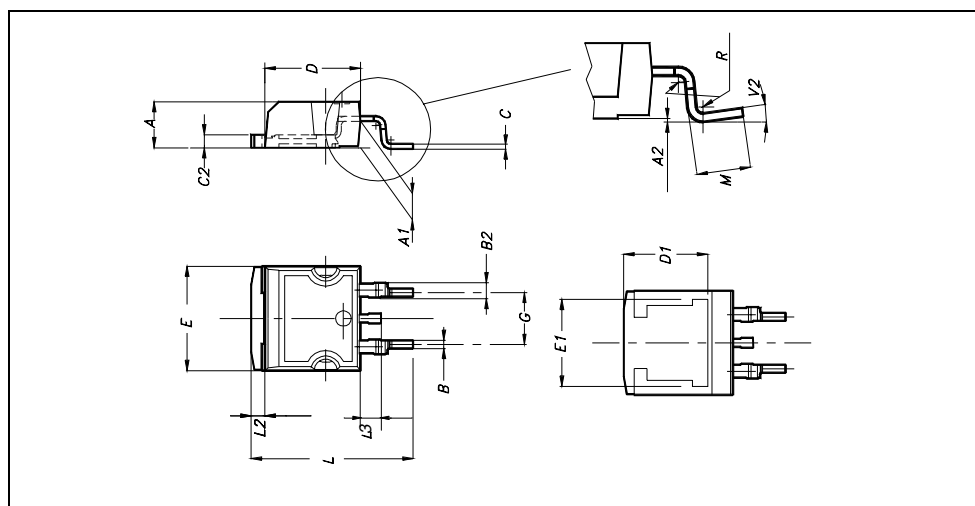


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



6 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Nov-2006	1	First release

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