MP2009

Ultra-Low-Noise Low-Dropout, 120mA Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP2009 is an ultra low noise, low dropout linear regulator. The output voltage of MP2009 ranges from 1.5V to 4.5 V in 100mV increments and 1% accuracy by operating from a +2.0V to +6.0V input. It is designed to deliver up to 120mA continuous output current. It achieves a low 120mV dropout for full load current.

The MP2009 uses an internal PMOS as the pass element, which consumes 50µA supply current at no load condition. New innovative design techniques make MP2009 achieve ultra-low output voltage noise of 16µV $_{RMS}$ without a noise bypass capacitor.

The MP2009 are designed and optimized to work with low value, low cost ceramic capacitors in space-limiting and performance consideration. It requires only 1µF (typ) of output capacitance for stability with any load. It is available in a 5-pin SC70 package.

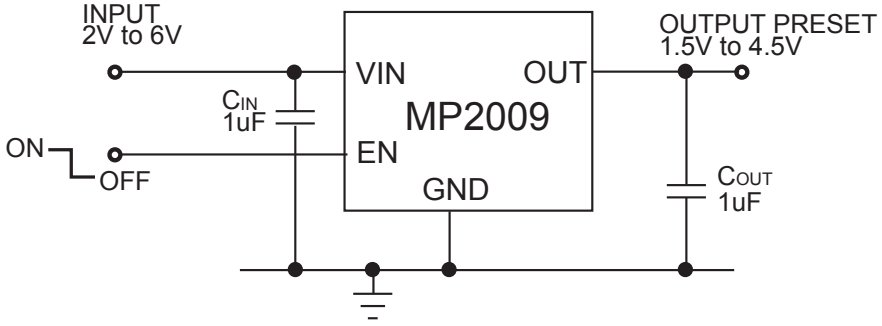
FEATURES

- Space-Saving SC70 Package
- 16µV $_{RMS}$ Output Noise (100Hz to 30kHz) No Bypass Capacitor Required
- 78dB PSRR at 1kHz
- 120mV Dropout at 120mA Load
- Stable with 1µF Ceramic Capacitor for Any Load
- Low 50µA Ground Current
- Very Fast Line and Load Transient Response with Small Input and Output Capacitor
- Current Limit and Thermal Protection

APPLICATIONS

- Cellular and Cordless Phones
- VCOs
- PDA and Palmtop Computers
- Digital Cameras
- Base Stations
- Wireless LANs
- Bluetooth Portable Radios and Accessories
- Portable and Battery-Powered Equipment

TYPICAL APPLICATION

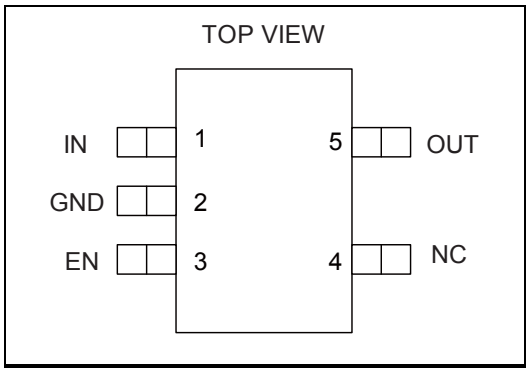


ORDERING INFORMATION

Part Number*	Package	VOUT(V) Top	Marking	Free Air Temperature Range (T_A)
MP2009EE-1.5 1.5	5-SC70			-20°C to +85°C
MP2009EE-1.8 1.8			8B	
MP2009EE-2.5 2.5			AQ	
MP2009EE-2.6 2.6				
MP2009EE-2.7 2.7				
MP2009EE-2.8 2.8				
MP2009EE-2.85 2.85				
MP2009EE-3 3				
MP2009EE-3.3 3.3			9U	
MP2009EE-4.0 4.0			CG	
MP2009EE-4.5		4.5		

* Available options are identified by those with top marking. For other options, please contact factory to check availability.

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Input Voltage 6.5V
Power Dissipation, P_D @ T_A =25°C (2)
5-SC70 ..... 0.385W
Operation Temperature Range ... -20°C to 85°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10sec) .....300°C

Recommended Operating Conditions (3)

Supply Input Voltage.....2.0V to 6.0V
Enable Input Voltage .....0V to 6.0V
Maximum Junction Temp. (T_J).....+125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
5-SC70	260	130 °C/W

Notes:

1) Exceeding these ratings may cause permanent damage to the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150°C(typ) and disengages at T_J=130°C (typ).
3) The device is not guaranteed to function outside its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{OUT}+0.5V, V_{EN}= V_{IN}, and C_{IN}=1μF, C_{OUT}=1μF, Typical values are at T_A=25°C, unless otherwise noted.

Parameter Sy	mbol	Conditions		Min	Typ	Max	Units
Input Voltage Range	V_{IN}			2		6	V
Output Voltage Accuracy		I_{OUT} =1mA,T_A=25°C -1				1	%
		I_{OUT} =100μA to 80mA,T_A=25°C -2				2	
		I_{OUT} =100μA to 80mA, T_A=-20°C ~85°C			±3		
Maximum Output Current	I_{OUT}			120			mA
Current Limit	I_{LIM}	V_{OUT} =1.8V OUT=90% of nominal value		130	200	300	mA
		V_{OUT} =2.5V OUT=90% of nominal value		160	230	330	mA
		V_{OUT} =3.3V OUT=90% of nominal value		180	250	350	mA
Dropout Voltage [5]		V_{OUT} =1.8V, I_{OUT} =80mA			115	240	mV
		V_{OUT} =1.8V, I_{OUT} =120mA			172		mV
		V_{OUT} =2.5V, I_{OUT} =80mA			100	220	mV
		V_{OUT} =2.5V, I_{OUT} =120mA			140		mV
		V_{OUT} =3.3V, I_{OUT} =80mA			80	200	mV
		V_{OUT} =3.3V, I_{OUT} =120mA			120		mV
Ground Current	I_Q	I_{OUT} =0.05mA			50	90	μA
		V_{IN}=Vout-0.1V, I_{OUT} =0mA			50	90	
Line Regulation[6]	V_{LNR}	V_{IN}=Vout+0.5V to 6V I_{OUT} =0.1mA			0.03		%/V
Load Regulation[7]	V_{LDR}	I_{OUT} =1mA to 120mA			0.002		%/mA
Shutdown Supply Current	I_{SHDN} V	$_{EN}$=0	T_A=25°C		0.01	1	μA
			T_A=85°C		0.2		
Ripple Rejection	PSRR	F=1kHz, I_{OUT} =10mA			78		dB
		F=10kHz, I_{OUT} =10mA			75		
		F=100kHz, I_{OUT} =10mA			55		
Output Noise Voltage		F=100Hz to 30kHz I_{LOAD}=10mA		16			$μV_{RMS}$
		F=100Hz to 30kHz I_{LOAD}=80mA		17			
EN Startup delay[8]		R_{LOAD}=50Ω				150	μs
V_{EN} Logic Low Level		V_{IN}=2V to 6V	T_A=25°C			0.4	V
			T_A=85°C			0.3	
V_{EN} Logic High Level		V_{IN}=2V to 6V		1.5			V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{OUT}+0.5V, V_{EN}= V_{IN}, and C_{IN}=1µF, C_{OUT}=1µF, Typical values are at T_A=25°C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
V_{EN} Input Bias Current		V_{IN}=6V, V_{EN}=6V	T_A=25°C			1	µA
			T_A=85°C		0.01		
Thermal Shutdown(9)					150		°C
Thermal Shutdown Hysteresis					20		°C

Notes:

5) Dropout is defined as V_{IN}-V_{OUT} when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN}= V_{OUT} +0.5V.

6) $$\text{Line Regulation} = \frac{\left|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}\right|}{(V_{IN(MAX)} - V_{IN(MIN)})} \times \frac{}{V_{OUT(NOM)}} \quad 100(\%/V)$$

7) $$\text{Load Regulation} = \frac{\left|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}\right|}{(I_{OUT(MAX)} - I_{OUT(MIN)})} \times \frac{}{V_{OUT(NOM)}} \quad 100(\%/mA)$$

8) Time needed for V_{OUT} to reach 90%of final value.

9) Guaranteed by design, not tested.

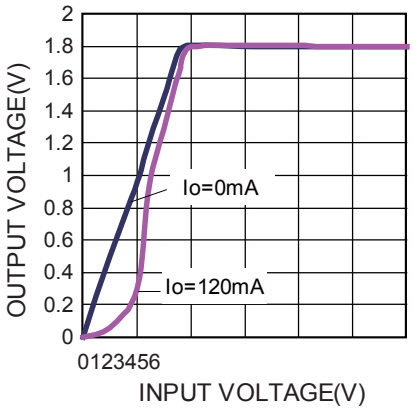
PIN FUNCTIONS

Pin #	Name	Description
1	IN	Input supply
2	GND	Common Ground
3 EN		When enable pin (EN) is high, the regulator turns on; when enable pin (EN) is low, the regulator shutdown.
4	NC	No Connection
5	OUT	Output of the regulator

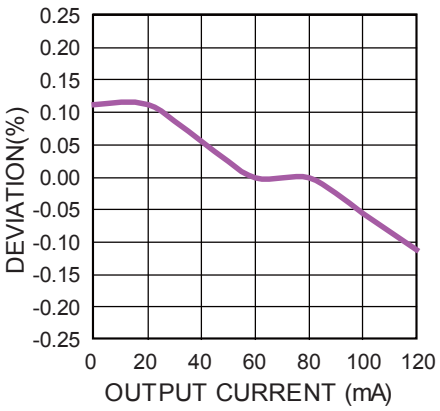
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=2.3V, V_{OUT}=1.8V, C_{IN}=1µF, C_{OUT}=1µF, EN=2.3V, Typical Value at T_A = 25°C unless otherwise specified.

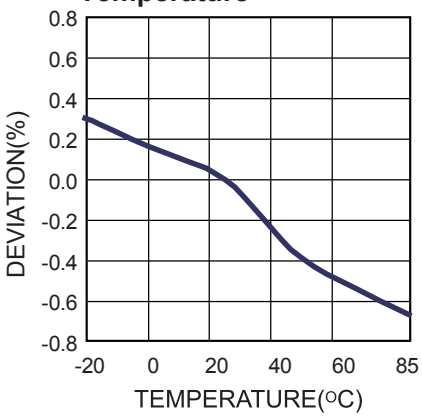
V_{IN} vs. V_{OUT}



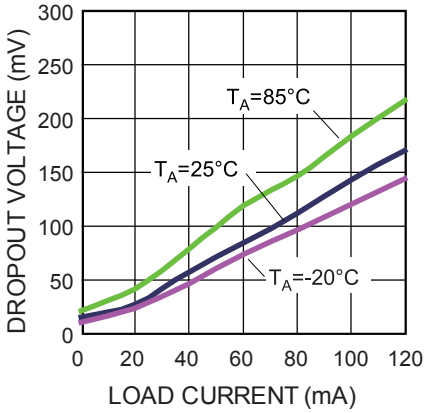
Load Regulation



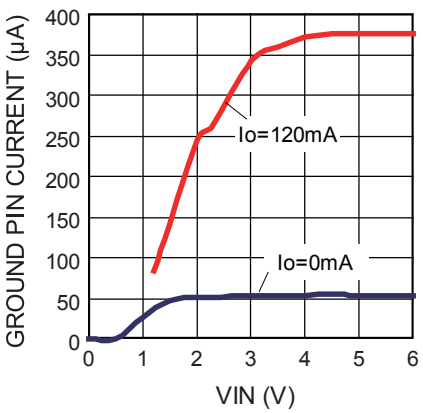
Voltage Accuracy vs. Temperature



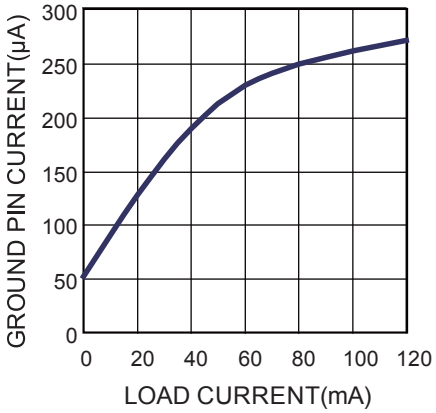
Dropout Voltage vs. Output Current



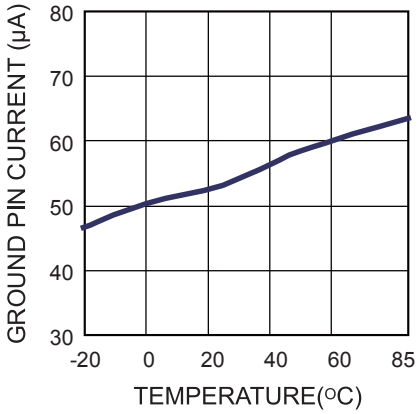
Ground Pin Current vs. V_{IN}



Ground Pin Current vs. Output Current

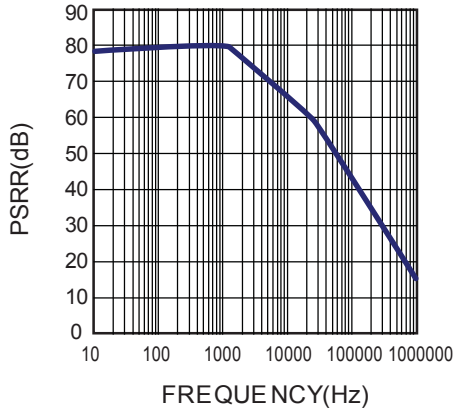


Ground Pin Current vs. Temperature

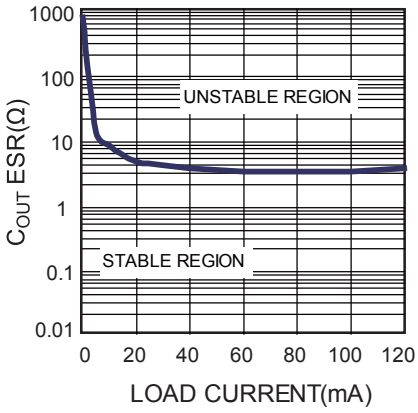


PSRR vs. Frequency

I_{OUT}=10mA



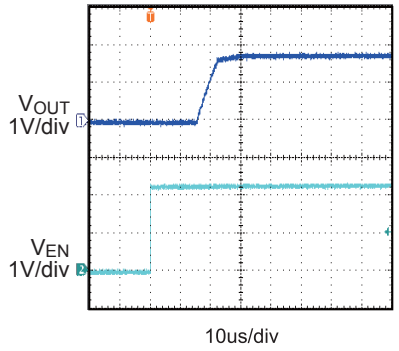
Region of Stable Cout ESR vs. Load Current



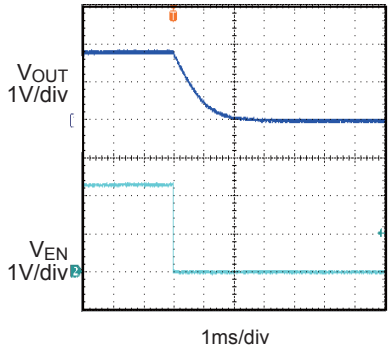
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=2.3V, V_{OUT}=1.8V, C_{IN}=1µF, C_{OUT}=1µF, EN=2.3V, Typical Value at T_A = 25°C unless otherwise specified.

EN Startup Waveform

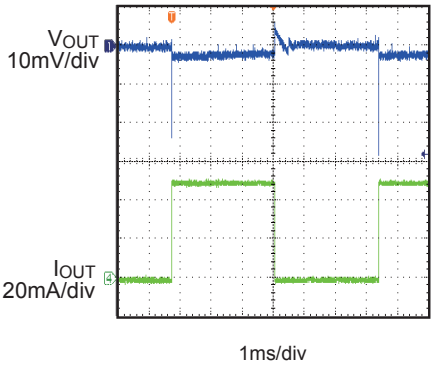


EN Shutdown Waveform



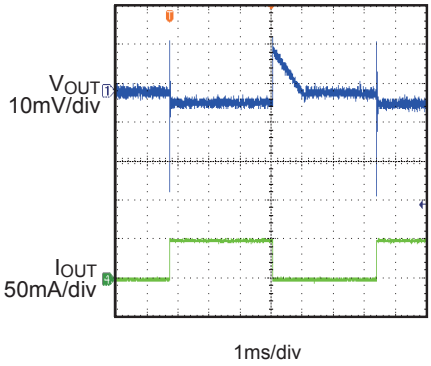
Load Transient Response

I_{OUT}=0 to 50mA



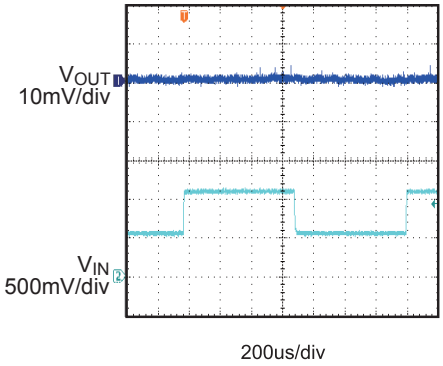
Load Transient Response Near Dropout

V_{IN}=1.9V, I_{OUT}=0 to 50mA



Line Transient Response

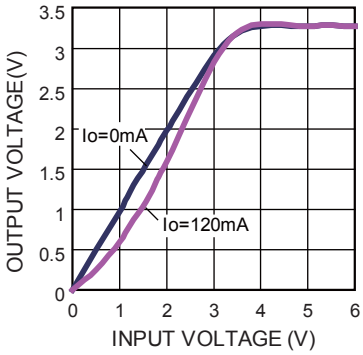
V_{IN}=2.3V to 2.8V, I_{OUT}=0mA



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

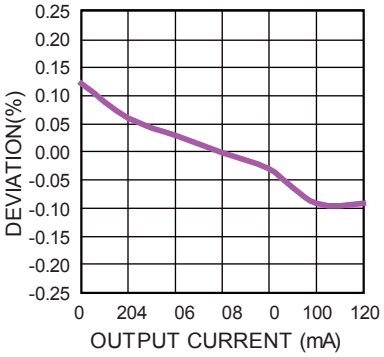
V_{IN}=3.8V, V_{OUT}=3.3V, C_{IN}=1μF, C_{OUT}=1μF, EN=3.8V, Typical Value at T_A = 25°C unless otherwise specified.

V_{IN} vs. V_{OUT}

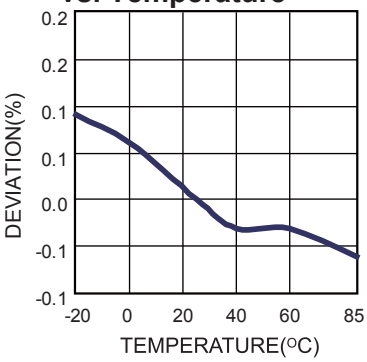


Load Regulation

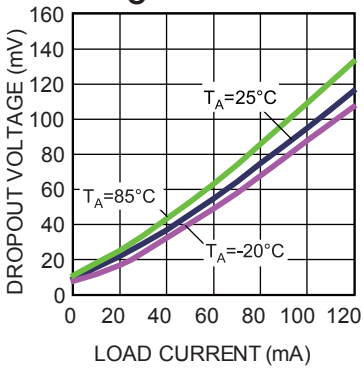
V_{IN}=3.8V



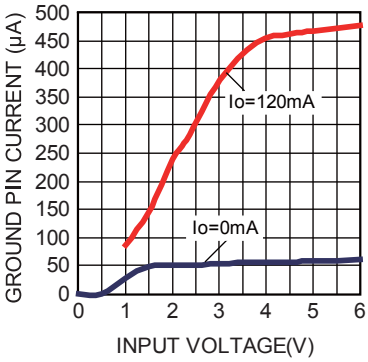
Output Voltage Accuracy vs. Temperature



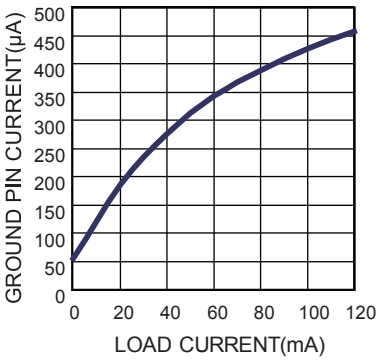
Dropout Voltage vs. I_O



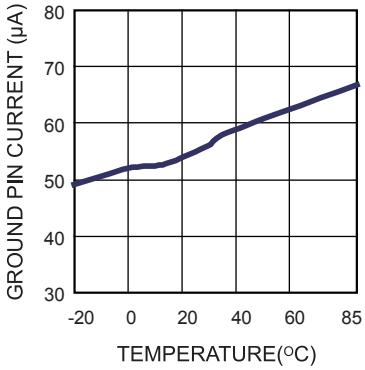
Quiescent Current vs. V_{IN}



Quiescent Current vs. I_O

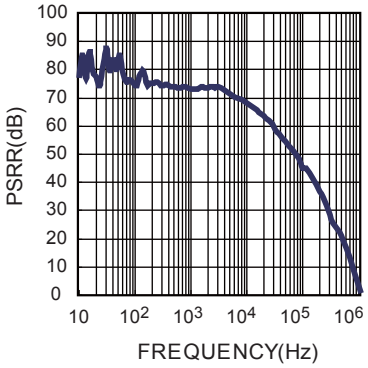


Quiescent Current vs. T_A

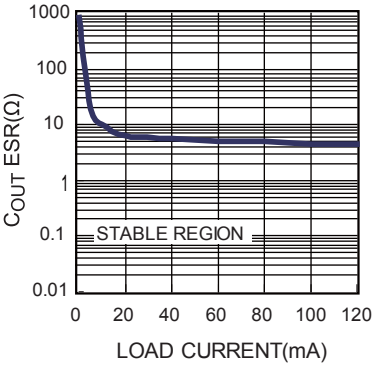


PSRR vs. Frequency

I_{OUT}=10mA



Region of Stable Cout ESR vs. Load Current

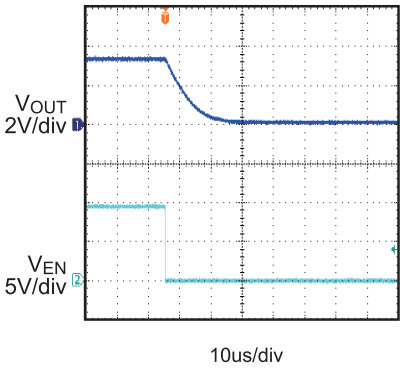


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=3.8V, V_{OUT}=3.3V, C_{IN}=1µF, C_{OUT}=1µF, EN=3.8V, Typical Value at T_A = 25°C unless otherwise specified.

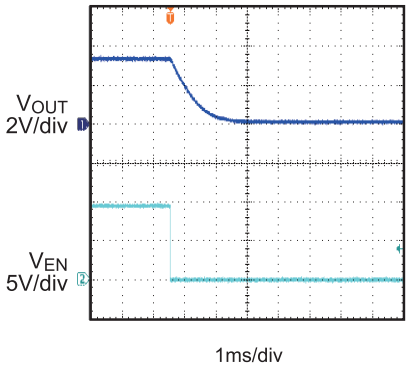
EN Startup Waveform

I_{OUT}=0mA



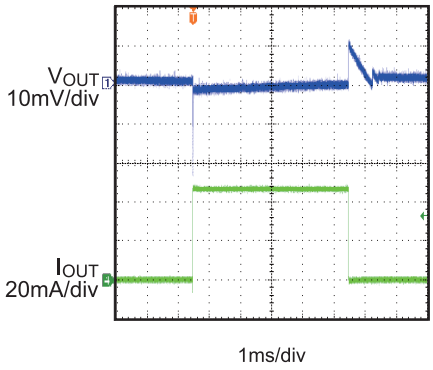
EN Shutdown Waveform

I_{OUT}=0mA



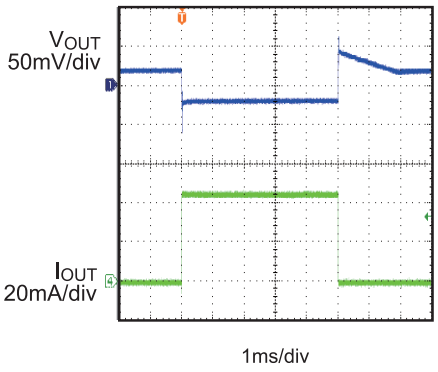
Load Transient Response

V_{IN}=3.8V, I_{OUT}=0mA to 50mA



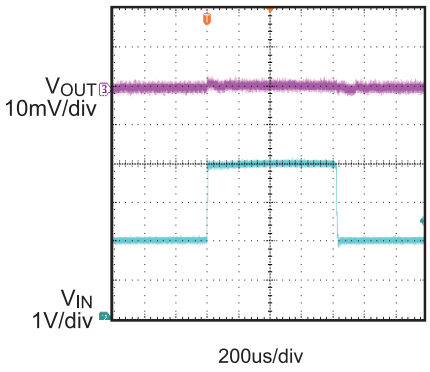
Load Transient Response Near Dropout

V_{IN}=3.2V, I_{OUT}=0mA to 50mA



Line Transient Response

V_{IN}=3.8V to 6V, I_{OUT}=0mA



FUNCTION BLOCK DIAGRAM

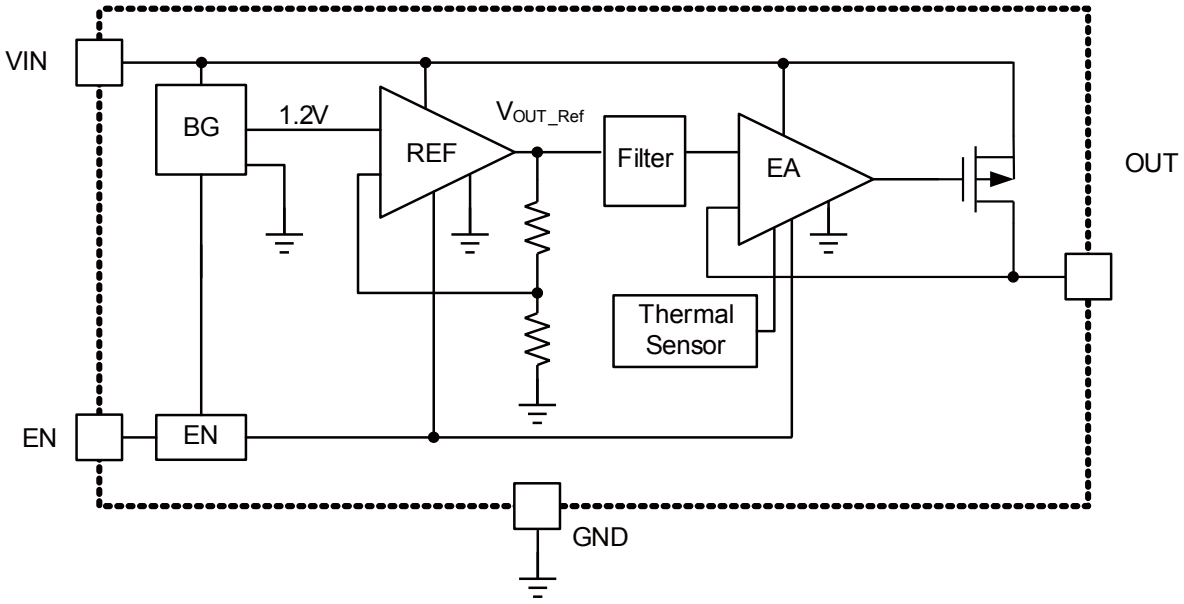


Figure1—Functional Block Diagram

OPERATION

The MP2009 is an ultra low noise, low dropout, low-quiescent current linear regulator designed for space-restricted applications. It is intended for use in devices that requires very low voltage, low quiescent current such as wireless LAN, battery-powered equipment and hand-held equipment.

Internal P-Channel Pass Transistor

The MP2009 features a 1.4Ω P-channel MOSFET as the pass transistor. It provides several advantages over similar designs using PNP pass transistor. The P-channel MOSFET requires no base drive, which reduces quiescent current considerably and increase the battery life. PNP-based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base-drive current under the large load condition. The MP2009 does not suffer from these problems and consume only 50μA of quiescent current in light load and dropout mode.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. It determines the available end-of-life battery voltage in battery-powered systems. For the P-channel MOSFET pass element, the dropout voltage is a function of drain to source on resistance. Because the P-channel MOSFET pass element behaves as a low-value resistor, the dropout voltage of MP2009 is very low.

Shutdown

The MP2009 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off. The EN pin should be tied to VIN to keep the regulator output always on if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit and Thermal Protection

The MP2009 includes an independent current limit structure which monitors and controls the P-channel MOSFET's gate voltage to limit the guaranteed maximum output current to 120mA. Thermal protection turns off the P-channel MOSFET when the junction temperature exceeds +150ºC, allowing the IC to cool. When the IC's junction temperature drops by 20º C, the PMOS will be turned on again. Thermal protection limits total power dissipation in the MP2009. For reliable operation, junction temperature should be limited to 125 ºC maximum.

APPLICATION INFORMATION

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction} - T_{Ambient}$) is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the GND pin of MP2009 to ground with a large ground plane will help the channel heat away.

Output Noise and PSRR

For the MP2009, an internal 50pF bypass capacitor with new innovative structure reduces output noises greatly. It does not need external bypass capacitor for space-limiting applications. The power supply rejection is 75dB at 10kHz and 55dB at 100kHz. (See the PSRR vs. Frequency graph in the Typical Performance Characteristics).

Input Capacitor Selection

Use a 1μF capacitor on the input of the MP2009. Larger values will help to improve line transient response with the drawback of increased size. Ceramic capacitors are preferred, but tantalum capacitors may also suffice.

Output Capacitor Selection

The MP2009 is designed specifically to work with very low ESR ceramic output capacitor in space-limiting and performance consideration. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size. A 1μF ceramic capacitor with ESR lower than 3Ω is sufficient for the MP2009 application circuit. (See the Region of Stable C_{OUT} ESR vs. Load Current graph in the Typical Performance Characteristics)

PCB LAYOUT GUIDE

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal perfo rmance. I t is highly recommended to duplicate EVB layout for optimum performance.

If change is ne cessary, please f ollow these guidelines and take figure 2 for reference.

1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
2) Ensure all feedback connections a re short and direct. Place the feedback re sistors and compensation components as clo se to the chip as possible.
3) Connect IN, OUT a nd especia lly GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

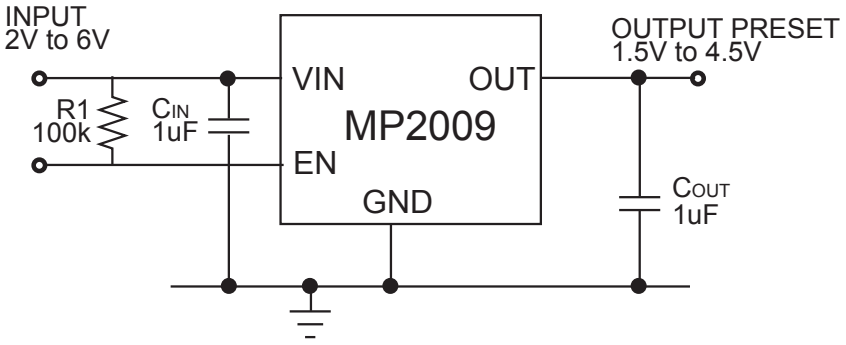


Figure 2 —MP2009 Typical Application Circuit

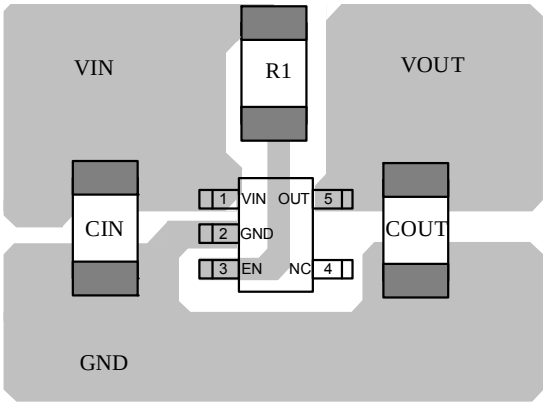
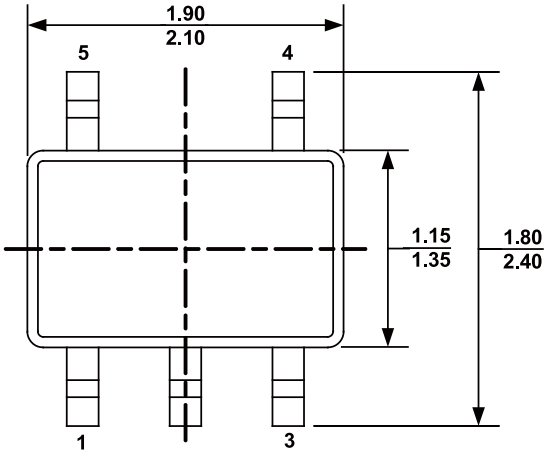


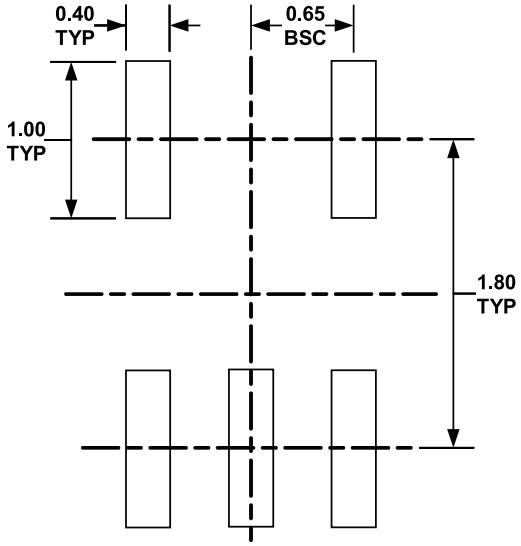
Figure 3—MP2009 Top Layer

PACKAGE INFORMATION

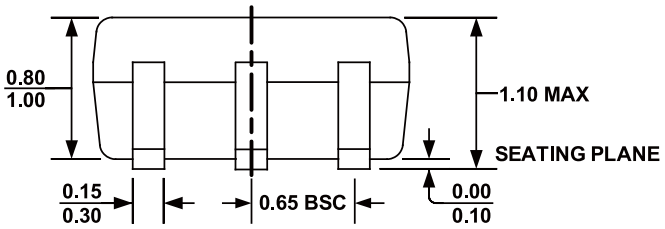
5-SC70



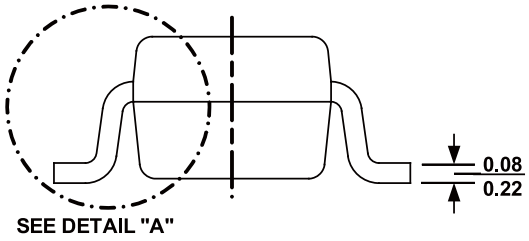
TOP VIEW



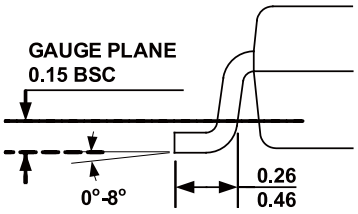
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-203, VARIATION AA.
6) DRAWING IS NOT TO SCALE