Bt475

Bt477

110 MHz 256-Word Color Palette Personal System/2® Power-Down RAMDAC™

4

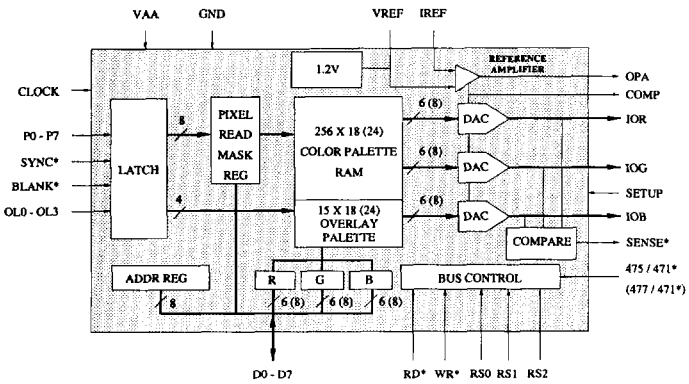
Distinguishing Features

- 110, 80, 66, 50, 35 MHz Operation
- Bt471/476/478 Pin Compatibility
- Power-Down Mode
- Antisparkle Circuitry
- Analog Output Comparators
- Triple 6-bit (8-bit) D/A Converters
- 256 x 18 (24) Color Palette RAM
- RS-343A/RS-170-Compatible Outputs
- 15 x 18 (24) Overlay Registers
- Programmable Pedestal
- Optional Internal Reference
- 44-pin PLCC Package

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Laptop Computers

Functional Block Diagram



Product Description

The Bt475 and Bt477 RAMDACs are designed specifically for Personal System/2®-compatible color graphics.

The Bt475 has a 256 x 18 lookup table RAM, 15 x 18 overlay registers, and triple 6-bit D/A converters.

The Bt477 has a 256 x 24 lookup table RAM, 15 x 24 overlay registers, and triple 8-bit D/A converters. Both 6-bit and 8-bit color modes are supported.

On-chip analog output comparators are included to simplify diagnostics and debugging with the result output onto the SENSE* pin. An on-chip voltage reference is also included to simplify use of the device.

A power-down mode is available to reduce power requirements when the analog outputs are not used. This is useful in laptop computer systems that need the option of driving an external RGB monitor.

When the 475/471* input pin (477/471* on the Bt477) is floating or a logical zero, the Bt475 and Bt477 behave as a Bt471 with antisparkle capabilities, on-chip reference, and analog comparators. When the pin is a logical one, the additional capabilities of the command register are available.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt475/477 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into an 18-bit or 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to se-

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register (Note 1)

Note 1: Available only when the 475/471* (477/471*) pin is a logical one.

Table 1. Control Input Truth Table.

Circuit Description *(continued)*

lect the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Additional Information

When the color palette RAM is accessed, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While the overlay color registers are accessed, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic. These data transfers take place during the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU. They are used to address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

The pixel clock must be active for MPU accesses to the color palette RAM.

Bt471-Compatible Operation

If the 475/471* (477/471*) pin is a logical zero, the Bt475/477 operates as a Bt471 RAMDAC; the command register is disabled, and 6-bit operation is selected. Color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

In the 6-bit mode, the Bt477's full scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

If the 475/471* (477/471*) input is a logical one, the command register is available. On the Bt477, the 6-bit/8-bit select bit in the command register may be used to specify whether 6-bit or 8-bit color data values are being used.

8-bit / 6-bit Color Selection

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus. D0 is the LSB and D5 is the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logical zeros.

In the 6-bit mode, the Bt477's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description *(continued)*

Power-Down Mode

The Bt475/477 incorporates a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt475/477 functions normally. The SLEEP enable bit is not initialized on power-up and must be a logical zero for normal operation.

While the SLEEP bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may still be read or written to while sleeping as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed.

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn the current reference off (IREF = 0 mA) during sleep mode.

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

SENSE Output*

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level of the SENSE comparator circuit. This output is used to determine the presence of a CRT monitor. Also with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For proper operation of the SENSE circuit, the following levels should be applied to the comparator through the IOR, IOG, and IOB outputs:

DAC Low Voltage ≤ 325 mV
DAC High Voltage ≥ 395 mV

There is an additional ±10-percent tolerance on the above levels when the internal voltage reference or an external current reference is used. SYNC* should be a logical zero for SENSE* to be stable. Also, the SENSE output can drive only one CMOS load.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bitwise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits (Bt475) or 24 bits (Bt477) of color information to the three D/A converters. For proper operation, the pixel read mask register must be initialized by the user after power-up.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 1–3. Tables 4–6 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input pin is logically ANDed with the SETUP command bit and is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used.

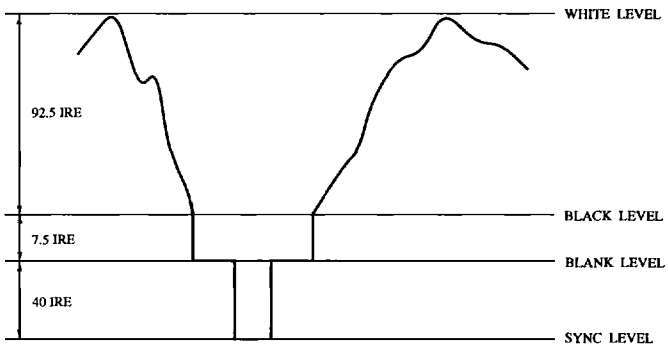
The analog outputs of the Bt475/477 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

OL0–OL3	P0–P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 1. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

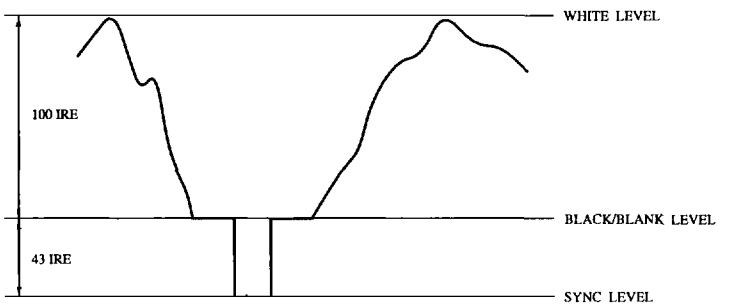
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 2. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE).

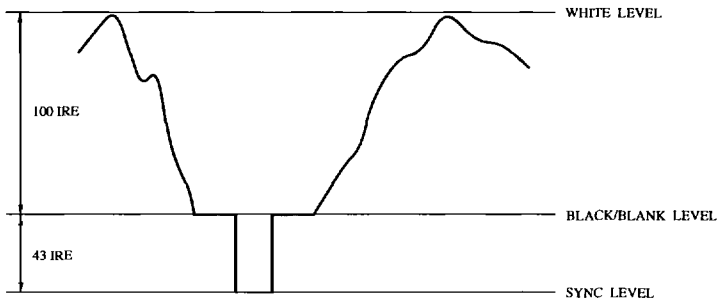
Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load and SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Command Register

This register is operational only while the 475/471* (477/471*) pin is a logical one. It may be written to or read by the MPU at any time and is not initialized. For proper operation, it must be initialized by the user after power-up.

D7	reserved (logical zero)	A logical zero must be written to this bit when writing to the command register to ensure proper operation.
D6	reserved (logical one)	A logical one must be written to this bit when writing to the command register to ensure proper operation.
D5	SETUP select (0) 0 IRE (1) 7.5 IRE	This bit specifies whether the blanking pedestal is 0 or 7.5 IRE. This bit is logically ANDed with the 475/471* (477/471*) input pin. Bit D5 controls the blanking pedestal only when in 475 (477) mode. The SETUP pin is disabled when it is operating inside this register.
D4	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output is to contain sync information.
D3	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output is to contain sync information.
D2	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output is to contain sync information.

Internal Registers *(continued)*

Command Register (continued)

D1	6-bit / 8-bit select (0) 6-bit (1) 8-bit	On the Bt477, this bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. On the Bt475, this bit must be a logical zero to ensure proper 6-bit operation.
D0	SLEEP enable (0) normal operation (1) sleep mode	While this bit is a logical zero, the Bt475/477 functions normally. The SLEEP enable must be initialized after power-up for normal operation. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may be read or written to as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. About 1 second is required for the Bt475/477 to output valid video data after enabling normal operation (coming out of sleep mode). This time will vary according to the size of the COMP capacitor. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If the DACs are using an external current reference, external circuitry should turn the current reference off during sleep mode. To further reduce power consumption in SLEEP mode, the pixel clock should be disabled while in SLEEP.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 4, 5, and 6. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). SETUP is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter. Clock Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which 1 of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 - OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as detailed in Table 3. When the overlay palette is accessed, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external or the internal voltage reference is used (Figures 4 and 5 in the PC Board Layout Considerations section), this pin should be connected to OPA. If an external current reference is used (Figure 6 in the PC Board Layout section), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *The PC Board Layout Considerations section contains critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating. However, the bypass capacitor should still be connected. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 4 and 5. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry other than the decoupling capacitor (Figure 4).
OPA	Reference amplifier output. If an external or the internal voltage reference is used (Figures 4 and 5), this pin must be connected to COMP. When an external current reference is used (Figure 6), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (Figures 4, 5, and 6).
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>IREF</td><td>Full-scale adjust control. The IRE relationships in Figures 1, 2, and 3 are maintained regardless of the full-scale output current.

When an external or the internal voltage reference is used (Figures 4 and 5), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

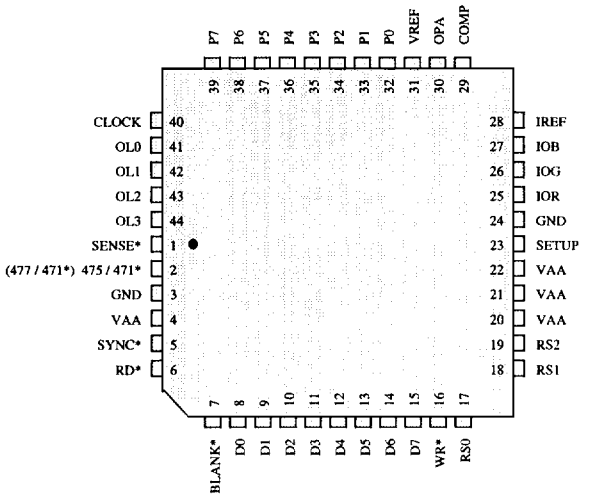
K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

When an external current reference is used (Figure 6), the relationship between IREF and the full-scale output current on each output is:

IREF (mA) = Iout (mA) / K

<table>
<tr><th>Part</th><th>Mode</th><th>Pedestal</th><th>K (with sync)</th><th>K (without sync)</th></tr>
<tr><td>Bt477</td><td>6-bit</td><td>7.5 IRE</td><td>3.013</td><td>2.170</td></tr>
<tr><td></td><td>8-bit</td><td>7.5 IRE</td><td>3.049</td><td>2.196</td></tr>
<tr><td></td><td>6-bit</td><td>0 IRE</td><td>2.852</td><td>2.010</td></tr>
<tr><td></td><td>8-bit</td><td>0 IRE</td><td>2.886</td><td>2.034</td></tr>
<tr><td>Bt475</td><td>(6-bit)</td><td>7.5 IRE</td><td>3.013</td><td>2.170</td></tr>
<tr><td></td><td></td><td>0 IRE</td><td>2.852</td><td>2.010</td></tr>
</table>
</td></tr>
<tr><td>WR*</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing in the PC Board Layout Considerations section contains detailed layout suggestions.</td></tr>
<tr><td>RD*</td><td>Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as shown in Tables 1 and 2. MPU Control Signal Interfacing contains detailed layout suggestions.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>475/471*
(477/471*)</td><td>Bt475 (Bt477) or Bt471 select input (TTL compatible). When the 475/471* (477/471*) input pin is floating or a logical zero, the Bt475/477 behaves as a Bt471 with antisparkle capabilities. When the 475/471* (477/471*) input pin is a logical one, the extra capabilities of the Bt475/477 command register are available.</td></tr>
<tr><td>SENSE*</td><td>Sense output (CMOS levels). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level. SENSE* may not be stable while SYNC* is toggling. Also, the SENSE* output can drive only one CMOS load.</td></tr>
</table>

Pin Descriptions *(continued)*



Names in parentheses are pin names for the Bt477.

PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt475 and Bt477, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt475 and Bt477 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt475 and Bt477 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt475 and Bt477 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within 3 inches of the Bt475 and Bt477. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 4, 5, and 6 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

Digital Signal Interconnect

The digital inputs to the Bt475 and Bt477 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt475 and Bt477 require a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt475 and Bt477 use the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt475 and Bt477 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt475 and Bt477 to minimize reflections. Unused analog outputs should be connected to GND.

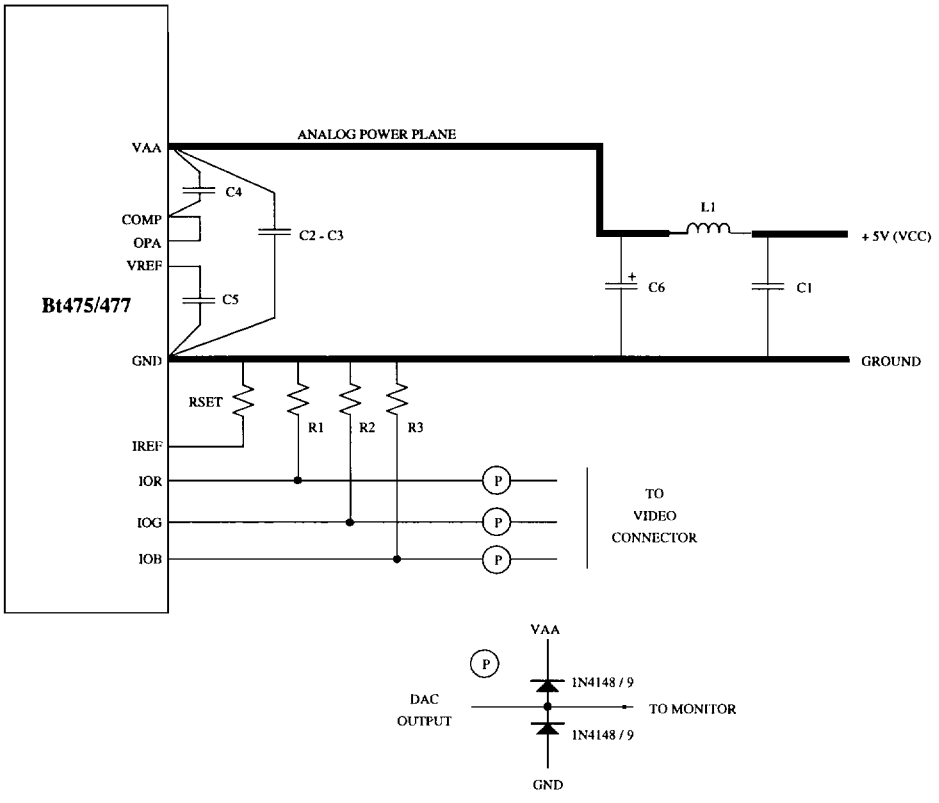
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt475 and Bt477 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



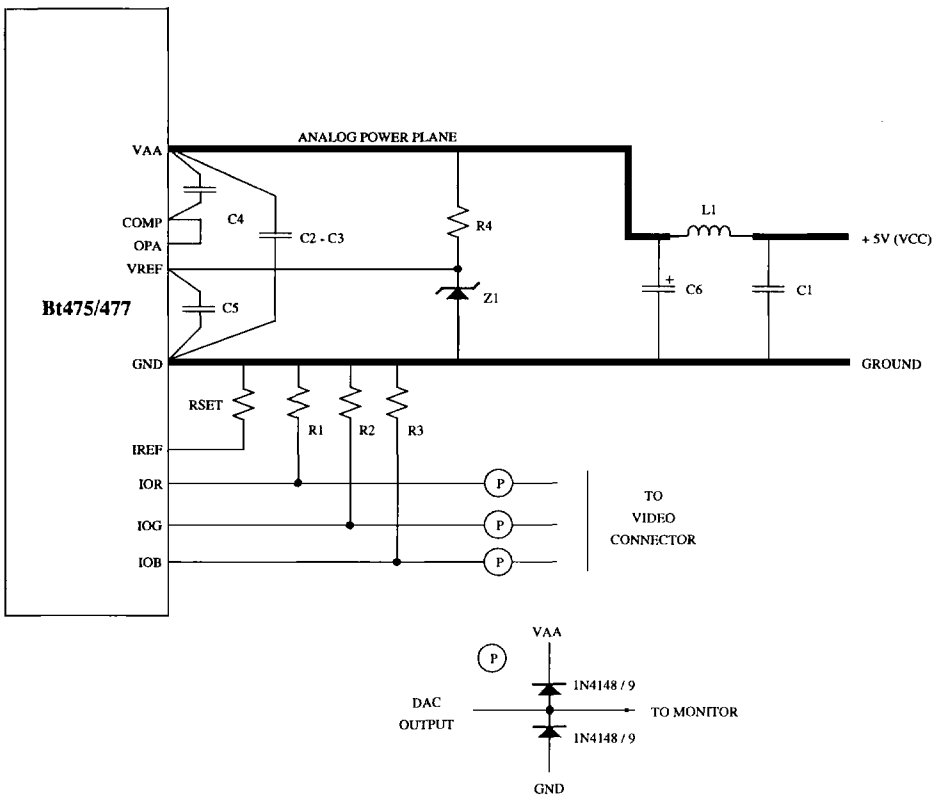
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 4. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



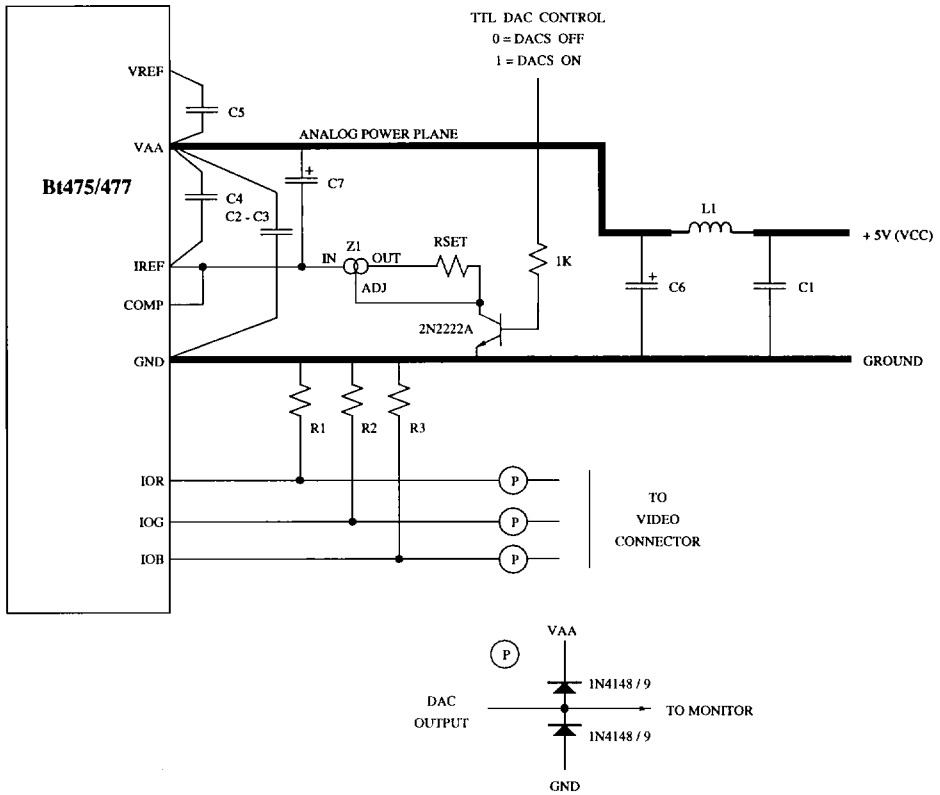
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	—
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 5. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM317LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 6. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When multipl112112:d475/477s are used, each Bt475/477 should share a common power plane with one ferrite bead. If the internal reference is used, each Bt475/477 should use its own.

Although the multiple Bt475/477s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAM-DAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt475/477 must have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about 10 times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

When an external current reference is used, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 6, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode. The SLEEP enable bit is not initialized on power-up and must be a logical zero for normal operation.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
110, 80, 66 MHz Parts		4.75	5.00	5.25	V
50, 35 MHz Parts		4.5	5.00	5.5	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

4

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt475		6	6	6	Bits
Bt477		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt475				±1/4	LSB
Bt477				±1	LSB
Differential Linearity Error	DL				
Bt475				±1/4	LSB
Bt477				±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current					
White Level Relative to Black (Note 1)		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size					
Bt475			279.68		µA
Bt477			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Internal Reference Output	VREF	1.11	1.235	1.36	V
Power Supply Rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 475/471* (477/471*) pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: Since the Bt475 has 6-bit DACs (and the Bt477 when in the 6-bit mode), the output levels are approximately 1.5-percent lower than these values.

Note 2: Guaranteed by characterization, not tested.

AC Characteristics

		110 MHz Devices			80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			110			80			66	MHz
RS0–RS2 Setup Time	1	3			3			3			ns
RS0–RS2 Hold Time	2	3			3			3			ns
RD* Asserted to Data Bus Driven	3	5			5			5			ns
RD* Asserted to Data Valid	4			40			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20			20	ns
Read Data Hold Time	6	5			5			5			ns
Write Data Setup Time	7	10			10			10			ns
Write Data Hold Time	8	3			3			3			ns
RD*, WR* Pulse Width Low	9	50			50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			3			ns
Pixel and Control Hold Time	12	3			3			3			ns
Clock Cycle Time (p13)	13	9			12.5			15.15			ns
Clock Pulse Width High Time	14	4			4			5			ns
Clock Pulse Width Low Time	15	4			4			5			ns
Analog Output Delay	16			30			30			30	ns
Analog Output Rise/Fall Time	17			3			3			3	ns
Analog Output Settling Time (Note 1)	18		13			13			13		ns
Clock and Data Feedthrough (Note 1)			–30			–30			–30		dB
Glitch Impulse (Note 1)			75			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23			–23		dB
Analog Output Skew				2			2			2	ns
SENSE* Output Delay	19		1			1			1		µS
Pipeline Delay		4			4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2) normal operation			220	280		180	240		180	240	mA
sleep enabled (Note 3)			1	1.5		1	1.5		1	1.5	mA

See test conditions and the notes at the end of this section.
See, also, Figures 7 and 8.

AC Characteristics *(continued)*

		50 MHz Devices			35 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	3			3			ns
RS0–RS2 Hold Time	2	3			3			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	3			3			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17			3			3	ns
Analog Output Settling Time (Note 1)	18		20			28		ns
Clock and Data Feedthrough (Note 1)			–30			–30		dB
Glitch Impulse (Note 1)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current (Note 2)	IAA							
normal operation			180	240		180	240	mA
sleep enabled (Note 3)			1	1.5		1	1.5	mA

See test conditions and notes on next page.
See, also, Figures 7 and 8.

AC Characteristics *(continued)*

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 475/471* (477/471*) pin = logical one. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points are at 50 percent for inputs and outputs. Analog output load ≤ 10 pF. SENSE*, D0–D7 output load ≤ 75 pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.æ., 5 V.

Note 1: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Note 3: External current or voltage reference is disabled during sleep mode, and pixel clock is inhibited. Guaranteed by characterization, not tested.

Timing Waveforms

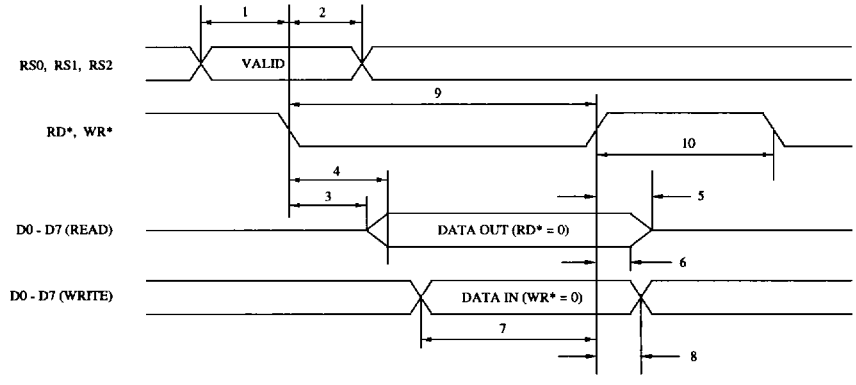
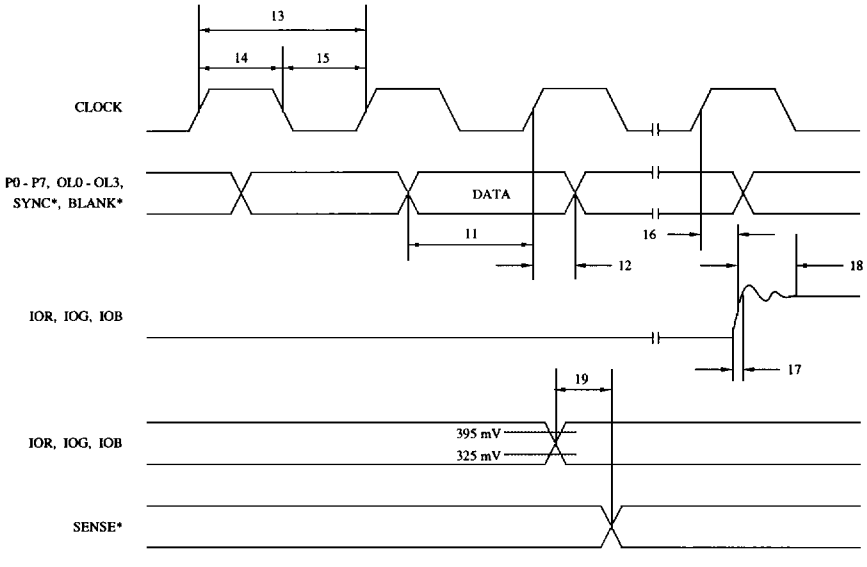


Figure 7. MPU Read/Write Timing.



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full scale transition to the output remaining within ±1 LSB (Bt477) or ±1/4 LSB (Bt475).

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. Video Input/Output Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Speed	Package	Ambient Temperature Range
Bt475KPJ80	256 x 18	15 x 18	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ66	256 x 18	15 x 18	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ50	256 x 18	15 x 18	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ35	256 x 18	15 x 18	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ110	256 x 24	15 x 24	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ80	256 x 24	15 x 24	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ66	256 x 24	15 x 24	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ50	256 x 24	15 x 24	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ35	256 x 24	15 x 24	35 MHz	44-pin Plastic J-Lead	0° to +70° C