Am28C256

32K x 8 Electrically Erasable PROM

ADVANCE INFORMATION

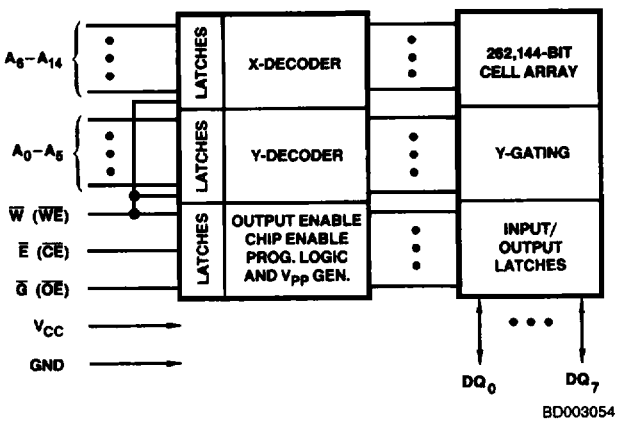
DISTINCTIVE CHARACTERISTICS

- 5-V only operation
- Military temperature range available
- Low-power CMOS
  - 60 mA active current
  - 1 mA standby current
  - 100 μA power-down current
- 64-byte page write
- Software-write protection
- Minimum endurance of 10,000 write cycles per byte with a ten year data retention

GENERAL DESCRIPTION

The Am28C256 is a 32,768 x 8-bit Electrically Erasable Programmable Read-Only Memory (EEPROM). It operates from a single 5-volt supply and has a fully self-timed write cycle with address, data, and control lines latched during the write operation. The 64-byte page-write mode allows full chip programming in as little as five seconds. The Am28C256, in the JEDEC-approved pinout, also features Status-Bit Polling, and a software-write protect that enhances the hardware-write protect. The Am28C256 is an upward-compatible part from the Am2864A and Am2864B. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



BD003054

PRODUCT SELECTOR GUIDE

Family Part No.				
Ordering Part No.: ±5% V_{CC} Tolerance	28C256-205	28C256	28C256-305	28C256-355
±10% V_{CC} Tolerance	28C256-200	28C256-250	28C256-300	28C256-350
t_{ACC} (ns)	200	250	300	350
t_{CE} (ns)	200	250	300	350
t_{OE} (ns)	75	100	110	120

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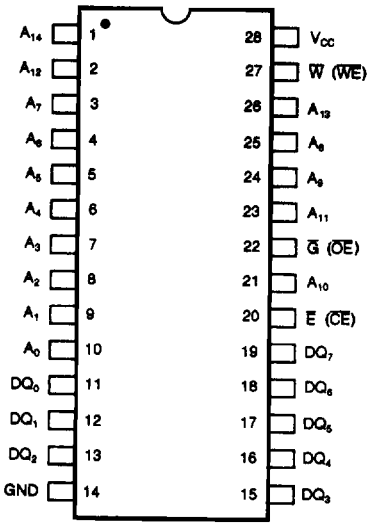
CONNECTION DIAGRAMS
Top View



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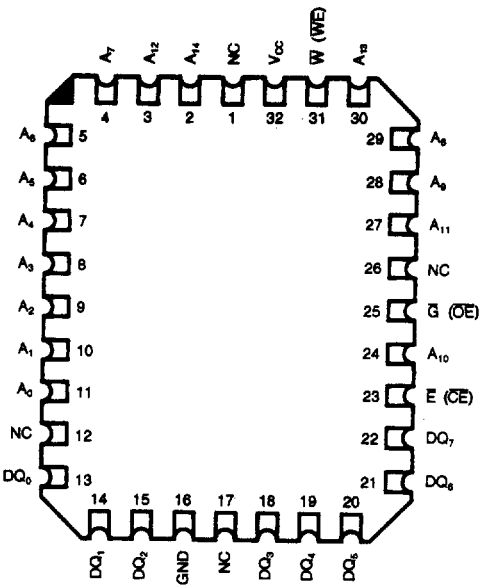

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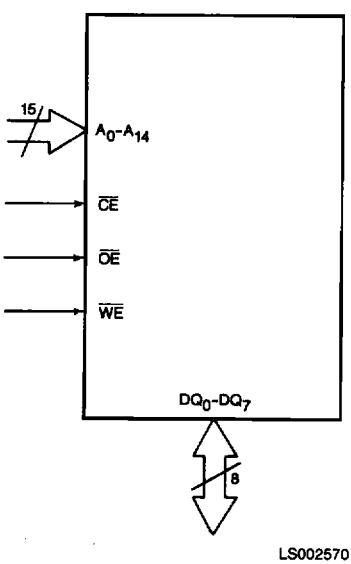
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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V_{CC} = Power Supply
GND = Ground

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FUNCTIONAL DESCRIPTION

Read Mode

The Am28C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable, $\overline{E}$ ($\overline{CE}$), is the power control and should be used for device selection. Output Enable, $\overline{G}$ ($\overline{OE}$), is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{E}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am28C256 has a standby mode which reduces the active power dissipation by 98%, from 300 mW to 5 mW (values for 0 to +70°C). The Am28C256 is placed in the standby mode by applying a TTL-HIGH signal to the $\overline{E}$ ($\overline{CE}$) input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{G}$ ($\overline{OE}$) input.

Power-Down Mode

The Am28C256 also has a power-down mode which reduces the power dissipation by 99.8% — from 300 mW to .5 mW (values for 0 to +70°C). The Am28C256 is placed in power down by raising $\overline{E}$ ($\overline{CE}$) to V_{CC} ±0.3 V.

Data Protection — Hardware

The Am28C256 incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.5 volts. It is the user's responsibility to ensure that the control levels are logically correct when V_{CC} is above 3.5 volts.

There is a $\overline{W}$ ($\overline{WE}$) lockout circuit that prevents $\overline{W}$ pulses of less than 20 ns duration from initiating a write cycle.

When the $\overline{G}$ ($\overline{OE}$) control is LOW (logic ZERO), a write cycle cannot be initiated.

Data Protection — Software

In addition to the hardware-protected write features provided on the Am28C256, the user may choose to implement software-write protect and minimize the chances of inadvertent writes.

The software-write protection has three modes of operation: set protection, write operation under protection, and disable protection.

Set Protection

The default power-up mode of the Am28C256 is with the protection disabled. The software-write protection is set by performing a three-byte write operation (with page-mode timing) using specific addresses and data.

TABLE 1. SET-PROTECTION MODE

Step	Mode	$A_{14} - A_0$	$I/O_7 - I/O_0$	Comment
1	Write	5555 Hex	AA Hex	Dummy Write
2	Write	2AAA Hex	55 Hex	Dummy Write
3	Write	5555 Hex	A0 Hex	Dummy Write

A violation of this sequence or the timeout of a 100-μs timer ($\overline{WE}$ transition LOW-to-HIGH starts the timer) aborts the set-protection operation.

The first time this sequence is applied to the part, a non-volatile bit is set. This reconfigures the part so that both software and hardware-protection are implemented. Once this bit is set, the software algorithm must be used every time a write cycle occurs.

Write Operation Under Protection

The write operation uses the same three steps to unlock the write protection for each byte-write, or page-write operation. Note that while under software write protection, a write can only be performed using page mode timing. Thus, a "byte write" is actually a four byte page write. The first three bytes unlock write protection (and are not written), while the fourth byte is the single byte to be written into the device.

TABLE 2. WRITE OPERATION UNDER PROTECTION MODE

Step	Mode	$A_{14} - A_0$	$I/O_7 - I/O_0$	Comment
1	Write	5555 Hex	AA Hex	Dummy Write
2	Write	2AAA Hex	55 Hex	Dummy Write
3	Write	5555 Hex	A0 Hex	Dummy Write
4 – 67	Write	Address	Data	Page-Load Writes

At the conclusion of the write cycle, the write operations to the Am28C256 are disabled. The page addresses ($A_6 - A_{14}$) should be held constant throughout the page-load operation (steps 4 – 67).

Disable Protection

The software protection can be disabled, and the part reconfigured to hardware-only protection, by using the operations shown in Table 3. Again, page mode timing must be used for all six bytes.

TABLE 3. DISABLE-PROTECTION MODE

Step	Mode	$A_{14} - A_0$	$I/O_7 - I/O_0$	Comment
1	Write	5555 Hex	AA Hex	Dummy Write
2	Write	2AAA Hex	55 Hex	Dummy Write
3	Write	5555 Hex	80 Hex	Dummy Write
4	Write	5555 Hex	AA Hex	Dummy Write
5	Write	2AAA Hex	55 Hex	Dummy Write
6	Write	5555 Hex	20 Hex	Dummy Write

The software-write protection is now disabled and the user has unrestricted write access to the Am28C256 — like on the Am2864B EEPROM.

Byte-Write Mode

To write into a particular location, addresses must be valid and a TTL LOW applied to the Write Enable ($\overline{W}$) pin of a selected ($\overline{E}$ LOW) device. This combined with Output Enable ($\overline{G}$) being HIGH, initiates a write cycle. During a byte-write cycle, all inputs except data are latched on the falling edge of $\overline{W}$ or $\overline{E}$, whichever occurred last. Data is latched on the rising edge of $\overline{W}$ or $\overline{E}$, whichever occurred first. An automatic erase is performed before data is written.

For system-design simplification, the Am28C256 is designed in such a way that either the $\overline{E}$ or $\overline{W}$ pin can be used to initiate a write cycle. The device uses the second HIGH-to-LOW transition of either $\overline{E}$ or $\overline{W}$ to latch addresses and the first LOW-to-HIGH transition to latch the data. For example, if $\overline{W}$ is used to initiate and terminate the write cycle, then $\overline{W}$ must go LOW after $\overline{E}$ goes LOW, and $\overline{W}$ must return HIGH before $\overline{E}$ goes HIGH. It is also permissible to mix control pins. As a second example, if $\overline{E}$ is used to initiate the write cycle and $\overline{W}$ is used to end the cycle, then $\overline{E}$ must go LOW after $\overline{W}$ goes LOW, and $\overline{W}$ must return HIGH before $\overline{E}$ goes HIGH. All address setup and hold times are with respect to the HIGH-to-LOW transition of the lagging control pin, and all data setup and hold times are with respect to the LOW-to-HIGH transition of the leading control pin.

To simplify the following discussion, the $\overline{W}$ pin is used as the write-cycle control pin throughout the rest of this data sheet.

Page-Write Mode

The page write allows from 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. The page-write mode consists of a load sequence, followed by an automatic write sequence.

During the load portion, sequential $\overline{W}$ ($\overline{WE}$) pulses load the byte address and the byte data into a 64-byte register; the bytes can be loaded into this register in any order. On each $\overline{W}$ pulse, the "Y" address is latched on the falling edge of $\overline{W}$, the data input is latched on the rising edge of $\overline{W}$, and the page address ($A_6 - A_{14}$) is latched on the falling edge of the last $\overline{W}$. Note that for a write to occur, $\overline{E}$ ($\overline{CE}$) and $\overline{W}$ ($\overline{WE}$) must be LOW, and $\overline{G}$ ($\overline{OE}$) must be HIGH. Although the page address ($A_6 - A_{14}$) is latched on the final $\overline{W}$ HIGH-to-LOW pulse (before t_{WW}), it is recommended that the page address be held steady during the entire page load. This is to ensure that an accidental software write protect sequence is not seen by the device. If the user chooses to change addresses during the page load, it is then the user's responsibility to make sure the three byte software algorithm is not accidentally sent to the device.

The automatic-write portion starts t_{WW} after the last transition of $\overline{W}$ from LOW-to-HIGH. If $\overline{W}$ transitions from HIGH-to-LOW before t_{WW} minimum (100 μs), the timer is reset and the automatic-write portion does not start. This is how the bytes are loaded into the register. If $\overline{W}$ is held LOW, this t_{WW} timer never starts and the write cycle is held indefinitely.

If $\overline{W}$ transitions from LOW-to-HIGH and stays HIGH for at least t_{WW} maximum, then the automatic-write sequence is initiated. Note that the load sequence can also be disabled if $\overline{G}$ ($\overline{OE}$) goes LOW. If $\overline{G}$ is LOW, attempts to load will be ignored. The part will time out if $\overline{G}$ ($\overline{OE}$) is held LOW longer than t_{WW} Max. and enter the automatic-write sequence.

The automatic-write sequence consists of an erase cycle — which erases any data that existed in each addressed cell, and a write cycle — which puts data back into the erased cells. Note that a page write will only write data to the locations selected during the page load and will not rewrite the entire page.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C ±5% ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line A_9 of the Am28C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28C256, these two identifier bytes are given in Table 5. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation.
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{E}$ ($\overline{CE}$) be decoded and used as the primary device-selecting function, while $\overline{G}$ ($\overline{OE}$) be made a common connection to all devices in the array and connected to the Read line from the system-control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Write-Operation Status Register

The Am28C256 features a Status-Bit register which can be used to poll the present state of the part. During a write cycle, a read to the Status register can be performed. Out of this register the toggle bit, the page-load timer, and $\overline{DATA}$ polling can be read.

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Toggle Bit (DQ_6)

The toggle bit is used to tell if the Am28C256 is still writing. The toggle bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device, as is required when using $\overline{DATA}$ polling. With each consecutive read, I/O_6 toggles. Therefore, two read operations must be performed to get the status.

Page-Load Timer (DQ_5)

The page-load timer tells the user if the page-write window (t_{WW}) has timed out, and the write cycle has commenced, or if it's still available to load data into. If I/O_5 is HIGH, the write cycle has begun; if it's LOW, t_{WW} has not timed out.

$\overline{DATA}$ Polling (DQ_7)

$\overline{DATA}$ polling requires a simple software routine that performs a read operation when the chip is in the automatic-write mode. The data that becomes valid during this $\overline{DATA}$ polling read is the inverse of DQ_7, last written to DQ_7. The true data (DQ_7) will become valid when the automatic write has been completed.

Endurance

Since endurance testing is a destructive test, it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data-retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point — when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide — the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant mortality failures to be screened out. For the next 20,000 to 30,000 write cycles, the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of 10^4 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD-test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability mechanisms are measured.

TABLE 4. Am28C256 MODE SELECT

MODE \ PINS	$\overline{E}$ ($\overline{CE}$)	$\overline{G}$ ($\overline{OE}$)	$\overline{W}$ ($\overline{WE}$)	A_9	OUTPUTS
Read	L	L	H	X	D_{OUT}
Write	L	H	L	X	D_{IN}
Standby/Write Inhibit	H	X	X	X	Hi-Z
Write Inhibit	X	L	X	X	
Write Inhibit	X	X	H	X	
Auto Select	L	L	H	V_H	CODE
$\overline{DATA}$ Polling	L	L	H	X	$DQ_7 - \overline{D_{IN7}}$

Key: L = LOW (V_L)
H = HIGH (V_H)
X = Don't Care
V_H = 12.0 V ±0.5 V

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed-circuit-board traces on EEPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −65 to +135°C
Voltage on All Inputs
with Respect to Ground, except A_9 ..+6.50 V to −0.6 V
Voltage on A_9
with Respect to Ground ..... +13.50 V to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −205, blank, −305, and −355 versions, V_{CC} = +4.75 to +5.25 V.
2. For −200, −250, −300, and −350 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V, $\overline{G}$ ($\overline{OE}$) = V_{IH}		10	μA
I_{CC3}	V_{CC} Current (Power Down)	$\overline{E}$ ($\overline{CE}$) = V_{CC} ±0.3 V		100	μA
I_{CC2}	V_{CC} Current (Standby)	$\overline{E}$ ($\overline{CE}$) = V_{IH}, $\overline{G}$ ($\overline{OE}$) = V_{IL}		1	mA
I_{CC1}	V_{CC} Current (Active)	$\overline{E}$ ($\overline{CE}$) = V_{IL}, $\overline{W}$ ($\overline{WE}$) = V_{IH}, f = 5 MHz, I_{OUT} = 0 mA (Note 3)		60	mA
I_{CC}	V_{CC} Current (Write)	$\overline{E}$ ($\overline{CE}$) = V_{IL}, $\overline{G}$ ($\overline{OE}$) = V_{IH}, $\overline{W}$ ($\overline{WE}$) = V_{IL}		60	mA
V_{IL}	Input LOW Voltage		−0.1	.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +1	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = 400 μA	2.4		V
V_{WI}	Write-Inhibit Voltage		3.5		V

CAPACITANCE (Notes 1 & 2)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4	10	pF
C_{OUT}	Output Capacitance	$\overline{G}$ ($\overline{OE}$) = $\overline{E}$ ($\overline{CE}$) = V_{IH}, V_{OUT} = 0 V	8	12	pF

Notes: 1. T_A = 25°C, f = 1 MHz
2. This parameter is sampled and not 100% tested.
3. This parameter is tested with $\overline{G}$ ($\overline{OE}$) = V_{IH} to simulate open outputs.

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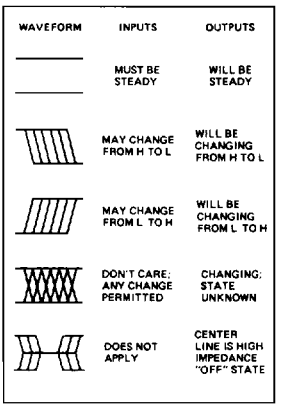
KEY TO SWITCHING WAVEFORMS



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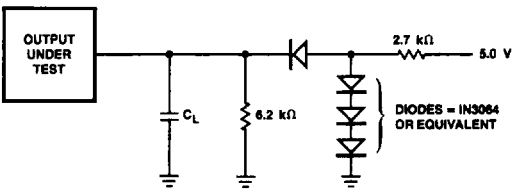
SWITCHING TEST CIRCUITS



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C_L = 100pF, including jig capacitance.

Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol JEDEC	Parameter Symbol Std.	Parameter Description	Test Conditions	28C256-205, -200 Min.	28C256-205, -200 Max.	28C256, -250 Min.	28C256, -250 Max.	28C256-305, -300 Min.	28C256-305, -300 Max.	28C256-355, -350 Min.	28C256-355, -350 Max.	Units
READ													
1	t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{E}$ ($\overline{CE}$) = $\overline{G}$ ($\overline{OE}$) = V_{IL}		200		250		300		350	ns
2	t_{ELQV}	t_{CE}	$\overline{E}$ to Output Delay	$\overline{G}$ ($\overline{OE}$) = V_{IL}		200		250		300		350	ns
3	t_{GLQV1}	t_{OE}	Output Enable to Output Delay	$\overline{E}$ ($\overline{CE}$) = V_{IL}		75		100		110		120	ns
4	t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 1)	Output Enable HIGH to Output Float	$\overline{E}$ ($\overline{CE}$) = V_{IL}	0	60	0	60		70	0	80	ns
5	t_{AXQX}	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{E}$ or $\overline{G}$ Whichever Occurred First	$\overline{E}$ ($\overline{CE}$) = $\overline{G}$ ($\overline{OE}$) = V_{IL}	0		0		0		0		ns
WRITE													
6		t_{AS}	Address to Write Setup Time		10		10		20		40		ns
7		t_{AH}	Address Hold Time		100		100		100		100		ns
8		t_{DS}	Data Setup Time		50		50		50		70		ns
9		t_{DH}	Data Hold Time		20		20		25		40		ns
10		t_{CS}	$\overline{E}$ to Write Setup Time		0		0		0		0		ns
11		t_{CH}	$\overline{E}$ Hold Time		0		0		0		0		ns
12		t_{OES}	$\overline{G}$ Setup Time		0		0		0		0		ns
13		t_{OEH}	$\overline{G}$ Hold Time		0		0		0		0		ns
14		t_{WP}	Write Pulse Width		100		100		120		150		ns
15		t_{WC}	$\overline{W}$ Cycle Time		1		1		1		1		µs
16		t_{WW}	Page Write Window (Note 2)		100	250	100	250	100	250	100	500	µs
17		t_{WH}	$\overline{W}$ Hold Time		100		100		120		150		ns
18		t_{WB}	Byte Write Cycle			10		10		10		10	ms
19		t_{RED}	Write Recovery from $\overline{DATA}$ Polling Time (Note 3)		0		0		0		0		µs
20		t_{SB}	$\overline{G}$ ($\overline{OE}$) LOW to Status Bit		150		150		150		150		ns
21		t_{OEW}	Write Control Recovery		50		50		50		50		ns
		(Note 1)	Number of Writes per Byte		10		10		10		10		x 1000

Notes: 1. This parameter is sampled and not 100% tested.
2. A timer of t_{WW} duration starts at every LOW-to-HIGH transition of $\overline{W}$ ($\overline{WE}$). If it is allowed to time out, a page write will start. A transition of $\overline{W}$ from HIGH to LOW will stop the timer.
3. This parameter is for information only. It is not tested or characterized.

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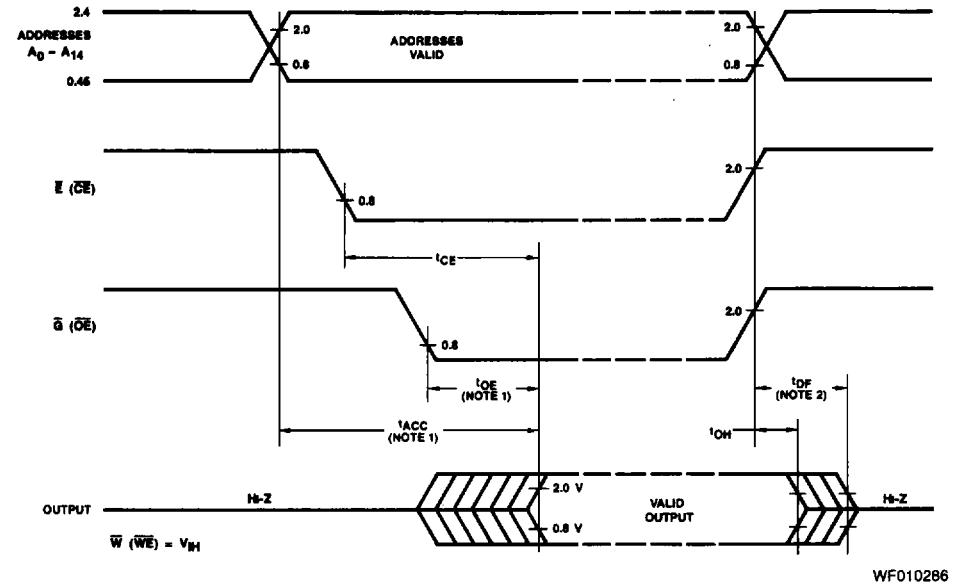
SWITCHING WAVEFORMS (Cont'd.)



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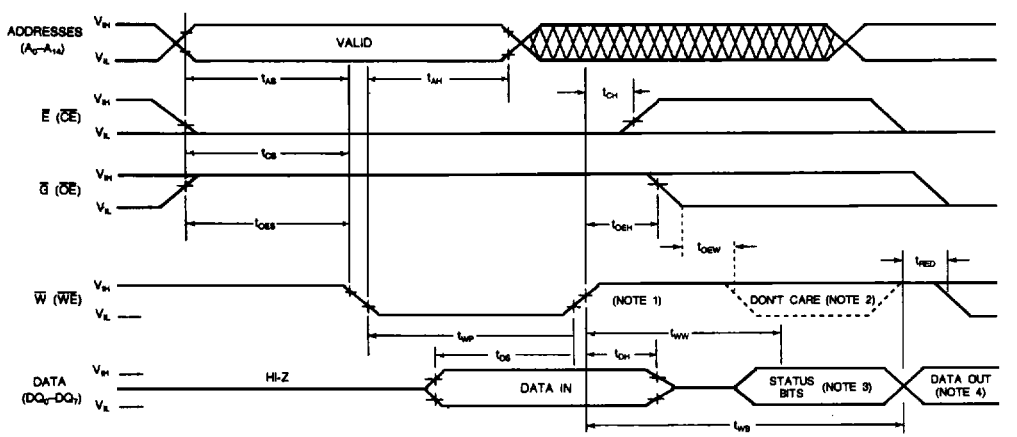
Read

Notes: 1. $\overline{G}$ ($\overline{OE}$) may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ ($\overline{CE}$) without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{G}$ ($\overline{OE}$) or $\overline{E}$ ($\overline{CE}$) whichever occurs first.



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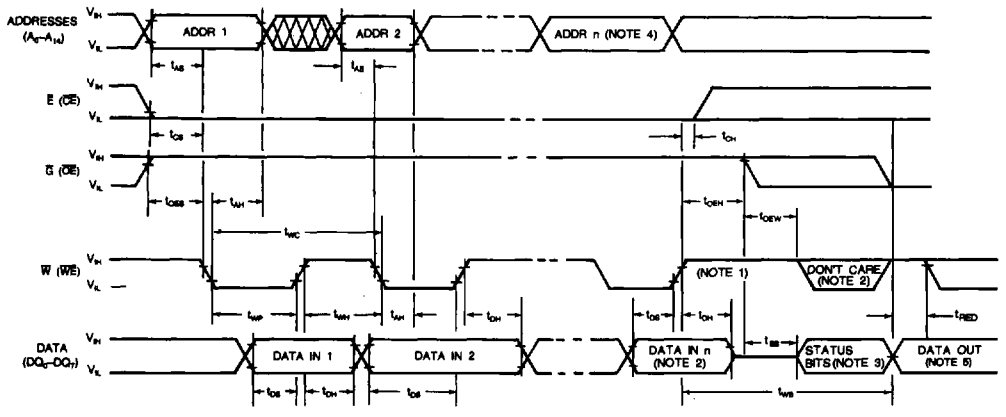
Byte — Write Timing

Notes: 1. To initiate the write cycle, one of the following write controls must be held for at least t_{WW} maximum: $\overline{W}$ ($\overline{WE}$) HIGH, $\overline{E}$ ($\overline{CE}$) HIGH, or $\overline{G}$ ($\overline{OE}$) LOW.
2. After being held HIGH for a minimum of $t_{OEW} + t_{OEH}$, $\overline{W}$ can be toggled LOW during the write cycle as long as one of the following conditions are met: $\overline{E}$ HIGH or $\overline{G}$ LOW.
3. This is where STATUS Bits are available. STATUS Bits are only available with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW.
4. Data is available only with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW.

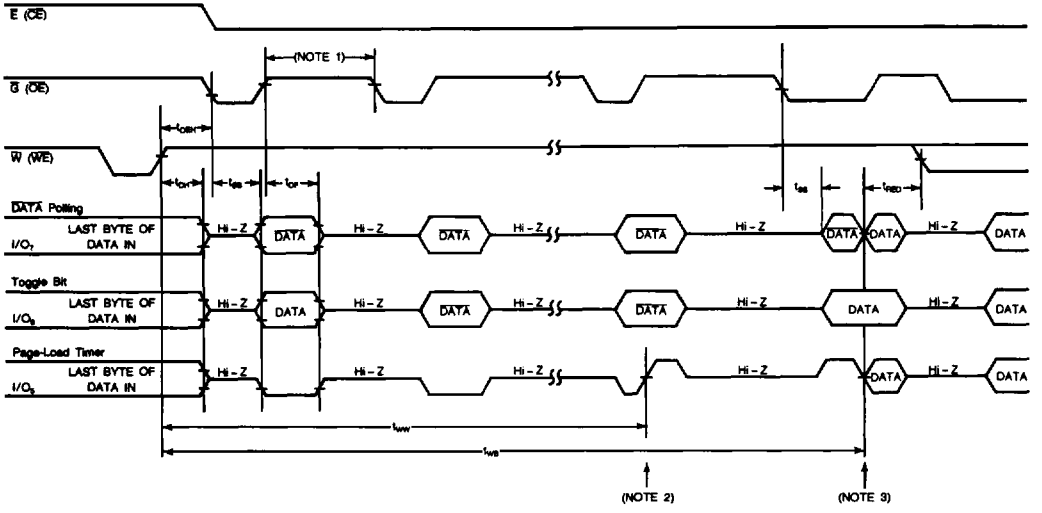
SWITCHING WAVEFORMS



WF020036

Page-Write Timing

Notes: 1. To initiate the page-write cycle, one of the following write controls must be held for at least t_{WW} maximum: $\overline{W}$ HIGH, $\overline{E}$ HIGH, or $\overline{G}$ LOW.
2. After being held HIGH for a minimum of t_{OEW}, $\overline{W}$ can be toggled LOW during the write cycle as long as one of the following conditions are met: $\overline{E}$ HIGH or $\overline{G}$ LOW.
3. This is where STATUS Bits are available. STATUS Bits are only available with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW. (See STATUS Bits Timing for setups.)
4. $n \leqslant 64$
5. Data is available only with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW.



WF022251

Write Operation STATUS Bit Timing

Notes: 1. $\overline{G}$ ($\overline{OE}$) HIGH Minimum 50 ns
2. Page load ends and internal write cycle starts here.
3. Internal write cycle ends and a fresh page load may be initiated here.

PROGRAMMING

Please refer to Table 5 for a summary of identifier bytes.

TABLE 5. IDENTIFIER BYTERS (Notes 1 & 2)

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am28C256 Device Code	V_{IH}	0	0	1	0	0	0	0	0	20

Key: 1 = Logic HIGH
0 = Logic LOW

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{E}$ ($\overline{CE}$), $\overline{G}$ ($\overline{OE}$) = V_{IL}
3. $\overline{W}$ ($\overline{WE}$) = V_{IH}