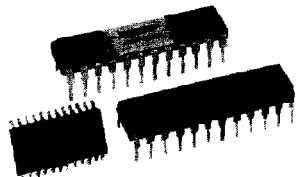


Or, Call Customer Service at 1-800-548-6132 (USA Only)



ADS7800

www.burr-brown.com/databook/ADS7800.html

12-Bit 3 μ s Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 333k SAMPLES PER SECOND
- STANDARD $\pm 10V$ AND $\pm 5V$ INPUT RANGES
- DC PERFORMANCE OVER TEMP:
No Missing Codes
1/2LSB Integral Linearity Error
3/4LSB Differential Linearity Error
- AC PERFORMANCE OVER TEMP:
72dB Signal-to-Noise Ratio
80dB Spurious-free Dynamic Range
-80dB Total Harmonic Distortion
- INTERNAL SAMPLE/HOLD, REFERENCE, CLOCK, AND 3-STATE OUTPUTS
- POWER DISSIPATION: 215mW max
- PACKAGE: 24-Pin Single-wide DIP
24-Lead SOIC

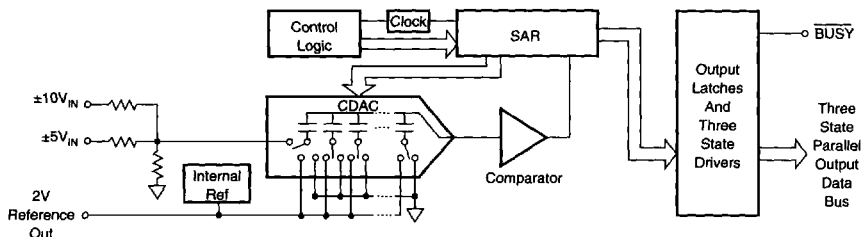
DESCRIPTION

The ADS7800 is a complete 12-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. It contains a complete 12-bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three-state output drivers.

The ADS7800 is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70 μ s max over temperature, and the high speed sampling input stage insures a total acquisition and conversion time of 3 μ s max over temperature. Precision, laser-trimmed scaling resistors provide industry-standard input ranges of $\pm 5V$ or $\pm 10V$.

AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.

The 24-pin ADS7800 is available in plastic and side-braze hermetic 0.3" wide DIPs, and in an SOIC package. It operates from a +5V supply and either a -12V or -15V supply. The ADS7800 is available in grades specified over 0°C to +70°C and -40°C to +85°C temperature ranges.



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PDS-1018E

2.133

ADS7800

A/D CONVERTERS, DATA ACQUISITION COMPONENTS

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = T_{MIN}$ to T_{MAX} , Sampling Frequency, $f_s = 333\text{kHz}$, $-V_S = -15\text{V}$, $V_S = +5\text{V}$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7800JP/JU/AH | | | ADS7800KP/KU/BH | | | UNITS |
|------------------------------------|-------------|-----------------|-----|------|-----------------|-----|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| TEMPERATURE RANGE Specification | JP/JU/KP/KU | 0 | | +70 | * | | * | °C |
| | AH/BH | -40 | | +85 | * | | * | °C |
| Operating Storage | JP/KP/JU/KU | -40 | | +85 | * | | * | °C |
| | | -65 | | +150 | * | | * | °C |

* Same as specification for ADS7800JP/JU/AH.

NOTES: (1) Adjustable to zero with external potentiometer. (2) LSB means Least Significant Bit. For ADS7800, 1LSB = 2.44mV for the $\pm 5\text{V}$ range, 1LSB = 4.88mV for the $\pm 10\text{V}$ range. (3) Noise was characterized over temperature near full scale, 0V, and negative full scale. 0.1LSB represents a typical rms level of noise at the worst case, which was near full scale input at $+125^\circ\text{C}$. (4) All specifications in dB are referred to a full-scale input, either $\pm 10\text{V}$ or $\pm 5\text{V}$. (5) For full scale step input, 12-bit accuracy attained in specified time. (6) Recovers to specified performance in specified time after $2 \times F_S$ input overvoltage.

ABSOLUTE MAXIMUM RATINGS

| | |
|--|-------------------------------|
| $-V_S$ to ANALOG COMMON | -16.5V |
| V_S to DIGITAL COMMON | +7V |
| Pin 23 (V_{SD}) to Pin 24 (V_{SA}) | $\pm 0.3\text{V}$ |
| ANALOG COMMON to DIGITAL COMMON | $\pm 1\text{V}$ |
| Control Inputs to DIGITAL COMMON | -0.3 to $V_S + 0.3\text{V}$ |
| Analog Input Voltage | $\pm 20\text{V}$ |
| Maximum Junction Temperature | 160°C |
| Internal Power Dissipation | 750mW |
| Lead Temperature (soldering, 10s) | $+300^\circ\text{C}$ |
| Thermal Resistance, θ_{JA} : | |
| Plastic DIP | 100°C/W |
| SOIC | 100°C/W |
| Ceramic | 50°C/W |



ELECTROSTATIC DISCHARGE SENSITIVITY

The ADS7800 is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PACKAGE/ORDERING INFORMATION

| PRODUCT | INTEGRAL LINEARITY ERROR (LSB) | SIGNAL-TO-(NOISE+DISTORTION) RATIO (dB min) | SPECIFICATION TEMPERATURE RANGE ($^\circ\text{C}$) | PACKAGE | PACKAGE DRAWING NUMBER ⁽¹⁾ |
|-----------|--------------------------------|---|--|---------------------|---------------------------------------|
| ADS7800JP | ± 1 | 67 | 0 to $+70$ | 24-Pin Plastic DIP | 243 |
| ADS7800KP | $\pm 1/2$ | 69 | 0 to $+70$ | 24-Pin Plastic DIP | 243 |
| ADS7800JU | ± 1 | 67 | 0 to $+70$ | 24-Pin Plastic SOIC | 239 |
| ADS7800KU | $\pm 1/2$ | 69 | 0 to $+70$ | 24-Pin Plastic SOIC | 239 |
| ADS7800AH | ± 1 | 67 | -40 to $+85$ | 24-Pin Ceramic DIP | 245 |
| ADS7800BH | $\pm 1/2$ | 69 | -40 to $+85$ | 24-Pin Ceramic DIP | 245 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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For Immediate Assistance, Contact Your Local Salesperson

PIN ASSIGNMENTS

| PIN # | NAME | DESCRIPTION |
|-------|-------------------|--|
| 1 | IN1 | ±10V Analog Input. Connected to GND for ±5V range. |
| 2 | IN2 | ±5V Analog Input. Connected to GND for ±10V range. |
| 3 | REF | +2V Reference Output. Bypass to GND with 22µF to 47µF Tantalum. Buffer for external loads. |
| 4 | AGND | Analog Ground. Connect to pin 13. |
| 5 | D11 | Data Bit 11. Most Significant Bit (MSB). |
| 6 | D10 | Data Bit 10. |
| 7 | D9 | Data Bit 9. |
| 8 | D8 | Data Bit 8. |
| 9 | D7 | Data Bit 7 if HBE is LOW; LOW if HBE is HIGH. |
| 10 | D6 | Data Bit 6 if HBE is LOW; LOW if HBE is HIGH. |
| 11 | D5 | Data Bit 5 if HBE is LOW; LOW if HBE is HIGH. |
| 12 | D4 | Data Bit 4 if HBE is LOW; LOW if HBE is HIGH. |
| 13 | DGND | Digital Ground. Connect to pin 4. |
| 14 | D3 | Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH. |
| 15 | D2 | Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH. |
| 16 | D1 | Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH. |
| 17 | D0 | Data Bit 0 if HBE is LOW. Least Significant Bit (LSB); Data Bit 8 if HBE is HIGH. |
| 18 | HBE | High Byte Enable. When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14-17, pins 9-12 output LOWs. Must be LOW to initiate conversion. |
| 19 | R/C | Read/Convert. Falling edge initiates conversion when \overline{CS} is LOW, HBE is LOW, and \overline{BUSY} is HIGH. |
| 20 | \overline{CS} | Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data. |
| 21 | \overline{BUSY} | Busy. Output LOW during conversion. Data valid on rising edge in Convert Mode. |
| 22 | -V _S | Negative Power Supply. -12V or -15V. Bypass to GND. |
| 23 | V _{SD} | Positive Digital Power Supply. +5V. Connect to pin 24, and bypass to GND. |
| 24 | V _{SA} | Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to GND. |

PIN CONFIGURATION

