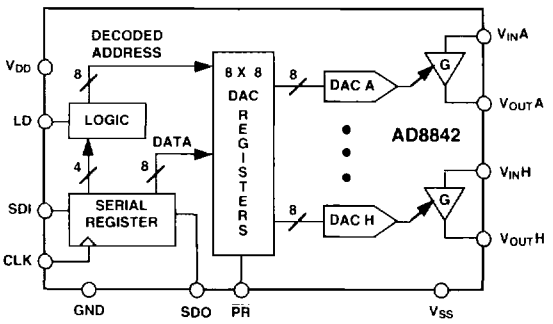
8-Bit Octal, 4-Quadrant Multiplying, CMOS TrimDAC

AD8842

FEATURES
Low Cost
Replaces 8 Potentiometers
50 kHz 4-Quadrant Multiplying Bandwidth
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 V Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Vertical Deflection Amplitude Adjustment
Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD8842 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC* capability allows replacement of the mechanical trimmer function in new designs. The AD8842 is ideal for ac or dc gain control of up to 50 kHz bandwidth signals. The four-quadrant multiplying capability is useful for signal inversion and modulation often found in video vertical deflection circuitry.

Internally the AD8842 contains eight voltage output digital-to-analog converters, each with separate voltage inputs. A new current conveyor amplifier design performs the four-quadrant multiplying function with a single amplifier at the output of the current steering digital-to-analog converter. This approach offers an improved constant input resistance performance versus previous voltage switched DACs used in TrimDAC circuits, eliminating the need for additional input buffer amplifiers.

Each DAC has its own DAC register that holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a registered trademark of Analog Devices, Inc.
The current conveyor amplifier is a patented circuit belonging to Analog Devices, Inc.

The AD8842 consumes only 95 mW from +5 V power supplies. For single 5 V supply applications consult the DAC8841. The AD8842 is pin compatible with the 1 MHz multiplying bandwidth DAC8840. The AD8842 is available in 24-pin plastic DIP and surface mount SOL-24 packages.

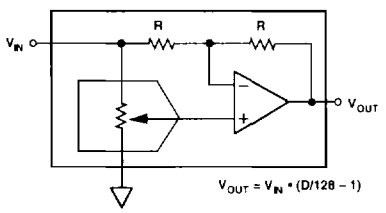

Figure 1. Functional Circuit of One 4-Quadrant Multiplying Channel

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option[2]
AD8842AN	XIND	24-Pin 300mil P-DIP	N-24
AD8842AR	XIND	24-Pin 300mil SOIC	SOL-24

NOTES
[1]XIND = -40°C to +85°C. The AD8842 contains 2452 transistors.
[2]For outline information see Package Information section.

AD8842–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V, V_{SS} = –5 V, All $V_{IN}x$ = +3 V, T_A = –40°C to +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY All Specifications Apply for DACs A, B, C, D, E, F, G, H						
Resolution	N		8			Bits
Integral Nonlinearity Error	INL			±0.2	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic		±0.4	±1	LSB
Full-Scale Gain Error	G_{FSE}			2		LSB
Output Offset	V_{OZE}	$\overline{PR}$ = 0, Sets D = 80_H		5	25	mV
Output Offset Drift	TCV_{OZ}	$\overline{PR}$ = 0, Sets D = 80_H		5		µV/°C
VOLTAGE INPUTS—Applies to All Inputs $V_{IN}x$						
Input Voltage Range[1]	IVR		±3	±4		V
Input Resistance	R_{IN}		12	19		kΩ
Input Capacitance	C_{IN}			9		pF
DAC OUTPUTS Applies to All Outputs $V_{OUT}x$						
Voltage Range[1]	OVR	R_L = 10 kΩ	±3	±4		V
Output Current	I_{OUT}	ΔV_{OUT} < 1.5 LSB	±3			mA
Capacitive Load	C_L	No Oscillation		500		pF
DYNAMIC PERFORMANCE Applies to All DACs						
Full Power Gain Bandwidth[1]	GBW	$V_{IN}x$ = ±3 V_p, R_L = 2 kΩ, C_L = 10 pF	10	50		kHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}x$ = +5.5 V	0.5	1.0		V/µs
Negative	SR–	$\Delta V_{OUT}x$ = –5.5 V	1.0	1.8		V/µs
Total Harmonic Distortion	THD	$V_{IN}x$ = 4 V p-p, D = FF_H, f = 1 kHz, f_{LPF} = 80 kHz, R_L = 1 kΩ		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz, V_{IN} = 0 V		78		nV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 00_H to FF_H		2.9		µs
		D = FF_H to 00_H		5.4		µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz		72		dB
Digital Feedthrough	Q	$V_{IN}x$ = 0 V, D = 0 to 255_{10}		5		nV-s
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		10	14	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		9	13	mA
Power Dissipation[2]	P_{DISS}			95	135	mW
Power Supply Rejection	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0001	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS} \rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7		pF
Input Coding				Offset Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS[1]						
Input Clock Pulse Width	t_{CH}, t_{CL}		60			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				80	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTES

[1]Guaranteed by design, not subject to production test.

[2]Calculated limit = 5 V × (I_{DD} + I_{SS}).

Specifications subject to change without notice