

## 3.8A, 250V LOGIC N-CHANNEL MOSFET

### ■ DESCRIPTION

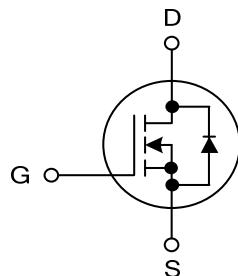
The UTC 5N25 is an N-Channel enhancement MOSFET, it uses UTC's advanced technology to provide customers with a minimum on-state resistance, high switching speed and low gate charge. It can also withstand high energy pulse in the avalanche and commutation modes.

The UTC 5N25 is suitable for high efficiency switching DC/DC converter, motor control and switch mode power supply.

### ■ FEATURES

- \*  $R_{DS(ON)} < 1.2\Omega$  @  $V_{GS} = 10V$
- \* Low gate charge ( Typ=14nC)
- \* Low  $C_{RSS}$  ( Typ=6.0pF)
- \* High switching speed

### ■ SYMBOL



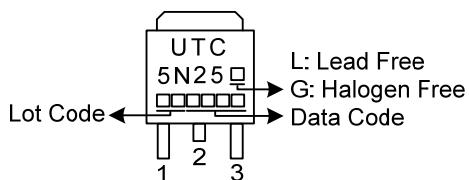
### ■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5N25L-TN3-T	5N25G-TN3-T	TO-252	G	D	S	Tube
5N25L-TN3-R	5N25G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

5N25L-TN3-T 	(1) Packing Type (2) Package Type (3) Lead Free	(1) T: Tube, R: Tape Reel (2) TN3: TO-252 (3) L: Lead Free, G: Halogen Free
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### ■ MARKING INFORMATION



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ\text{C}$ , unless otherwise noted)

PARAMETER SYMBOL		RATINGS	UNIT	
Drain-Source Voltage	$V_{DSS}$	250	V	
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V	
Drain Current	Continuous I <sub>D</sub>	3.8	A	
	Pulsed (Note 2)	I <sub>DM</sub> 9	A	
Avalanche Current (Note 2)	I <sub>AR</sub>	3.8	A	
Avalanche Energy	Single Pulsed (Note 3)	E <sub>AS</sub> 85	mJ	
	Repetitive (Note 2)	E <sub>AR</sub>	3.7	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5.5	V/ns	
Power Dissipation	$T_A=25^\circ\text{C}$	P <sub>D</sub>	2.5	W
	$T_C=25^\circ\text{C}$		37	W
	Derate above 25°C		0.29	W/°C
Junction Temperature	T <sub>J</sub> -55~	+150	°C	
Storage Temperature Range	T <sub>STG</sub> -55~	+150	°C	

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

1. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L=6.2mH, I<sub>AS</sub>=3.8A, V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C.
4. I<sub>SD</sub>≤4.5A, di/dt≤300A/μs, V<sub>DD</sub>≤BV<sub>DSS</sub>, Starting T<sub>J</sub>=25°C.

■ THERMAL CHARACTERISTICS

PARAMETER SYMBOL		RATINGS	UNIT
Junction to Ambient (Note)	$\theta_{JA}$	50 °C/W	
Junction to Ambient		110	°C/W
Junction to Case	$\theta_{JC}$	3.4	°C/W

Note: When mounted on the minimum pad size recommended (PCB Mount)

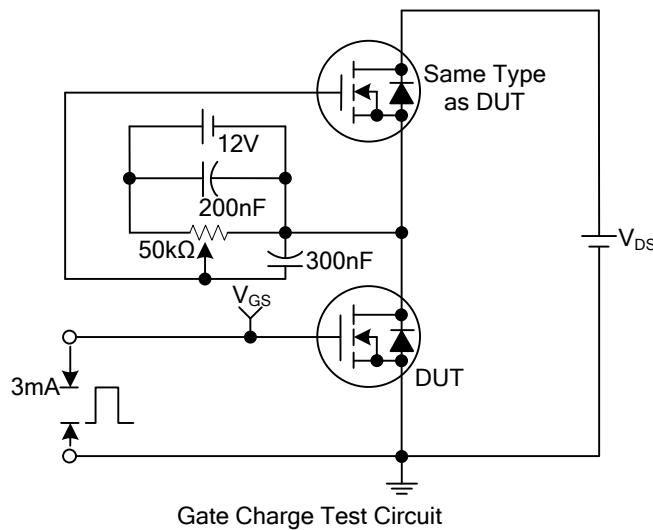
■ ELECTRICAL CHARACTERISTICS ( $T_C=25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	250			V
Breakdown Voltage Temperature Coefficient	$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	Reference to $25^\circ\text{C}$ , $I_D=250\mu\text{A}$		0.18		$\text{V}^\circ\text{C}$
Drain-Source Leakage Current	$I_{\text{DSS}}$	$V_{DS}=250\text{V}, V_{GS}=0\text{V}$		1		$\mu\text{A}$
Gate-Source Leakage Current	<div style="display: flex; align-items: center;"> <span>Forward</span> <span style="margin: 0 10px;"></span> <span><math>I_{\text{GSS}}</math></span> </div>	$V_{GS}=+20\text{V}, V_{DS}=0\text{V}$		+100		nA
	<div style="display: flex; align-items: center;"> <span>Reverse</span> <span style="margin: 0 10px;"></span> <span><math>V_{GS}</math></span> </div>	$V_{GS}=-20\text{V}, V_{DS}=0\text{V}$		-100		nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$		4		V
Static Drain-Source On-State Resistance (Note 1)	$R_{\text{DS(ON)}}$	<div style="display: flex; align-items: center;"> <span><math>V_{GS}=10\text{V}, I_D=1.9\text{A}</math></span> <span style="margin: 0 10px;"></span> <span>0.74</span> </div> <div style="display: flex; align-items: center;"> <span><math>V_{GS}=5\text{V}, I_D=1.9\text{A}</math></span> <span style="margin: 0 10px;"></span> <span>0.92</span> </div>	1.2	1.25		$\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{DS}=30\text{V}, I_D=1.9\text{A}$	3.35			S
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{\text{ISS}}$	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1.0\text{MHz}$	250	325		pF
Output Capacitance	$C_{\text{OSS}}$		40	50		pF
Reverse Transfer Capacitance	$C_{\text{RSS}}$		6	8		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{GS}=5\text{V}, V_{DS}=160\text{V}, I_D=4.5\text{A}$ (Note 1, 2)	14	20		nC
Gate to Source Charge	$Q_{GS}$		1.2			nC
Gate to Drain Charge	$Q_{GD}$		2.4			nC
Turn-ON Delay Time	$t_{\text{D(ON)}}$	$V_{DD}=100\text{V}, I_D=4.5\text{A}, R_G=25\Omega$ (Note 1, 2)	28	40		ns
Rise Time	$t_R$		24	80		ns
Turn-OFF Delay Time	$t_{\text{D(OFF)}}$		80	110		ns
Fall-Time	$t_F$		20	90		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$			3.8		A
Maximum Body-Diode Pulsed Current	$I_{\text{SM}}$			9		A
Drain-Source Diode Forward Voltage	$V_{SD}$	$I_S=3.8\text{A}, V_{GS}=0\text{V}$		1.5		V
Body Diode Reverse Recovery Time	$t_{\text{RR}}$	$I_S=4.5\text{A}, V_{GS}=0\text{V}, dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)	95			ns
Body Diode Reverse Recovery Charge	$Q_{\text{RR}}$		0.3			$\mu\text{C}$

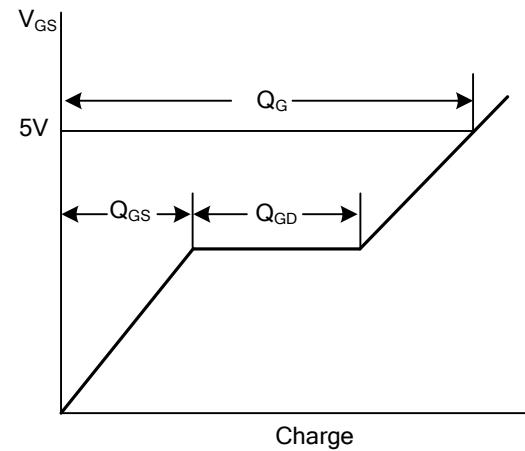
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

2. Essentially independent of operating temperature

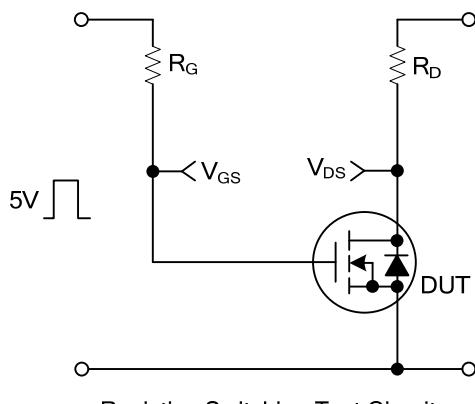
■ TEST CIRCUITS AND WAVEFORMS



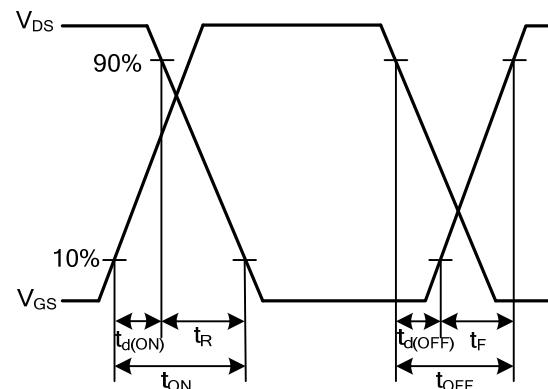
Gate Charge Test Circuit



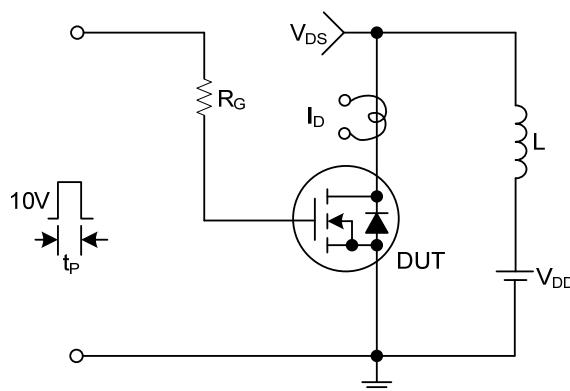
Gate Charge Waveforms



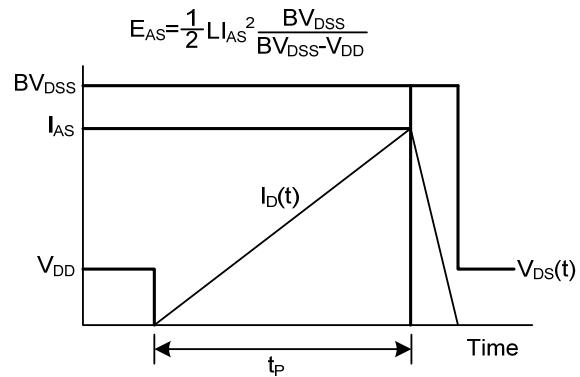
Resistive Switching Test Circuit



Resistive Switching Waveforms

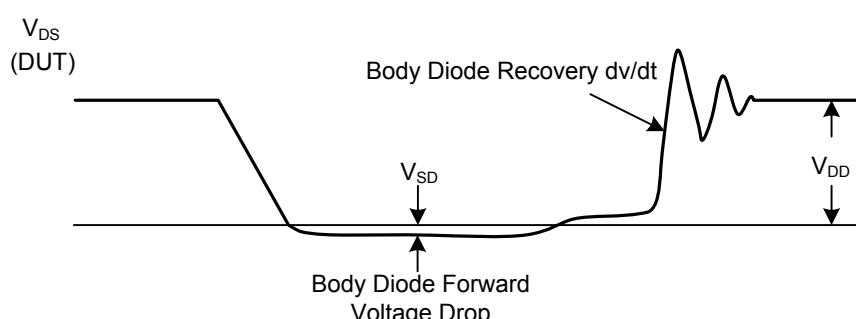
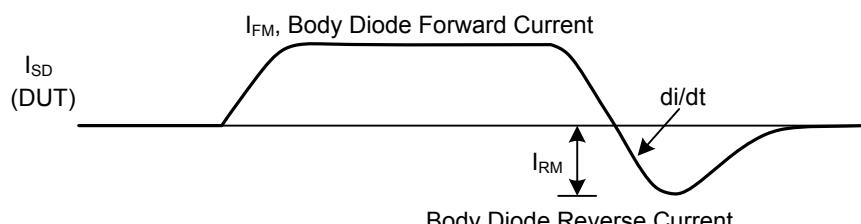
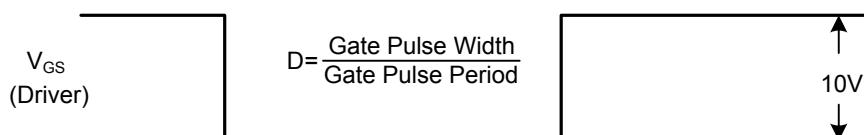
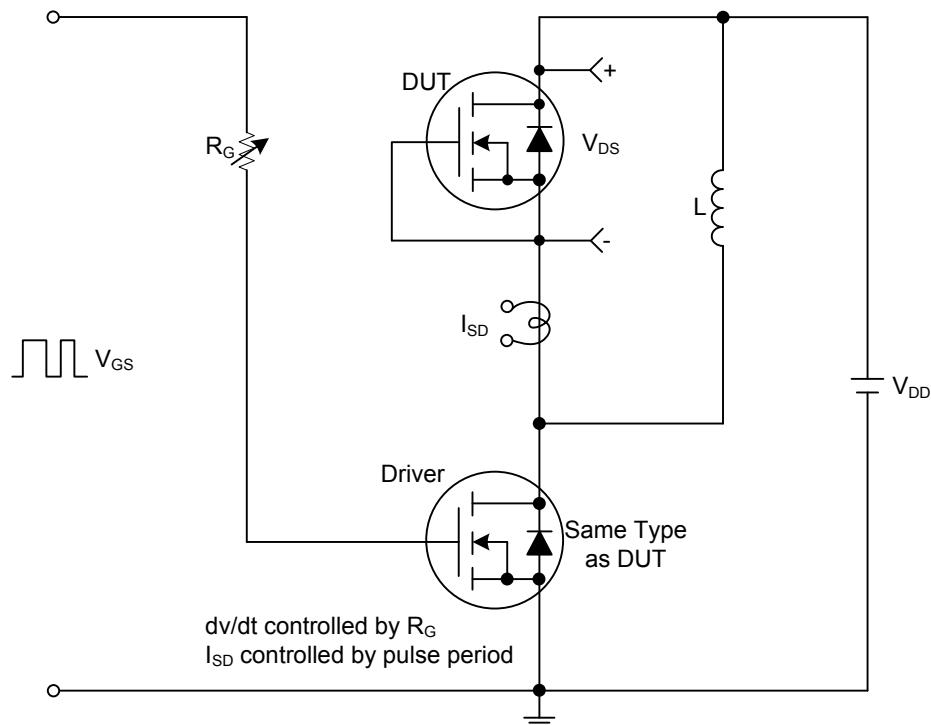


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery  $dv/dt$  Test Circuit and Waveforms

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