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12-Port DS3/E3/STS-1 Electrical Integrated Line Termination Device for Transport Networks

M29320 – Single Chip Solution

The M29320 provides a complete physical-layer solution for flexible high-bandwidth DS3/E3 services, including secure private leased lines and video conferencing. The M29320 replaces up to 3 discrete devices, enabling cost-effective DS3/E3 services to be deployed in both new and existing platforms.

The M29320 includes 12 independent DS3/E3/STS-1E electrical line interface units (LIUs) with built-in digital jitter attenuators (DJAT), 24 DS3/E3 framers (12x in receive and 12x in transmit for monitoring only), and 12 STS-1 framers. Each port is capable of supporting DS3/E3/STS-1E mapped/demapped signals to/from SONET/SDH interface.

The M29320 line side interfaces support electrical DS3/E3/STS-1E, requiring only the addition of transformers and passive termination.

The M29320 system interface supports STS-12/STM-4 for the SONET/SDH traffic via dual high speed serial LVDS (622 Mbps) interfaces as active and protect, or a standard 8-bit, 77 MHz TDM telecom bus.

Granularity of service is an important feature of this device. It can take a channelized OC-12 connection and break it all the way down to DS3/E3 streams.

KEY FEATURES

- High-density - 12 DS3/E3/STS-1 LIUs with jitter attenuation/desynchronization
- 24 DS3/E3 framers
- 12 DS3/E3 mappers/demappers
- 12 STS-1 SONET/SDH framers
- STS-12/STM-4 SONET/SDH TDM framer
- Parallel 8-bit, 77.76 MHz TDM Telecom Bus
- Dual high speed serial LVDS 622 MHz interface
- Dual embedded OC-12 CDRs

Densely channelized OC-12 line cards, enabled by the M29320, are becoming enormously popular at the edge of the network as carriers backhaul all their traffic to an access Point-of-Presence (POP) where they will terminate the customer traffic in an edge router or multiservice switch before transporting it onto the internet SONET/SDH backbone.

The M29320 integrates 12 DS3/E3/STS-1E mapper/framers, with corresponding field-proven desynchronizers using DSP technology (DJAT) and an STS-12/STM-4 SONET/SDH framer, to support DS3/E3/STS-1E mapping into SONET/SDH on a channel-by-channel basis. This allows ADMs/OEDs and MSPPs to deploy a single line card that supports the simultaneous mapping and transport of both DS3 and E3, which is significant for European and Asian carriers as their networks have a mix of DS3 and E3 that must be transported across their SDH infrastructure.

In addition, the M29320 supports Pseudo-Random Bit Sequence testing, and a full set of loopback functions are provided at different functional blocks.

The M29320 requires only one 19.44 MHz reference clock (passive crystal) or seven 7.76/155.52 MHz SONET reference clocks for generating all the necessary internal line rate clocks and enabling the same reference clock to be available on an output pad. The M29320 is offered in a 35mm FCBGA package.
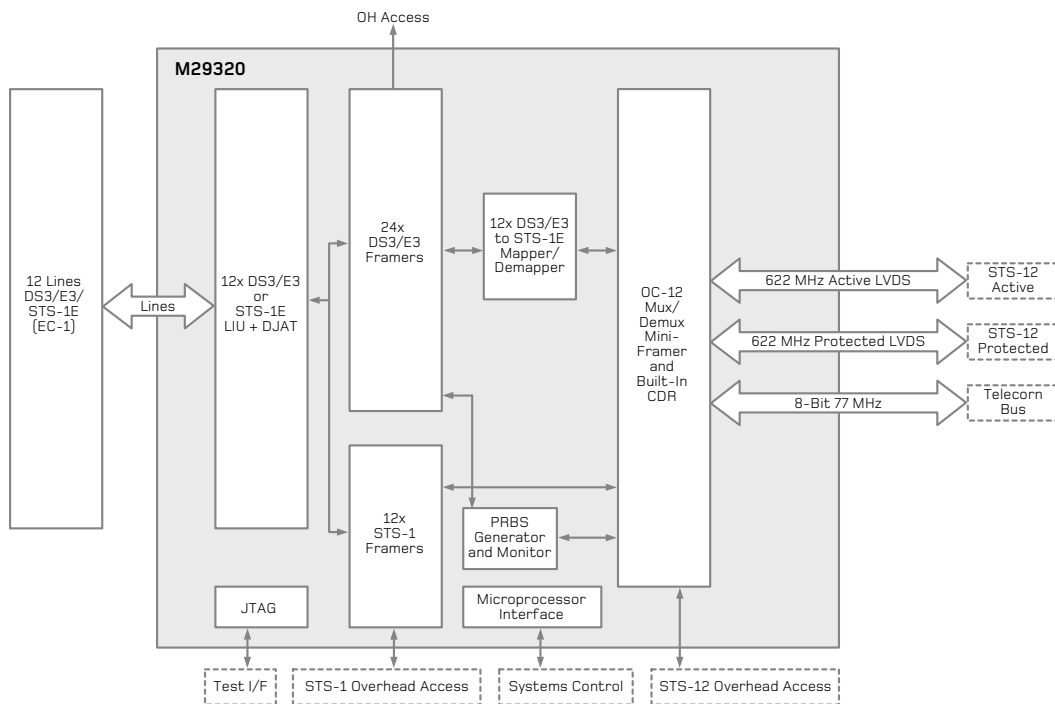
M29320 Functional Block Diagram

Product Features

- **12 DS3/E3/STS–1E LIUs with jitter attenuation/desynchronization**
  - Fully adaptive receive equalizer enables greater than 1800 ft of cable reach
  - Fully programmable transmit pulse mask configuration
  - Dynamic loop bandwidth to comply with all SONET and Bell Core intrinsic and output jitter requirements
- **24 DS3/E3 framers support DS3–M13, DS3–M23, DS3 C–bit parity E3–G.751, E3–G.832**
- **12 DS3/E3 mappers/demappers supporting DS3/VC–3/AU–3; DS3/TUG–3/AU–4; E3/VC–3/AU–3; E3/TUG–3/AU–4**

- **12 STS–1 SONET/SDH framers support transport overhead access; includes monitor and generator**
- **STS–12/STM–4 SONET/SDH TDM supporting mapping/demapping of 12 STS–1E or AU–3 into/from STS–12/STM–4 frame**
  - Pointer processing
  - Transport overhead insertion and extraction
  - Parallel 77.76 MHz x 8–bit Telecom bus interface
  - Dual serial LVDS 622 MHz Bus interface with embedded CDR with support for no–bit–loss switching

- **Synchronous 16–bit microprocessor interface bus at 30–77 MHz bus rate**
- **Local (source) and remote (line) loopback capability at various internal points in the device**
- **PRBS detector and generator supporting framed and unframed modes**
- **JTAG (IEEE 1149.1) boundary scan**
- **Single rail 1.8 V core supply with 3.3 V LvTTL I/O, 1.8V LVDS I/O**
- **Embedded CLADs internally generating the three line rate (DS3/E3/STS–1) clocks**

Applications
- **ADM/OEDs**
- **DSLAM & NGDLC**
- **Digital Access Cross–Connect Systems**

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