32-Position Manual Up/Down Control Potentiometer

Preliminary Technical Data

AD5228

FEATURES

- 32-Position Digital Potentiometer
- 10k, 50k, 100kΩ end-to-end terminal resistance
- Simple Manual Up/Down Push Button Control
- Built-in Adaptive De-bouncer
- Discrete Step Counts Up/Down
- Fast Scan Counts Up/Down 4 Steps Per Seconds
- Zeroscale/Midscale Selectable Preset
- Low Potentiometer Mode Tempco 5ppm/°C
- Low Rheostat Mode Tempco 35ppm/°C
- Internal Pull-Up Resistors
- Digital Control Compatible
- Low power, I_{DD} = 5μA Max
- Low Operating Voltage, 2.7V to 5.5V
- Automotive Temperature Range -40°C to +105°C
- Compact Thin SOT23-8 (2.9 mm × 3 mm) package

APPLICATIONS

- Mechanical Potentiometers and Trimmers Replacements
- LCD Contrast, Brightness, and Backlight Controls
- Digital Volume Control
- Portable Devices Level Adjustments
- Electronics Front Panel Level Controls
- Programmable Power Supply

GENERAL DESCRIPTIONS

AD5228 is Analog Devices latest 32-Step Up/Down Control Digital Potentiometer[1] emulating mechanical potentiometer operation. Its simple up/down control interface allows manual control with just two external pushbutton switches. AD5228 designed with a built-in adaptive de-bouncer that ignores any invalid bounces due to the spring-load rebounce mechanism commonly found in pushbuttons during contact closure. The de-bouncer is adaptive that can accommodate variety of mechanical switches with irregular bouncing mechanisms.

In addition, AD5228 can be counted up and down in discrete step or in fast scanning mode. When the $\overline{PU}$ or $\overline{PD}$ button is briefly pressed and released, AD5228 resistance changes by one step. Repeat pressing and releasing the button change the numbers of steps accordingly. When $\overline{PU}$ or $\overline{PD}$ button is held continuously, the device will change to the fast scan mode after 1 second and count 4 steps per second thereafter.

In addition to manual control, AD5228 can be controlled digitally and its up/down control features simplify discrete logics or micro-controller control. The up down inputs have internal pull-up resistors which ensure proper logic operation.

The AD5228 is available in compact thin SOT23-8 package. All parts are guaranteed to operate over the automotive temperature range of -40°C to +105°C.

AD5228 simple interface, small footprint, and very low cost enable it to be the potential replacements of mechanical potentiometers and trimmers with typically 3X improved resolution, solid-state reliability, and fast adjustment. These enhancements can result in considerable cost saving in end users' systems.

For users who consider EEMEM potentiometers, they may refer to some recommendations in the Applications Section.

FUNCTIONAL BLOCK DIAGRAMS

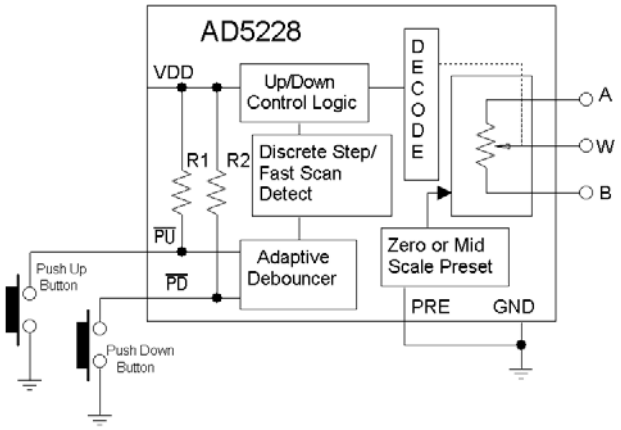
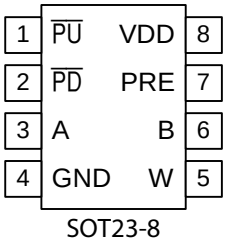


Figure 1. AD5228 Functional Block Diagrams

Table 1. Truth Table

$\overline{PU}$	$\overline{PD}$	Operation
0	0	R_{WB} and R_{WA} Do Not Change
0	1	R_{WB} Increment, R_{WA} Decrement
1	0	R_{WB} Decrement, R_{WA} Increment
1	1	R_{WB} and R_{WA} Do Not Change

Pin Configuration



SOT23-8

Figure 2. AD5228 Package and Pin Configuration

Note.1. The term digital potentiometer and RDAC are used interchangeably.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

TABLE OF CONTENTS

REVISION HISTORY

Revision PrC: Initial Version

Table 2. ELECTRICAL CHARACTERISTICS 10k , 50k, 100kΩ VERSION (V_{DD} = +3V±10% or +5V±10%, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +105°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A=NC	-1	±0.25	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC	-1	±0.5	+1	LSB
Nominal resistor tolerance	$\Delta R_{AB}/R_{AB}$	T_A = 25°C	-30		30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 5V		120	200	Ω
Wiper Resistance	R_W	$I_W = V_{DD}/R$, V_{DD} = 2.7V		200	400	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Resolution	N				5	Bits
Integral Nonlinearity[3]	INL		–1	±0.5	+1	LSB
Differential Nonlinearity[3,4]	DNL		–1	±0.1	+1	LSB
Voltage Divider Temp Coefficient	$(\Delta V_W/V_W)/\Delta T$	Mid-scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	+16 Steps from Mid-scale (Full-scale)	–2	-0.5	+0	LSB
Zero-Scale Error	V_{WZSE}	-16 Steps from Mid-scale (Zero-scale)	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		0		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Mid-scale		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Mid-scale		60		pF
Common Mode Leakage	I_{CM}	$V_A = V_B = V_W$		1		nA
$\overline{PU}$ & $\overline{PD}$ INPUTS						
Input High	V_{IH}	V_{DD} = +5V	2.4			V
Input Low	V_{IL}	V_{DD} = +5V			0.8	V
Input Current	I_{IL}	V_{IN} = 0V or +5V			1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		+2.7		+5.5	V
Supply Current Standby	I_{DD_STBY}	V_{DD} = +5V			5	µA
Supply Current Active	I_{DD_ACT}	V_{DD} = +5V, $\overline{PU}$ or $\overline{PD}$ is held		50		µA
Power Dissipation[7]	P_{DISS}	V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V			25	µW
Power Supply Sensitivity	PSS	•V_{DD} = +5V ±10%		0.05	0.15	%/%
DYNAMIC CHARACTERISTICS[6,9,10]						
Built-in Debounce & Settling Time	t_{DB}			10		ms
Fast Scan Start Time	t_{FSS}	$\overline{PU}$ or $\overline{PD}$ is held		1		s
Fast Scan Time	t_{FS}	$\overline{PU}$ or $\overline{PD}$ is held		0.25		s
Bandwidth –3dB	BW	R_{AB} = 10k/50k/100kΩ, Mid-scale		600/X/Y		kHz
Total Harmonic Distortion	THD_W	V_A =1Vrms + 2V dc, V_B = 2V DC, f=1KHz		0.05		%
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5KΩ, f = 1kHz		14		nV•Hz

NOTES:

1. Typicals represent average readings at +25°C, V_{DD} = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure X XX test circuit.
3. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0V.
4. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions. See Figure XXX test circuit.
5. Resistor terminals A,B,W have no limitations on polarity with respect to each other.
6. Guaranteed by design and not subject to production test.
7. P_{DISS} is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation.
8. Bandwidth, noise and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value result in the minimum overall power consumption.
9. All dynamic characteristics use V_{DD} = +5V.
10. See timing diagram for location of measured values. All input control voltages are specified with t_R=t_F=1ns(10% to 90% of V_{DD}) and timed from a voltage level of 1.6V. Switching characteristics are measured using both V_{DD} = +5V.

Absolute Maximum Ratings

Table 3. AD5228 Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	–0.3, +7V
V_A, V_B, V_W to GND	GND, V_{DD}
Maximum Current	
I_{WB}, I_{WA} Pulsed	±20mA
I_{WB} Continuous (R_{WB} ≤ 1 kΩ, A open) [1]	±5mA
I_{WA} Continuous (R_{WA} ≤ 1 kΩ, B open) [1]	±5mA
Digital Input Voltage to GND	0V, V_{DD}
Operating Temperature Range	–40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 – 30 sec)	245°C
Thermal Resistance[2] θ_{JA},	230°C/W

[1]Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. V_{DD} = 5 V.
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Package Power Dissipation = (T_JMAX – T_A) / θ_{JA}

Pin Configurations And Functional Descriptions

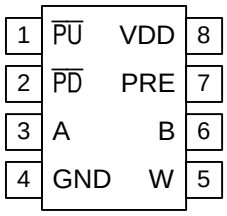


Figure 3. SOT23-8

Table 3. Pin Function Descriptions

Pin No.	Name	Description
1	$\overline{PU}$	Push Up Pin. Connect To External Push Button. Active Low
2	$\overline{PD}$	Push Down Pin. Connect To External Push Button. Active Low
3	A	Resistor Terminal A. GND≤V_A≤V_{DD}
4	GND	Common Ground
5	W	Wiper Terminal W. GND≤V_W≤V_{DD}
6	B	Resistor Terminal B. GND≤V_B≤V_{DD}
7	PRE	Power On Preset. Tie to Ground for Mid-scale and V_{DD} for Zero-scale Presets. Do Not Let PRE Pin Floating
8	V_{DD}	Positive Power Supply, +2.7 V to +5.5 V

Interface Timing Diagram

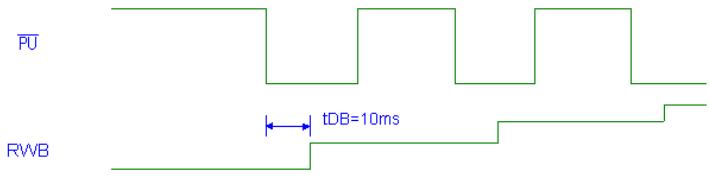


Figure 4.Step Up R_{WB} in Discrete Steps

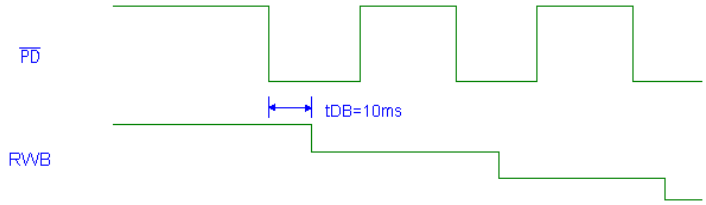


Figure 5. Step Down R_{WB} in Discrete Steps

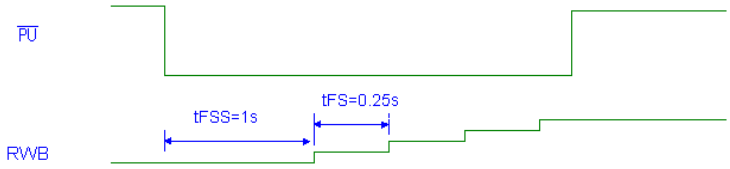


Figure 6. Step Up R_{WB} In Fast Scan Mode

.

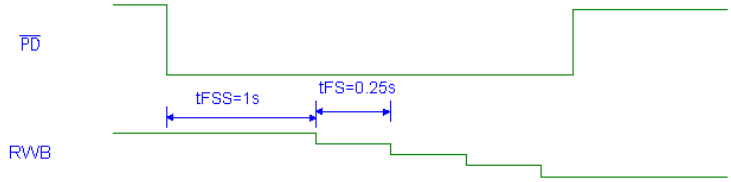


Figure 7. Step Down R_{WB} in Fast Scan Mode

OPERATION

The AD5228 is a 32-position manual up/down control digital potentiometer with selectable power on preset. AD5228 presets to Mid-scale when the PRE pin is tied to ground and Zero-scale when PRE is tied to V_{DD}. Floating the PRE pin is not allowed. The step up and step down operations require the manipulations of the $\overline{PU}$ (push up) and $\overline{PD}$ (push down) pins. These pins have internal pull-up resistors that the $\overline{PU}$ and $\overline{PD}$ activate at low. The common practices are applying external pushbuttons or tactile switches as shown in Figure 8. Because of the spring load re-bounce mechanism in most pushbutton switches, a single pushbutton press can generate numerous bounces during the contact closure, see Figures 9 and 10.

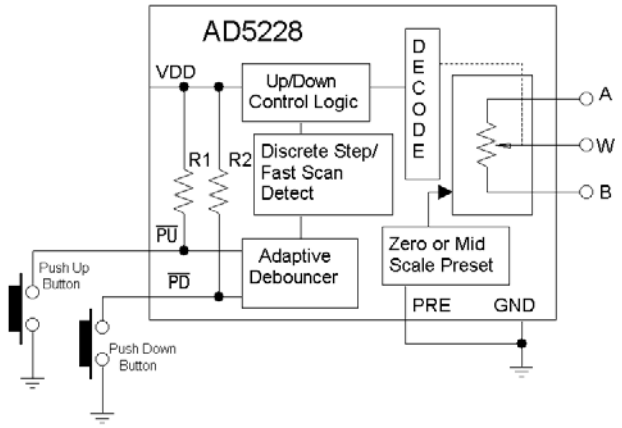


Figure 8. Typical Pushbuttons Interface

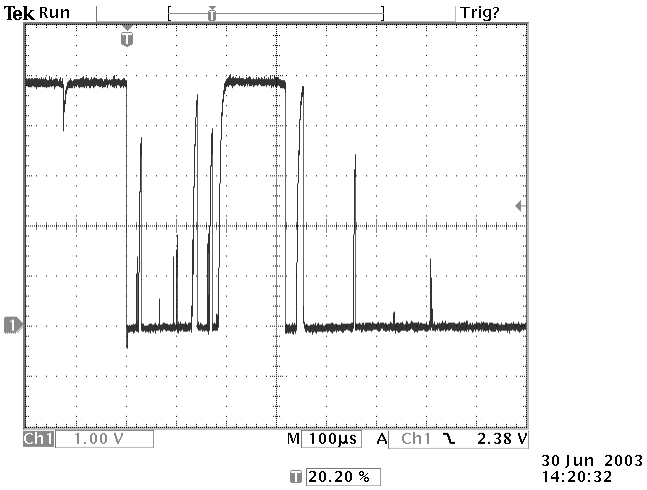


Figure 9. Typical Pushbutton Switch Initial Bouncing

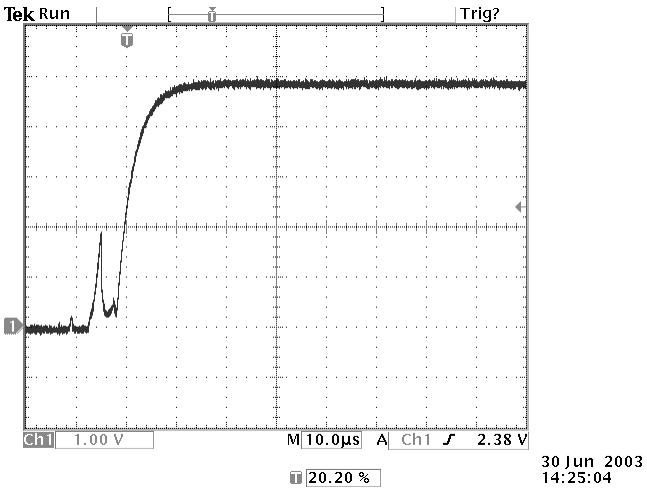


Figure 10. Typical Pushbutton Switch Tail Bouncing

AD5228 features adaptive de-bounce function, the de-bouncer works by monitoring and timing all the bounces. If the durations, between the bounces, are shorter than 10ms, the de-bouncer ignores the bounces and continues to look for the last bounce. When the off state after a bounce reaches 10ms, the de-bouncer will recognize it as the last bounce, therefore allows AD5228 to change the resistance by one step. The timing requirements are shown in Figures 4-7. The AD5228 de-bouncer is carefully designed that is capable to handle most standard pushbutton switches in the market.

Pressing the $\overline{PU}$ or $\overline{PD}$ button once increment or decrement R_{WB} by one step respectively. Repeat pressing these buttons separately and discretely for fast adjustment is allowed provided each press is not faster than 10ms (Fast video game players can achieve approximately 40ms per press). On the other hand, AD5228 comes with a fast scan feature such that when $\overline{PU}$ or $\overline{PD}$ button is held continuously, the fast scan mode is activated after 1 second and AD5228 will change the resistance 4 steps per second thereafter. The change will stop when it hits at either ends of the resistor string unless the opposite button is pressed. The timing informations given are based on the typical values which may vary ±30%.

When both $\overline{PU}$ and $\overline{PD}$ buttons are pressed simultaneously, the output will not change but it will change once one button is let go earlier than another.

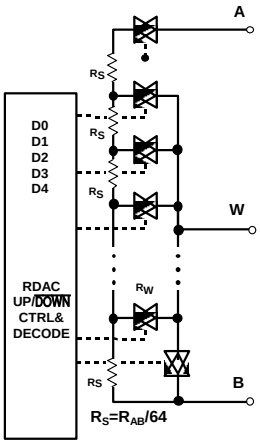


Figure 11. AD5228 Equivalent RDAC Circuit

PROGRAMMING THE DIGITAL POTENTIOMETERS

Rheostat Operation

If only the W-to-B or W-to-A terminals are used as variable resistor, the unused terminal can be opened or shorted with W, such operation is called rheostat mode, Figure 12.

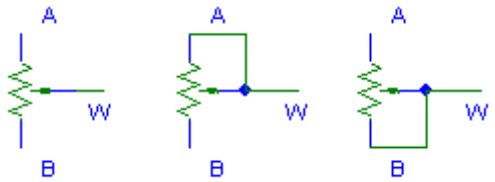


Figure 12. Rheostat Mode Configuration

The end-to-end resistance R_{AB} has 32 contact points accessed by the wiper terminal, plus the B terminal contact if R_{WB} is used. Pushing the $\overline{PU}$ pin discretely increments R_{WB} by one step from B to W. The total resistance becomes Rs + Rw, see Figure 11. The change of resistance, R_{WB} can be determined by the number of discrete $\overline{PU}$ executions provided its maximum and minimum settings are not reached. The R_{WB} can therefore be approximated as

$$\Delta R_{WB} = +\left(\overline{PU} \cdot \frac{R_{AB}}{32} + R_W\right) \quad (1)$$

$$\Delta R_{WB} = -\left(\overline{PD} \cdot \frac{R_{AB}}{32} + R_W\right) \quad (2)$$

where:
$\overline{PU}$ is the number of Discrete Push Up Executions.
$\overline{PD}$ is the number of Discrete Push Down Executions
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on-resistance of the internal switch.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a complementary resistance R_{WA}. When these terminals are used, the B-terminal can be opened or shorted to W. The R_{WA} can also be approximated if its maximum and minimum settings are not reached.

$$\Delta R_{WA} = -\left((32 - \overline{PU})\frac{R_{AB}}{32} + R_W\right) \quad (3)$$

$$\Delta R_{WA} = +\left((32 - \overline{PD})\frac{R_{AB}}{32} + R_W\right) \quad (4)$$

Equations 1 to 4 do not apply when $\overline{PU}$ and $\overline{PD}$ = 0.

Since in the lowest end of the resistor string, a finite wiper resistance of 60Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

The typical distribution of the resistance tolerance from device to device is process lot dependent and is possible to have ±30% tolerance.

Potentiometer Mode Operation

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation, Figure 13.

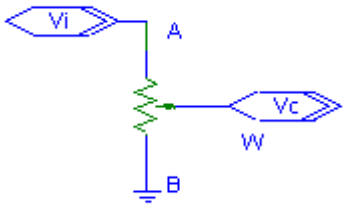


Figure 13. Potentiometer Mode Configuration

The transfer function is:

$$\Delta V_W = \frac{\frac{\overline{PU}}{32}R_{AB} + R_W}{R_{AB} + 2R_W}V_A \quad (5)$$

If we ignore the effect of the wiper resistance, the transfer function simplifies to

$$\Delta V_W = +\frac{\overline{PU}}{32}V_A \quad (6)$$

$$\Delta V_W = -\frac{\overline{PD}}{32}V_A \quad (7)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratio-metric function of $\overline{PU}$/32 or $\overline{PD}$/32 with a relatively small error contributed by the R_W terms, the tolerance effect is therefore almost cancelled. Although the thin film step resistor R_S and CMOS switches resistance R_W have very different temperature coefficients, the ratio-metric adjustment also makes the overall temperature coefficient effect reduced to 5ppm/°C except at low value codes where R_W dominates.

Potentiometer mode operations include others such as opamp input and feedback resistors network and other voltage scaling applications. A, W, and B terminals can in fact be input or output terminals and have no polarity constraint provided that $|V_{AB}|$, $|V_{WA}|$, and $|V_{WB}|$ do not exceed VDD-to-GND.

CONTROLLING INPUTS

All $\overline{PU}$ and $\overline{PD}$ inputs are protected with a series input resistor and parallel Zener ESD structure shown in Figure 14.

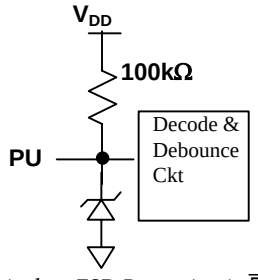


Figure 14. Equivalent ESD Protection in $\overline{PU}$ and $\overline{PD}$ Pins

Terminal Voltage Operation Range

The AD5228 is designed with internal ESD diodes for protection but they also set the voltage boundary of the terminal operating voltages. Positive signals present on terminal A, B, or W that exceeds V_{DD} will be clamped by the forward biased diode. There is no polarity constraint between V_A, V_W, and V_B but they cannot be higher than V_{DD} or lower than GND.

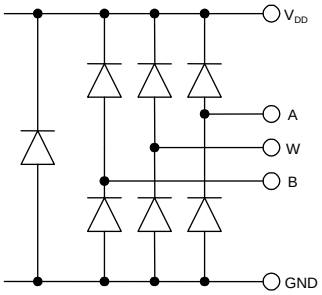


Figure 15. Maximum Terminal Voltages Set by V_{DD} and GND

Power-Up and Power-Down Sequences

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (Figure 15), it is important to power V_{DD} before applying any voltage to terminals A, B, and W. Otherwise, the diodes will be forward biased such that V_{DD} will be powered unintentionally and may affect the rest of the users' circuit. Similarly, V_{DD} should be powered down last. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}.

Layout and Power Supply Biasing

It is always a good practice to employ compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low ESR (Equivalent Series Resistance) 1µF to 10µF tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple. Figure 16 illustrates the basic supply-bypassing configuration for the AD5228

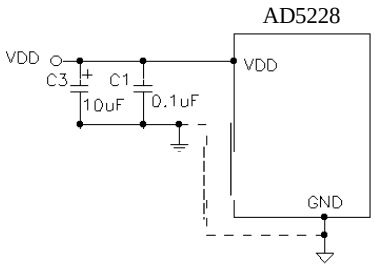


Figure 16. Power Supply Bypassing

The ground pin of the AD5228 is a digital ground reference. To minimize the digital ground bounce, the AD5228 ground terminal should be joined remotely to the common ground, Figure 16.

Applications

Constant Bias To Retain Resistance Setting

For users who consider EEMEM pots but cannot justify the additional cost for their designs, they may consider AD5228 as low cost alternatives. They may constantly bias the AD5228 with the supply to retain the resistance setting. AD5228 is designed specifically with low power in mind that allows power conservation even in the battery-operated systems. As shown in Figure 17, a similar low power digital pot is applied in a 3.4V 450mAhour Li-ion cellphone battery. The measurement shows that the device drains negligible power. Constantly bias the pot is not an impractical approach because most of the portable devices nowadays do not require detachable batteries for charging purpose. Although the resistance setting of AD5228 will be lost when the battery needs replacement, such event occurs infrequently that such inconvenience is justified for most applications. And when it happens, user should be provided with a mean to adjust the setting accordingly.

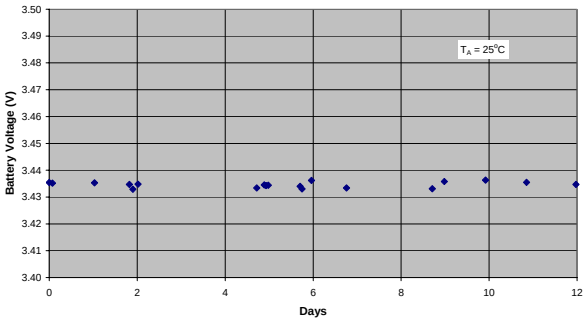


Figure 17. Battery Consumption Measurement.

Outline Dimensions

Dimensions shown in inches and (mm)

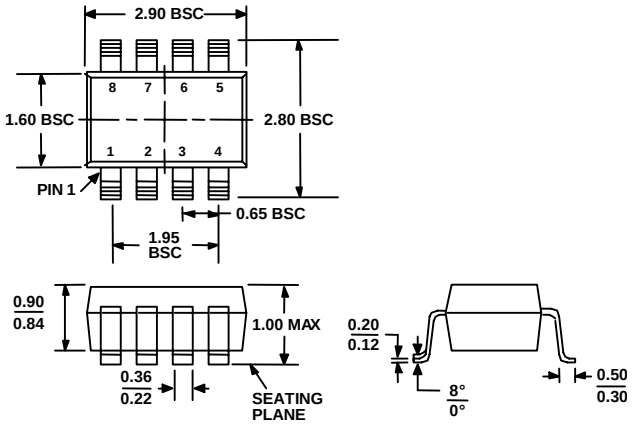


Figure 18. 8-Lead Small Outline Transistor Package [Thin SOT-23] (UJ-8)
Dimensions shown in millimeters

Table 1. Ordering Guide

Model[1]	R_{AB} (kΩ)	Temperature Range	Package Code	Package Description	Full Container Quantity	Brand
AD5228BUJ10-R7	10	-40°C to +105°C	UJ	SOT23-8	3000	D3K
AD5228BUJ10	10	-40°C to +105°C	UJ	SOT23-8	250	D3K
AD5228BUJ50-R7	50	-40°C to +105°C	UJ	SOT23-8	3000	D3L
AD5228BUJ50	50	-40°C to +105°C	UJ	SOT23-8	250	D3L
AD5228BUJ100-R7	100	-40°C to +105°C	UJ	SOT23-8	3000	D3M
AD5228BUJ100	100	-40°C to +105°C	UJ	SOT23-8	250	D3M
AD5228EVAL	10				1	

1. Z=Pb Free Parts

The end-to-end resistance RAB is available in 10kΩ, 50kΩ, and 100kΩ . The final three characters of the part number determine the nominal resistance value, e.g., 10kΩ =10.