DRAM MODULE

256K x 9 DRAM

FAST PAGE MODE (MT3D2569)
LOW POWER,
EXTENDED REFRESH (MT3D2569 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW (.9mW L-version) standby; 625mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 60µA maximum (L-version)

OPTIONS

	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
• Access Mode	
FAST PAGE MODE	P
• Power/Refresh	
Normal Power/8ms	Blank
Low Power/64ms	L

- Part Number Example: MT3D2569MPL-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM (T-2) — MT3D2569MP

Vcc	1	16	DQ5
CAS	2	17	A8
DQ1	3	18	NC
A0	4	19	NC
A1	5	20	DQ6
DQ2	6	21	WE
A2	7	22	Vss
A3	8	23	DQ7
Vss	9	24	PRD
DQ3	10	25	DQ8
A4	11	26	Q9
A5	12	27	RAS
DQ4	13	28	CAS9
A6	14	29	D9
A7	15	30	Vcc

30-Pin SIP (S-2) — MT3D2569NP

Vcc	1	16	DQ5
CAS	2	17	A8
DQ1	3	18	NC
A0	4	19	NC
A1	5	20	DQ6
DQ2	6	21	WE
A2	7	22	Vss
A3	8	23	DQ7
Vss	9	24	PRD
DQ3	10	25	DQ8
A4	11	26	Q9
A5	12	27	RAS
DQ4	13	28	CAS9
A6	14	29	D9
A7	15	30	Vcc

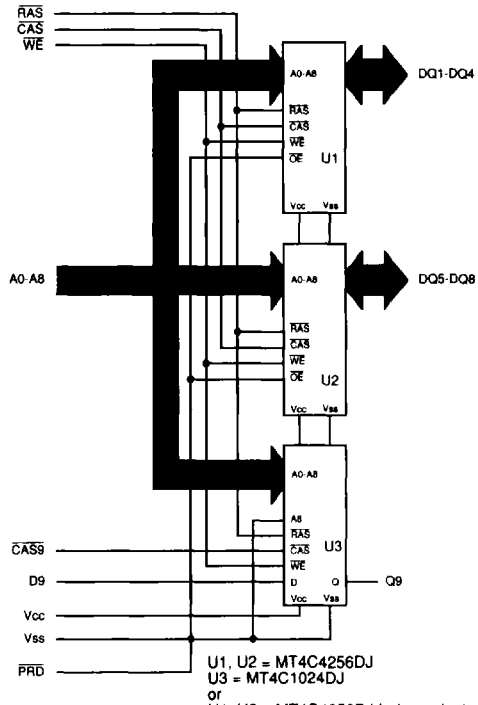
GENERAL DESCRIPTION

The MT3D2569 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered nine bits (A0-A8) at a time. RAS is used to latch the first nine bits and CAS the latter nine bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES tR	ADDRESSES tC	DATA IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V_{IN} ≤ V_{CC}, (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A8, $\overline{RAS}$, $\overline{WE}$	I_I	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	DQ1-DQ8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)		V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	6	6	6	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	3	3	3	mA	24
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)		.6	.6	.6	mA	24, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current	I_{CC3}	270	240	210	mA	2, 22
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		255	225	195	mA	2,22,26
OPERATING CURRENT: FAST PAGE MODE Average power supply current	I_{CC4}	210	180	150	mA	2, 22
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN))		195	165	135	mA	2,22,26
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current	I_{CC5}	270	240	210	mA	2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))		255	225	195	mA	2, 26
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current	I_{CC6}	270	240	210	mA	2, 19
($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))		255	225	195	mA	2,19,26
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ = 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left OPEN), ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	.6	.6	.6	mA	26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		19	pF	17
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	17
Input Capacitance: D9	C_{I3}		10	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		15	pF	17
Output Capacitance: Q9	C_O		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	40		40		45		ns	
PAGE-MODE READ or WRITE cycle time	^tPC	n/a		n/a		n/a		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
Access time from $\overline{CAS}$ (FAST PAGE MODE)	^tCAC		20		20		20	ns	9
Output Enable	^tOE		20		20		20	ns	
Access time from column address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	30	15	35	15	40	ns	24
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		15		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	25
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	25

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

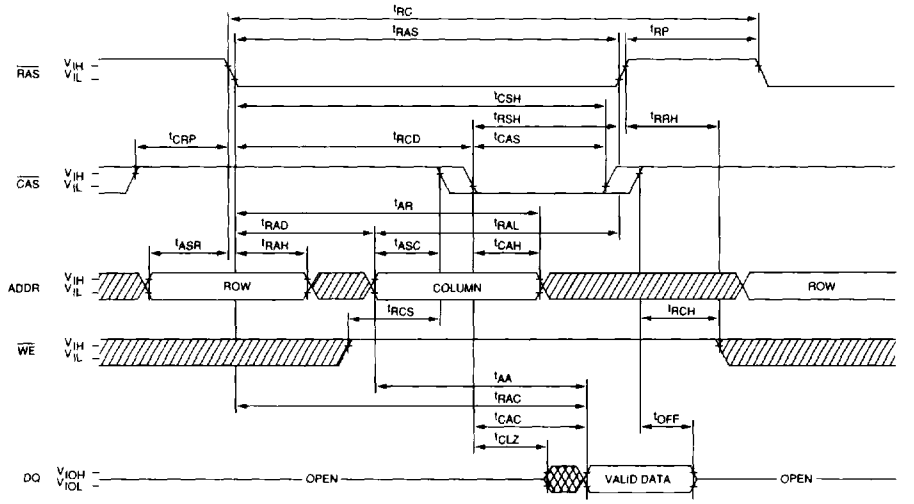
(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
Write command pulse width	^tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		20		ns	
Data-in setup time	^tDS	0		0		0		ns	15
Data-in hold time	^tDH	15		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^tREF		8/64		8/64		8/64	ms	3/26
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	^tCHR	10		15		15		ns	19

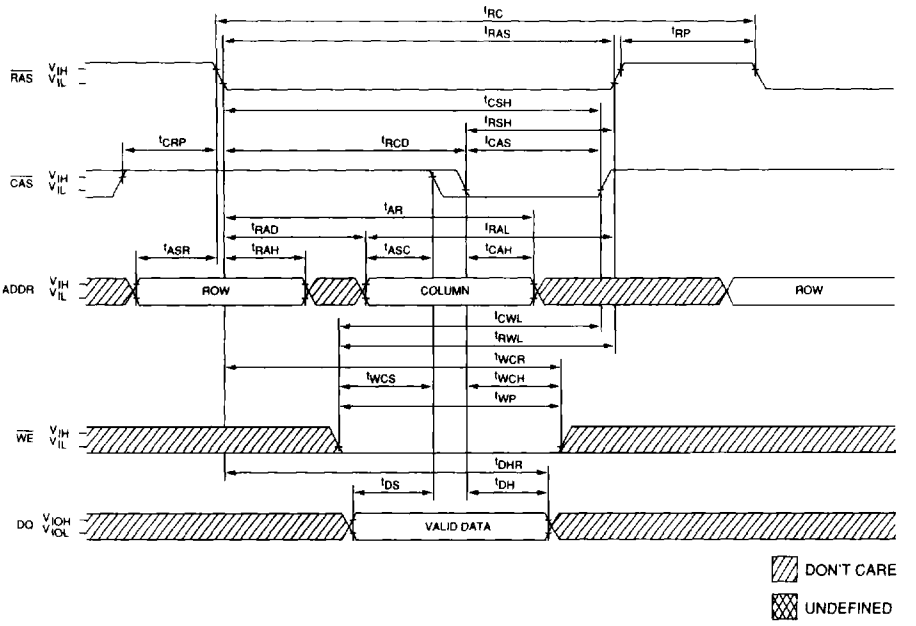
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that $^{t}RCD \ge {}^{t}RCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 andU2.
22. I_{CC} is dependent on cycle rates.
23. All other inputs at V_{CC} -0.2V.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
25. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
26. Applies to L-version only.

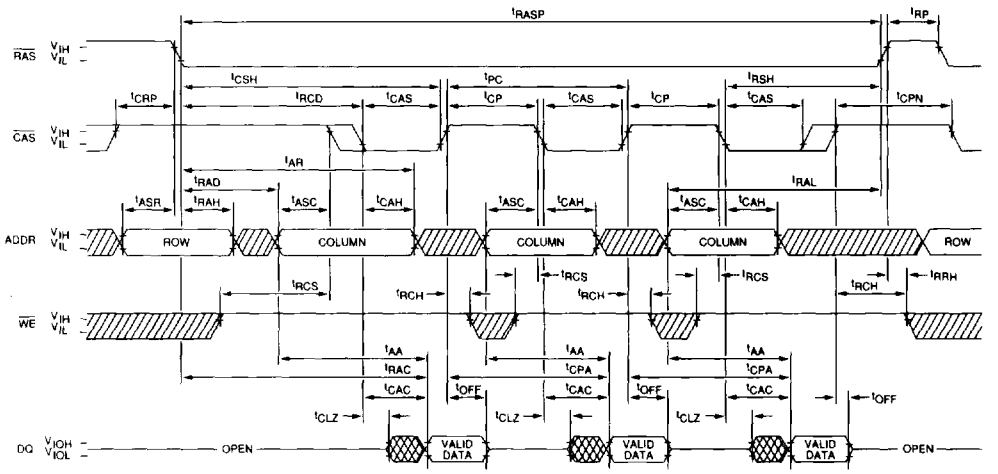
READ CYCLE



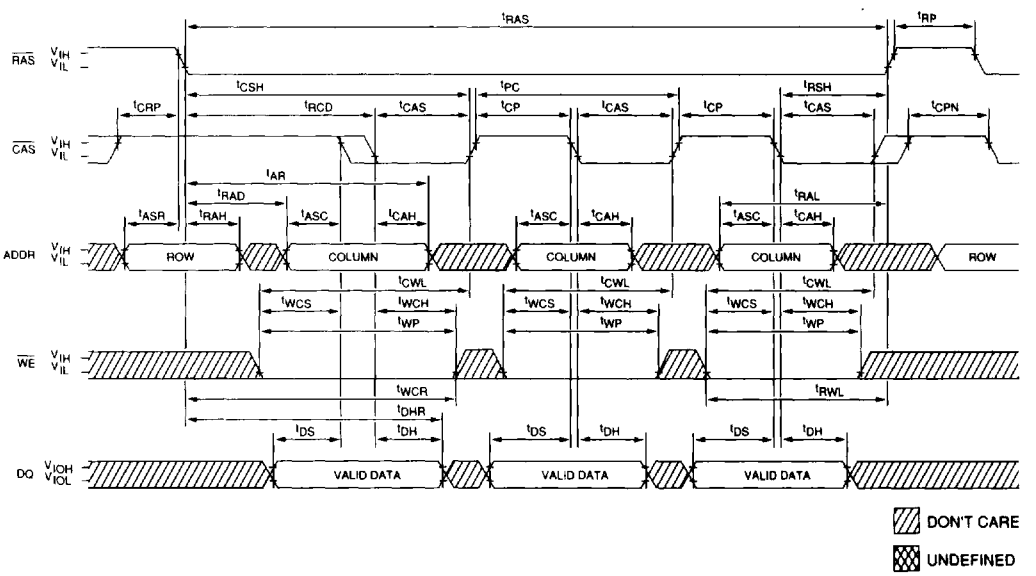
EARLY-WRITE CYCLE



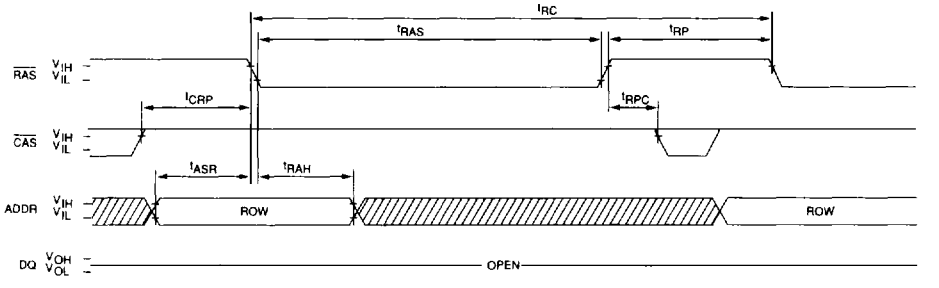
FAST-PAGE-MODE READ CYCLE



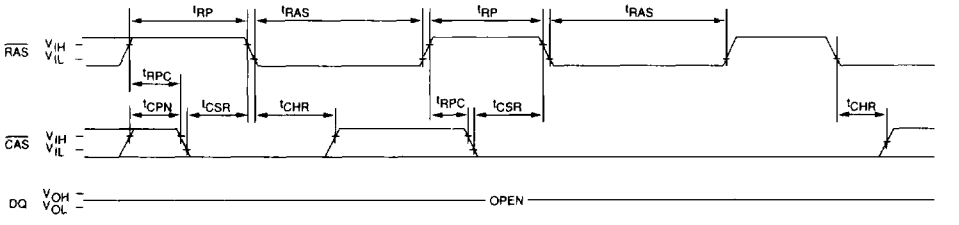
FAST-PAGE-MODE EARLY-WRITE CYCLE



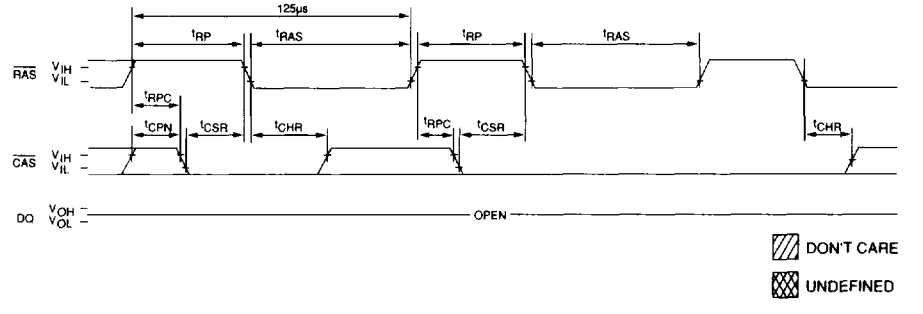
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8 and WE = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE [26]
(A0-A8 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
($\overline{WE}$ = HIGH)