Preliminary

GaN Hybrid Power Amplifier HM2060-10A

Product Features

- GaN on SiC HEMT
- In/Out Impedance Matching
- Small Size & Mass
- High Efficiency
- Low Cost
- Custom design available

Applications

- Radio System

Package Type : NP-1EL

Description

The HM2060-10A is designed for Radio system application frequencies from 2000 ~ 6000MHz.
This amplifier uses GaN HEMT technology which performs high breakdown voltage, high efficiency.
High In/Output impedance, high power density.

Electrical Specifications @ Vds =32V, Ta=25℃

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	2000	-	6000	ZS = ZL = 50 ohm
Power Gain	dB	-	16	-	Input Power = 24dBm
Power Gain Flatness		-	±2	-	
Input Return Loss		-	-3.5	-	Amp : Idq1 = 100mA Idq2 = 150mA
Pout @ Psat	dBm	39.5	40	-	
Drain Efficiency	%	-	25	-	
Ids	A	-	1.4	-	
Supply Voltage	V		-3.0	-2	Gate Bias (Vgs1 and Vgs2)
	V	-	32	-	Main Bias(Vds)

Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on : Turn on the Gate Voltage supply and last turn On the Drain voltage supplies

Turn off : Turn off the Drain Voltage and last turn off the Gate voltage

Note

HM Series have internal DC blocking capacitors at the RF input and output ports

Mechanical Specifications

PARAMETER	UNIT	TYP	REMARK
Mass	g	2	-
Dimension	㎜	20.5 x 15 x 3.5	-

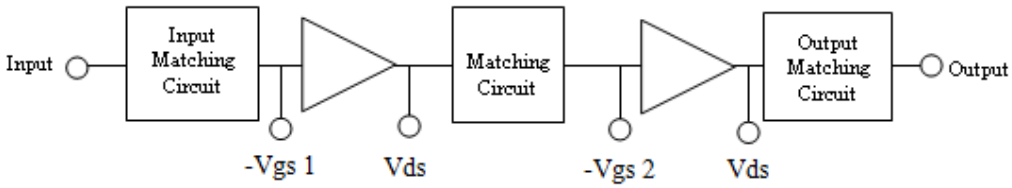
Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL
Gate-Source Voltage	V	-10 ~ 0	Vgs1 Vgs2
Drain-Source Voltage	V	84	Vds
Gate Current	mA	6.9	Ig
Operating Case Temperature	°C	-30 ~ 65	T_C
Storage Temperature	°C	-40 ~ 100	T_{STG}

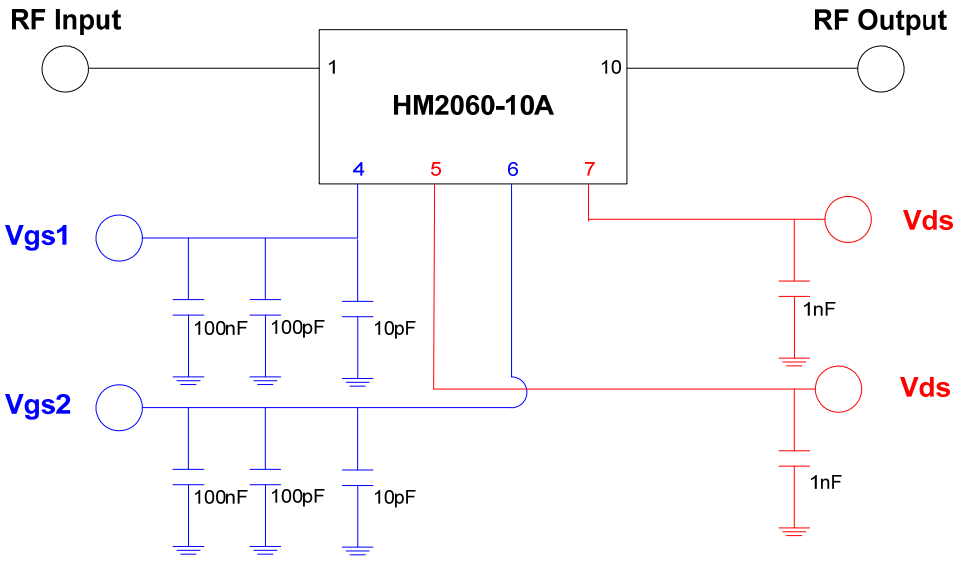
Operating Voltages

PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage	V	31.8	32	32.5	Vds
Gate Voltage (on-stage)	V	-	Vgs1@Idq1	-2	Vgs 1
Gate Voltage (on-stage)	V	-	Vgs2@Idq2	-2	Vgs 2
Gate Voltage (off-stage)	V	-	-8	-	Vgs 1
Gate Voltage (off-stage)	V	-	-8	-	Vgs 2

Block Diagram



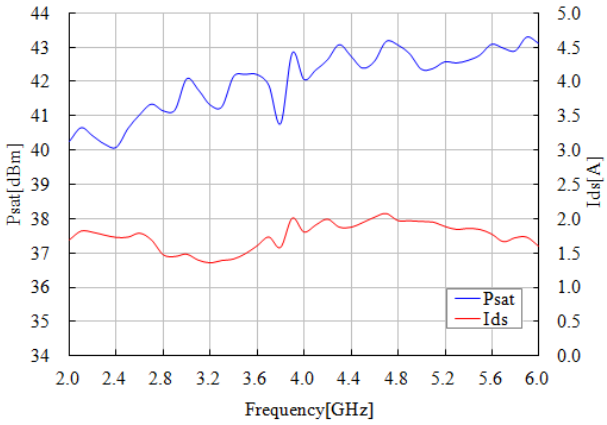
Application Circuit



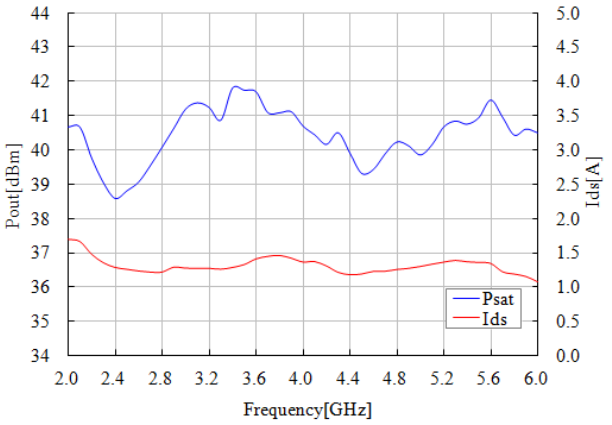
Performance Charts

* **Bias condition** @ Idq1 100mA, Idq2 150mA, Vds =+32V, Ta=25℃

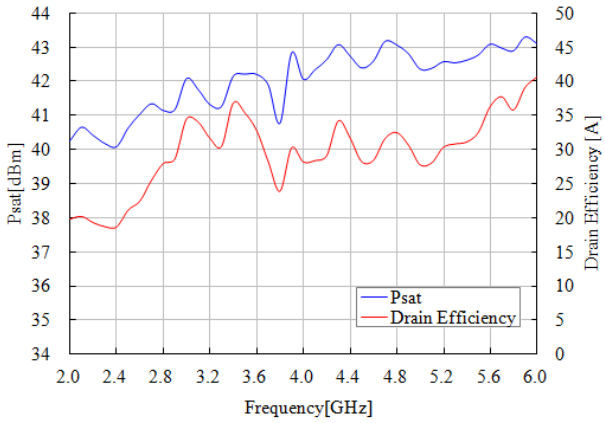
Saturation Power & Ids vs. Frequency



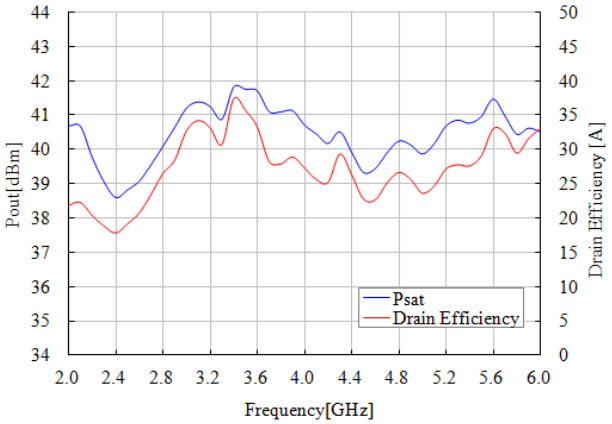
Output Power @ Pin= 24dBm & Ids vs. Frequency



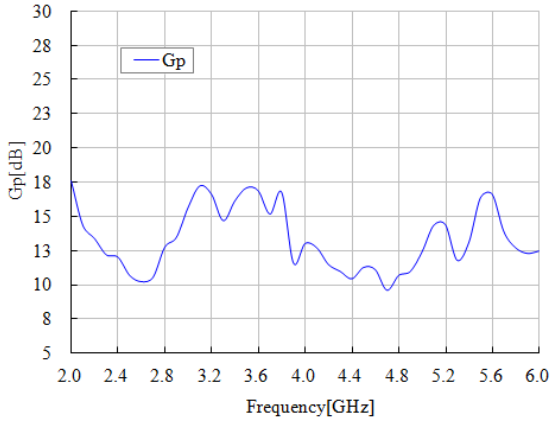
Saturation Power & Drain Efficiency vs. Frequency



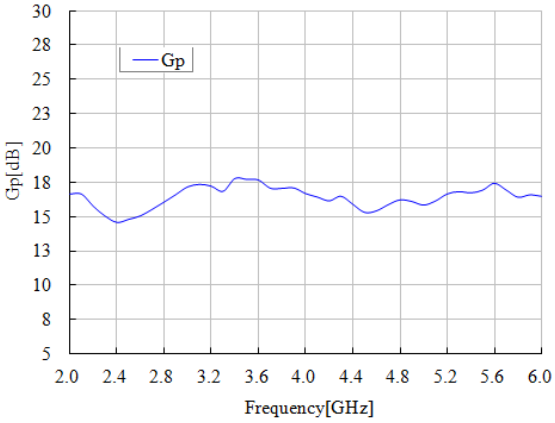
Output Power @ Pin= 24dBm & Drain Efficiency vs. Frequency



Power Gain @ Psat vs. Frequency

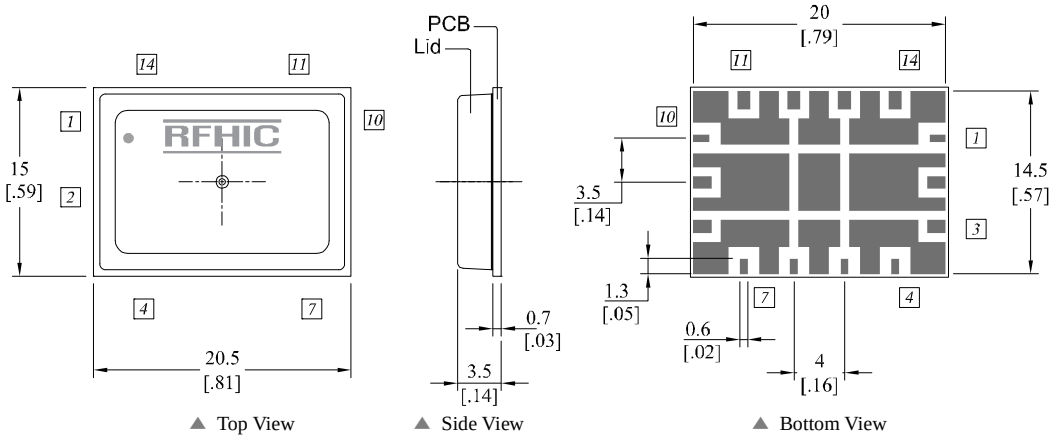


Power Gain @ Pin= 24dBm vs. Frequency



Package Dimensions (Type: NP-1EL)

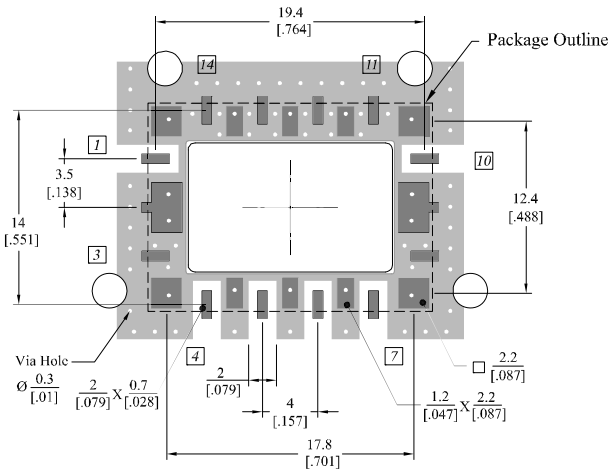
* Unit: mm[inch] | Tolerance: ±0.15[.006]



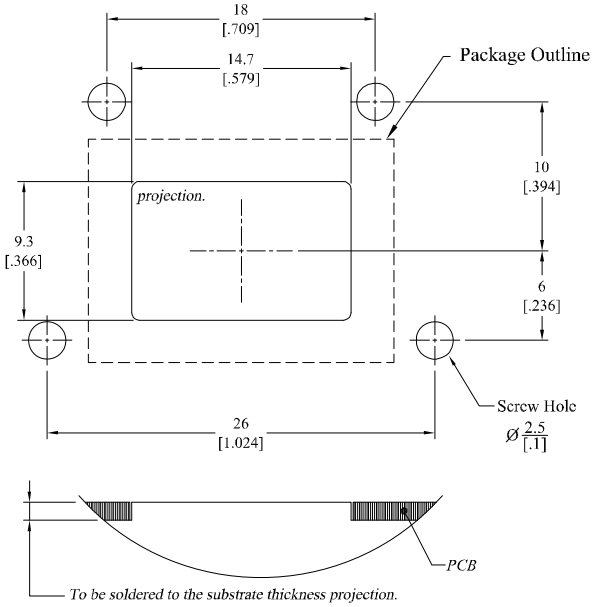
▲ Top View ▲ Side View ▲ Bottom View

Pin Description							
Pin No	**Function**	**Pin No**	**Function**	**Pin No**	**Function**	**Pin No**	**Function**
1	RF Input	4	Vgs1	8	GND	11	GND
2	GND	5	Vds	9	GND	12	GND
3	GND	6	Vgs2	10	RF Output	13	GND
-	-	7	Vds	-	-	14	GND

Recommended Pattern



Recommended Mounting Configuration



Precautions

This product is a Gallium Nitride Transistor.
The Gallium Nitride Transistor requires a Negative Voltage Bias which operates alongside a Positive Voltage Bias. These Biases are applied in accordance to the Sequence during Turn-On and Turn-Off.
The Pallet Amplifier does not have a built-in Bias Sequence Circuit. Therefore, users need to either apply positive voltages and negative voltages in the required sequence, or add an external Bias Circuit to this Amplifier.
The required sequence for power supply is as follows.

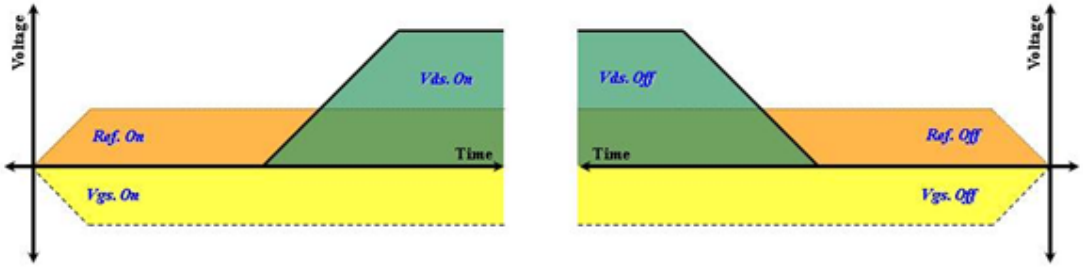
During Turn-On

1. Connect GND.
2. Apply Vgs1 and Vgs2.
3. Apply Vds.
4. Apply the RF Power.

During Turn-Off

1. Turn off RF power.
2. Turn off Vds, and then, turn off the Vgs1 and Vgs2.
3. Remove all connections.

Turn On **Turn Off**



- Sequence Timing Diagram -

Ordering Information

Part Number	Package Design
HM2060-10A	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

Revision History

Part Number	Release Date	Version	Modification	Data Sheet Status
HM2060-10A	2013.5.07	0.3	New data	Preliminary