Fixed Frequency Flyback Controller with Ultra-low No Load Power Consumption

The Future of Analog IC Technology

DESCRIPTION

HFC0400 i s a fixed-frequency current-mode controller with built-in slope compensation. It targets medium-power, off-line, flyb ack, switch-mode power supplie s. At light loads, th e controller freezes the peak current and reduces its switching frequency down to 25 kHz to offer excellent light-load efficiency.

At very ligh t loads, the controller enters burst mode to achieve very low standby power consumption.

HFC0400 offers frequency jittering to help dissipate energy generated by conducted noise.

HFC0400 also has an X -cap discharge function to discharg e the X -cap when the input is unplugged.

HFC0400 features multiple prote ctions that include ther mal shutdown (TSD), VCC under-voltage lockout (UVLO), overloa d protectio n (OLP), ove r-voltage protection (OVP), and brown-out protection.

HFC0400 is available in an SOIC8-7A package.

FEATURES

- Fixed-frequency current-mode control with built-in slope compensation
- Frequency foldback down to 25kHz at light loads
- Burst mode for low standby power consumption
- Frequency jitter to reduce EMI signature
- X-cap discharge function
- Internal high-voltage current source
- VCC under-voltage lockout with hysteresis (UVLO)
- Brown-out protection on HV pin
- Overload protection with programmable delay
- Thermal shutdown (auto-restart with hysteresis)
- Latch-off for external over-voltage protection (OVP) and over-temperature protection (OTP) on TIMER pin
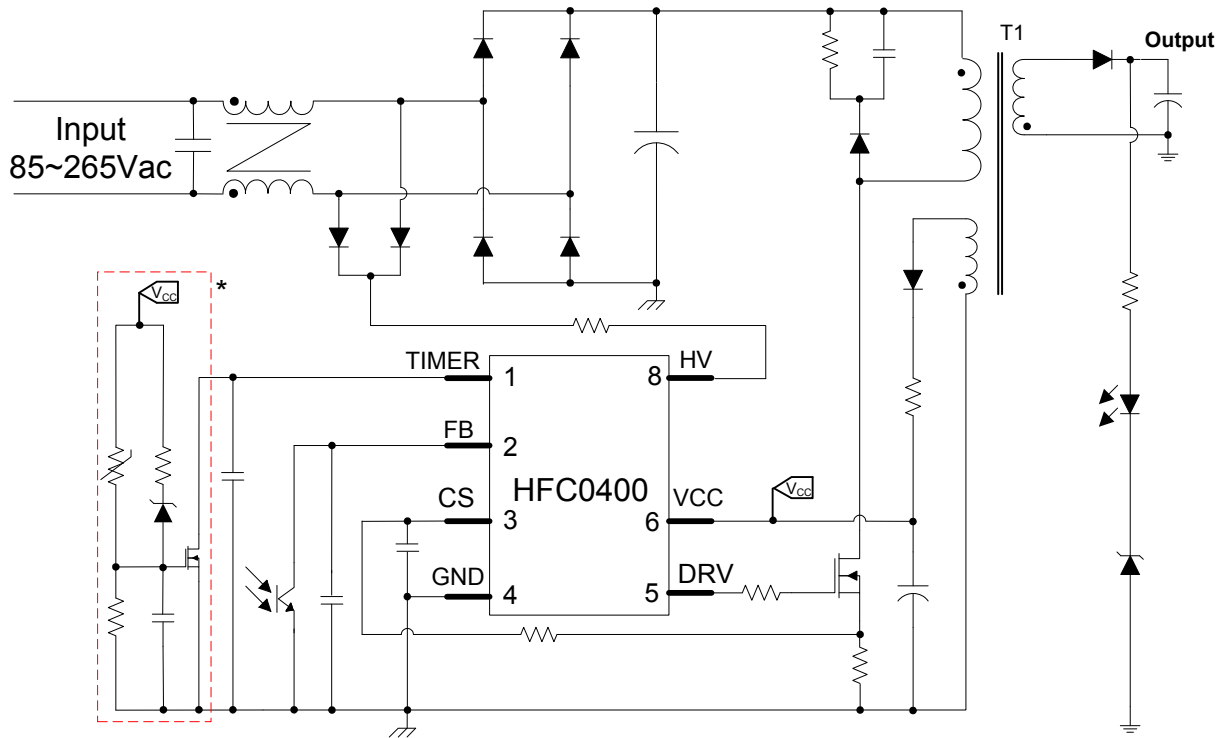- Short-circuit protection
- Programmable soft start

APPLICATIONS

- AC/DC adapters for notebook computers, tablets, and smartphones
- Offline battery chargers
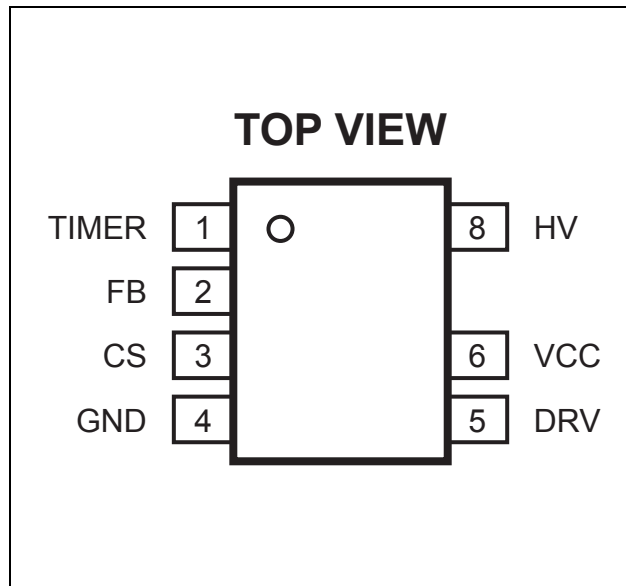- LCD TV s and monitors

TYPICAL APPLICATION

* The circuit in red is optional. Implements exte rnal OVP a nd OTP fun ction by pulling the TIMER pin down.

ORDERING INFORMATION

Part Number*	Package	Top Marking
HFC0400GS	SOIC8-7A	HFC0400

* For Tape & Reel, add suffix –Z (e.g. HFC0400GS–Z);

PACKAGE REFERENCE

TOP VIEW

TIMER	1	8 HV
FB	2	
CS	3	6 VCC
GND	4	5 DRV

ABSOLUTE MAXIMUM RATINGS [1]

HV Break Down Voltage .... -0.7V to 700V
V_{CC}, DRV to GND...........................-0.3V to 30V
FB, TIMER, CS to GND ....-0.3V to 7V
Continuous Power Dissipation (T_A = +25°C) [2]
.... 1.3W
Junction Temperature...............................150°C
Thermal Shutdown....................................150°C
Thermal Shutdown Hysteresis....................25°C
Lead Temperature ....260°C
Storage Temperature .... -60°C to +150°C
ESD Capability Human Body Model (All Pins
except HV) 4.0kV
ESD capability for Machine Mode.............. 200V

Recommended Operation Conditions [3]

Operating Junction Temp (T_J).. -40°C to +125°C
Operating V_{CC} range ....8V to 20V

Thermal Resistance [4] θ_{JA} θ_{JC}

SOIC8-7A ....96 ...... 45... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERICS

For typical value T_J=25°C, unless otherwise noted

Parameter Sy	mbol	Conditions	Min	Typ	Max	Unit
Start-up Current Source (HV)						
Supply Current from HV	I_{HV}	V_{CC}=6V;V_{HV}=400V	1.6	1.85	2.1	mA
Leakage Current from HV	I_{HV}	V_{CC}=10V;V_{HV}=400V	12	15	18	µA
Break-Down Voltage	V_{BR}		700			V
Supply Voltage Management (VCC)						
VCC Current-Source Turn-Off Level, Rising	VCC_{OFF}		12	14.5	17	V
VCC Threshold for HV Turn-On Detection, Falling	VCC_{SS}		9.5	11.5	13.5	V
VCC Hysteresis for HV Turn-On Detection	$VCC_{OFF} - VCC_{SS}$	1.5		3		V
VCC Current-Source Turn-On Level, Falling	VCC_{ON}		7.0	8.0	9.0	V
VCC UVLO Hysteresis	$VCC_{OFF} - VCC_{ON}$	5		6.5		V
VCC Re-charge Level When Protection Occurs	VCC_{PRO}		4.7	5.3	5.9	V
VCC Decreasing Level When Latch-Off Phase Ends	VCC_{LATCH}			2.5		V
Internal IC Consumption	I_{CC}	V_{FB}=2V;C_L=1nF, V_{CC}=12V	1	1.5	2	mA
Internal IC Consumption, Latch Off Phase	$I_{CCLATCH}$	V_{CC}=6V	520	585	650	µA
Voltage above V_{CC} Where the Controller Latches Off (OVP)	V_{OVP}		22	25	27	V
OVP Comparator Blanking Duration	τ_{OVP}			26		µs
Brown-out						
HV Turn-On Threshold	HV_{ON}	V_{HV} rising	95	108	120	V
HV Turn-Off Threshold	HV_{OFF}	V_{HV} falling	90	103	115	V
Brown-Out Hysteresis	ΔHV	4		5.2	6.4	V
Timer Duration for Line Cycle Drop-out	τ_{HV}	C_{TIMER}=47nF	50			ms
Oscillator						
Oscillator Frequency	f_{OSC}		60	65	69.5	kHz
Frequency Jitter Amplitude, in Percentage of f_{OSC}	A_{jitter}			±6.7		%
Frequency Jitter Modulation Period	τ_{jitter}	C_{TIMER}=47nF		3.7		ms
Current Sense						
Current Limit	V_{ILIM}		0.9	0.95	1	V
Short-Circuit Protection Level	V_{SCP}		1.3	1.45	1.55	V
Leading-Edge Blanking for V_{ILIM}	τ_{LEB1}			350		ns
Leading-Edge Blanking for V_{SCP}	τ_{LEB2}			270		ns
Slope of the Compensation Ramp	S_{RAMP}		20	25	30	mV/µs

ELECTRICAL CHARACTERICS *(continued)*
For typical value T_J=25°C, unless otherwise noted

Parameter Sy	mbol	Conditions	Min	Typ	Max	Unit
Feedback (FB)						
Internal Pull-Up Resistor	R_{FB}		12	13	14	kΩ
Internal Pull-Up Voltage	V_{DD}			4.3		V
V_{FB} to Internal Current Set-Point Division Ratio	K_{FB}			3.0		--
FB Level (Falling) at which the Controller Enters Burst Mode	V_{BURL}		0.29	0.32	0.35	V
FB Level (Rising) at which the Controller Exits Burst Mode	V_{BURH}		0.42	0.46	0.50	V
Over Load Protection						
FB Level at which the Controller Enters OLP after Blanking Time	V_{OLP}			3.7		V
Time Duration When FB Reaches Protection Point, Before OLP	τ_{OLP} C	$_{TIMER}$=47nF 50				ms
Frequency Foldback						
Frequency Foldback FB Voltage Threshold, Upper Limit	$V_{FB(FOLD)}$			1.8		V
Minimum Switching Frequency	$f_{OSC(min)}$		21	25	30	kHz
Frequency Foldback FB Voltage Threshold, Lower Limit	$V_{FB(FOLDE)}$			1.0		V
Latch-Off Input (Integration in TIMER)						
The Threshold below which Controller is Latched	$V_{TIMER(LATCH)}$		0.9	1	1.1	V
Blanking Duration on Latch Detection	τ_{LATCH}			12		µs
DRV Voltage						
Driver Voltage High Level	V_{High}	C_L=1nF V_{CC}=8.4V		6.7		V
		C_L=1nF V_{CC}=12V		10.3		V
Driver Voltage-Clamp Level	V_{Clamp}	C_L=1nF, V_{CC}=24V		13.4		V
Driver Voltage, Low Level	V_{Low} C	$_L$=1nF, V_{CC}=24V		16		mV
Driver Voltage, Rise Time	τ_R C	$_L$=1nF, V_{CC}=16V		13		ns
Driver Voltage, Fall Time	τ_F	C_L=1nF, V_{CC}=16V		23		ns
Driver Pull-Up Resistance	$R_{Pull-up}$	C_L=1nF, V_{CC}=16V		8		Ω
Driver Pull-Down Resistance	$R_{Pull-down}$ C	$_L$=1nF, V_{CC}=16V		20		Ω

PIN FUNCTIONS

Pin #	Name	Description
1 TIMER		Timer. This pin combines the soft start, frequency jittering, and timer functions for OLP, brown-out protection, and X-cap discharge. Latch the IC by pulling this pin down.
2	FB	Feedback. Use a pull-down optocoupler to control output regulation.
3	CS	Current Sense. Senses the primary current for current-mode operation.
4 GND		IC Ground.
5	DRV	Drive Signal Output.
6 VCC		Power Supply.
8	HV	High-Voltage Current Source. Includes brown-out and X-cap discharge functions.

TYPICAL CHARACTERISTICS

Supply Current from HV vs. Temperature

V_{CC}=6V;V_{HV}=400V
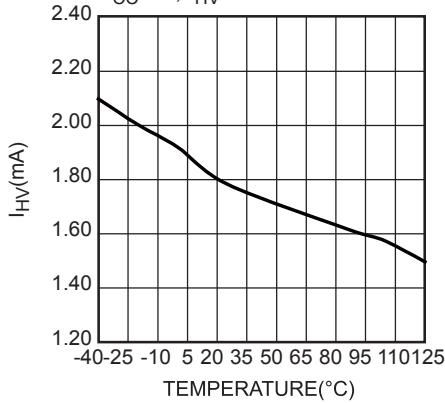
Leakage Current from HV vs. Temperature

V_{CC}=10V;V_{HV}=400V
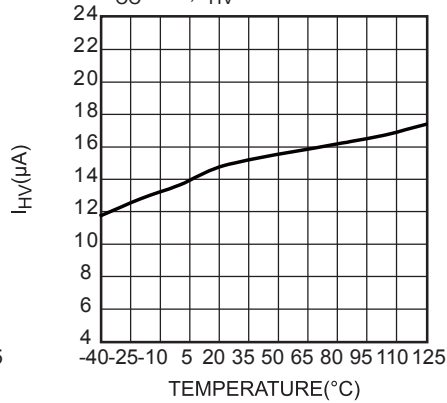
Internal IC Consumption vs. Temperature

VFB=2V, CL=1nF, VCC=12V
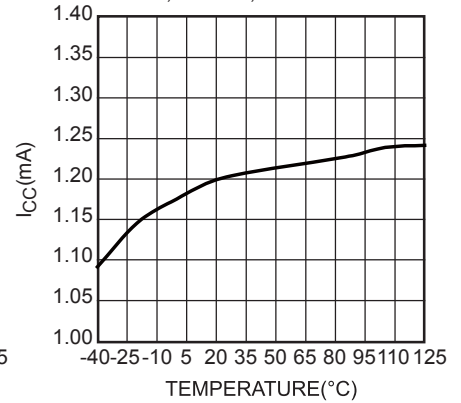
Break-Down Voltage vs. Temperature
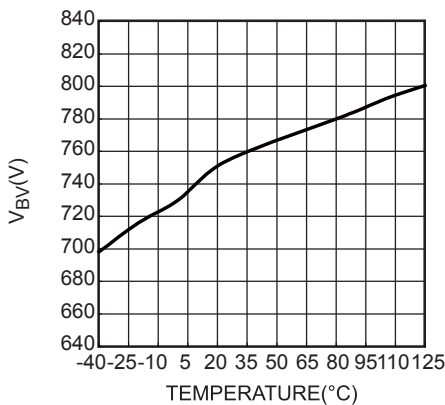
VCC Current-Source Turn-Off Level, Rising vs. Temperature
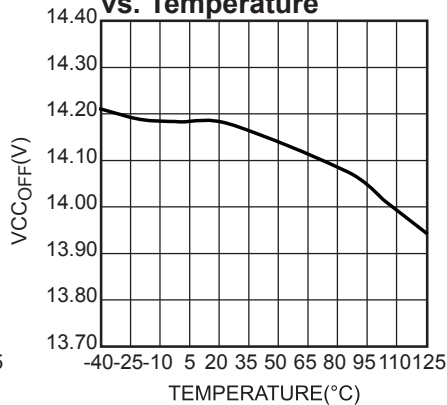
VCC Threshold for HV Turn-On Detection, Falling vs. Temperature
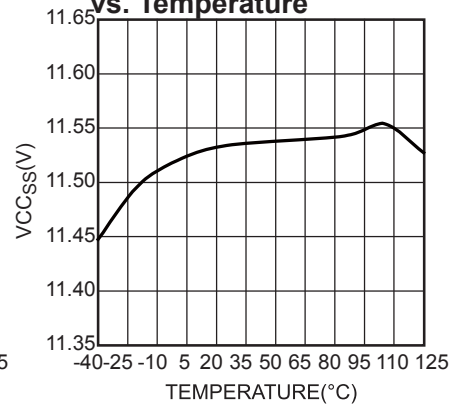
VCC Current-Source Turn-On Level, Falling vs. Temperature
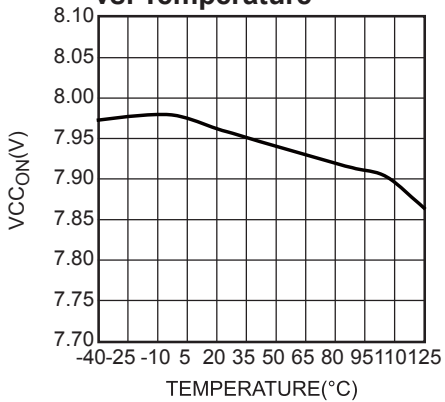
Voltage above VCC Where the Controller Latches Off (OVP) vs. Temperature
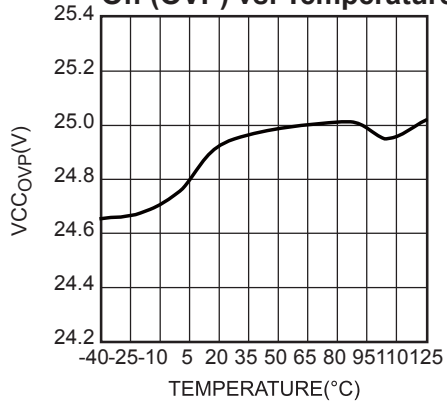
VCC Hysteresis for HV Turn-On Detection vs. Temperature
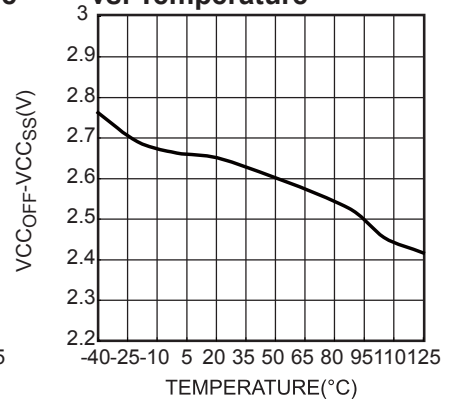
TYPICAL CHARACTERISTICS *(continued)*

VCC Re-charge Level when Protection Occurs vs. Temperature
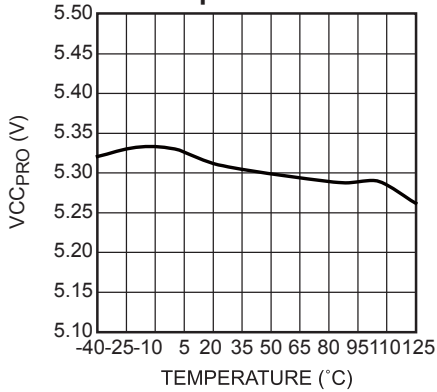
VCC Decreasing Level When Latch-off Phase Ends vs. Temperature
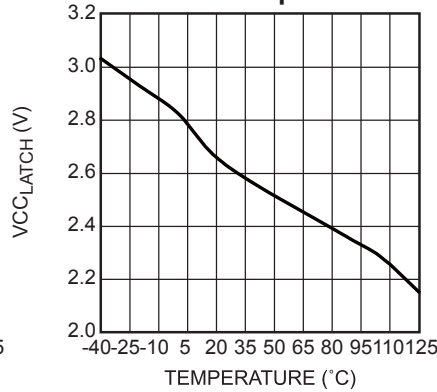
HV Turn-on Threshold vs. Temperature
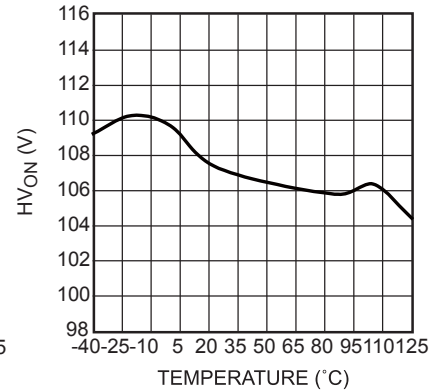
HV Turn-off Threshold vs. Temperature
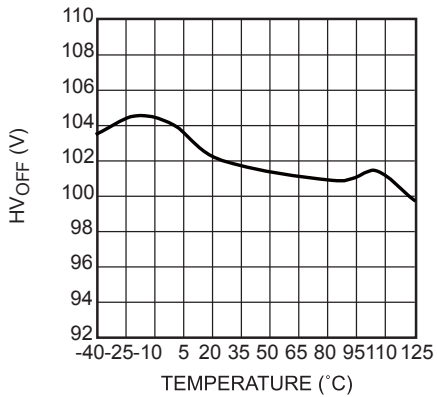
Oscillator Frequency vs. Temperature
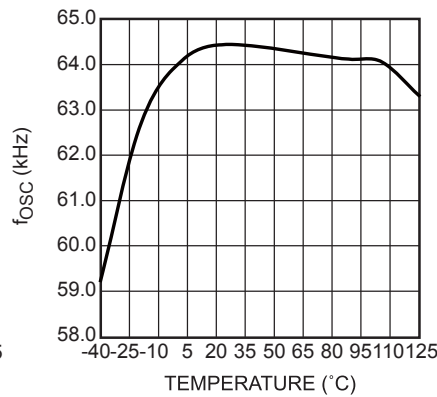
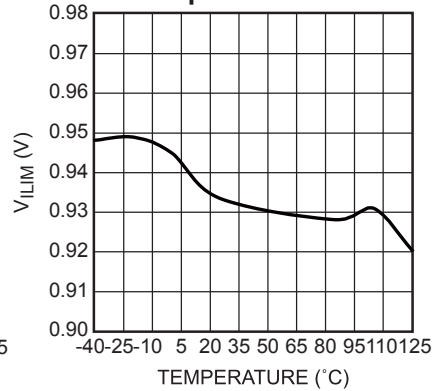**Frequency Jitter Amplitude, in Percentage of f$_{OSC}$ vs. Temperature**
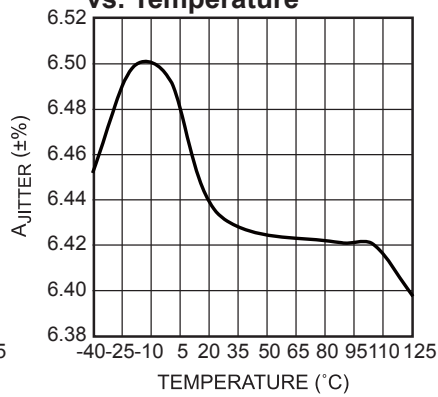
Minimum Switching Frequency vs. Temperature
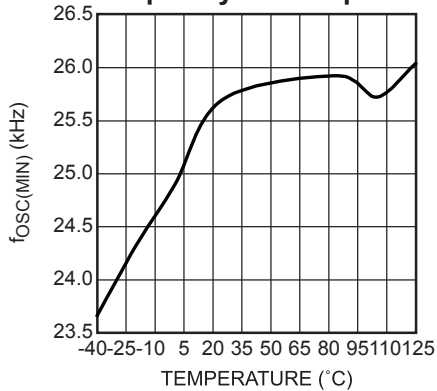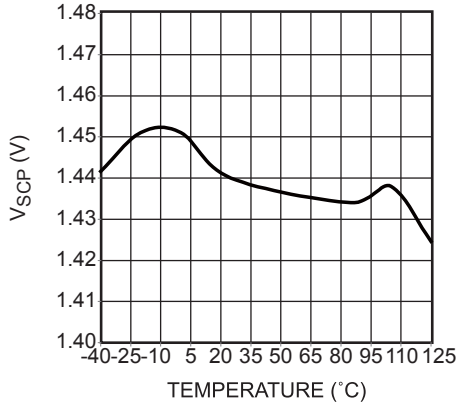
Slope of the Compensation Ramp vs. Temperature
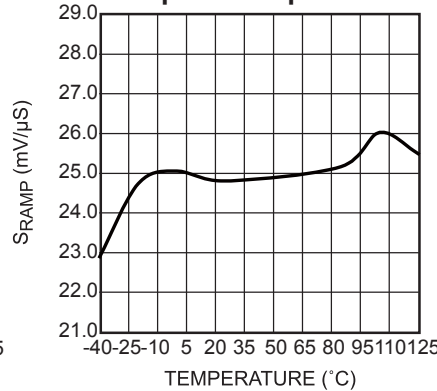
Current Limit vs. Temperature

8

TYPICAL CHARACTERISTICS *(continued)*

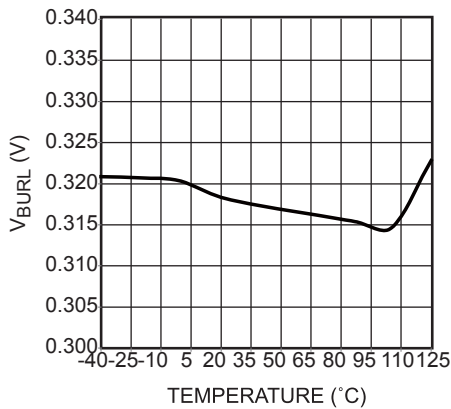**Short-Circuit Protection Level vs. Temperature**

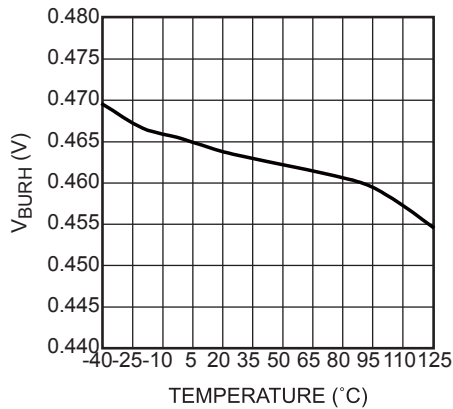**Leading-Edge Blanking for VILIM vs. Temperature**
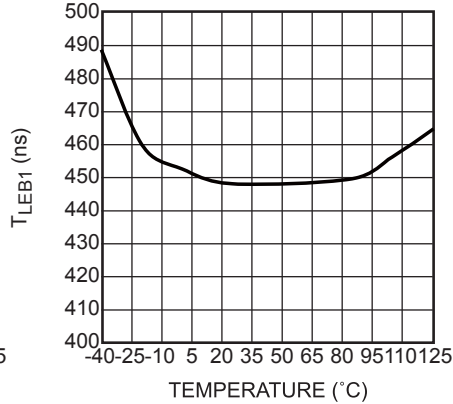
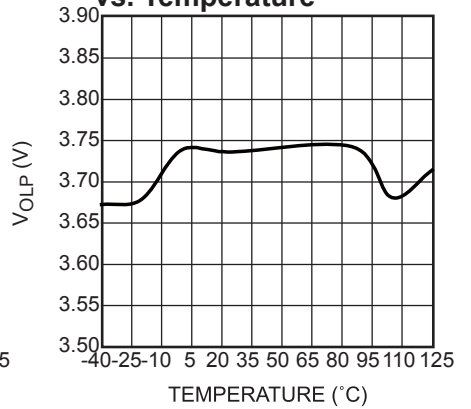**Leading Edge Blanking for VSCP vs. Temperature**
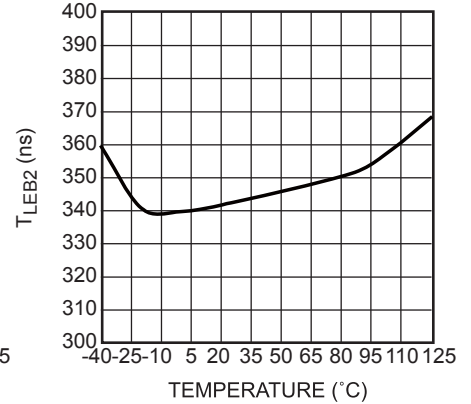
FB Level (Falling) at which the Controller Enters Burst Mode vs. Temperature
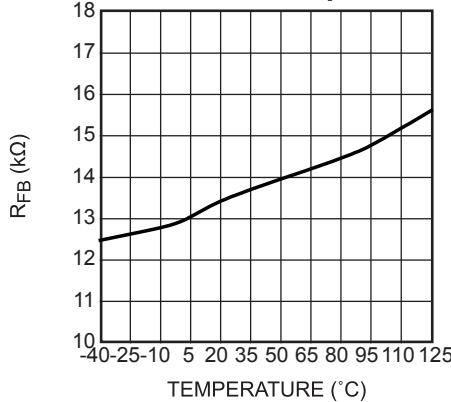

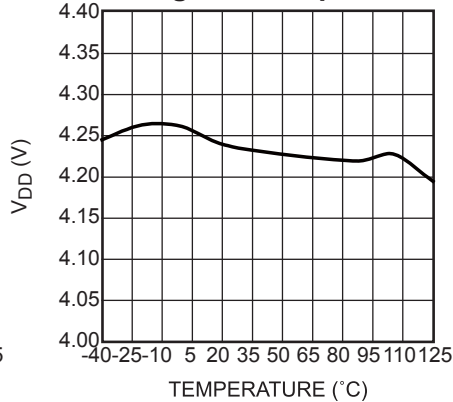**FB Level (Rising) at which the Controller Exits Burst Mode vs. Temperature**

FB Level at which the Controller Enters OLP after Blanking Time vs. Temperature

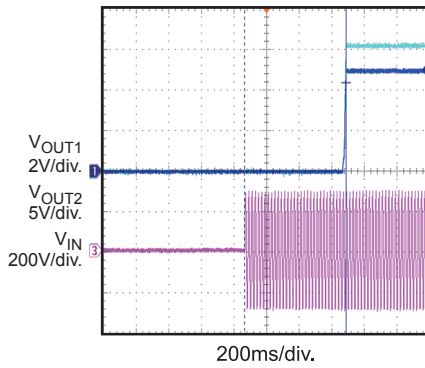**FB Internal Pull-up Resistor vs. Temperature**
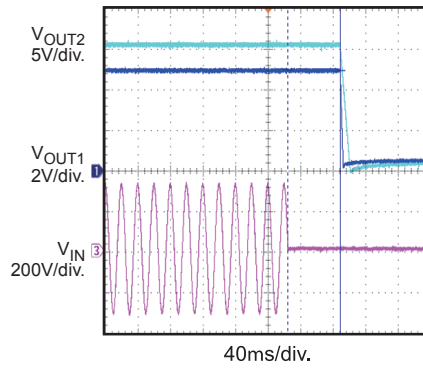

FB Internal Pull-up Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISIC

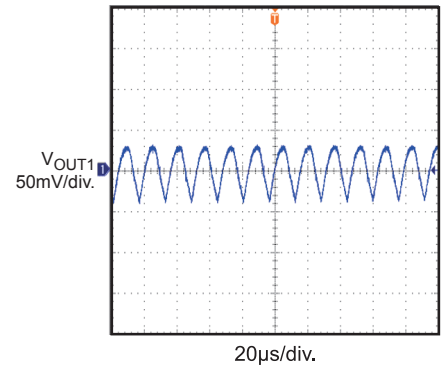V_{IN}=230VAC, V_{OUT1}=5V, I_{OUT1}=3A, V_{OUT2}=16V, I_{OUT2}=1.5A, T_A=25°C, unless otherwise noted.

Input Power Start Up

200ms/div.

Inut Power Shut Down
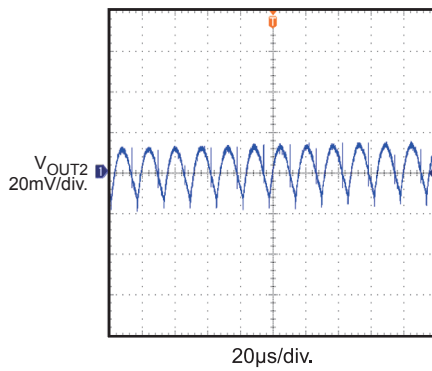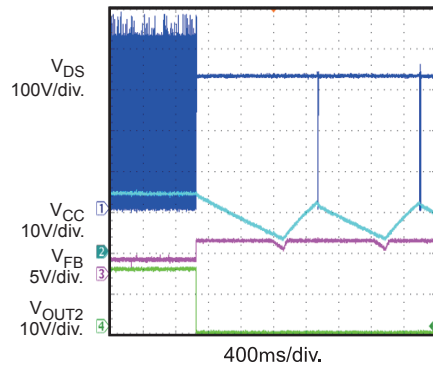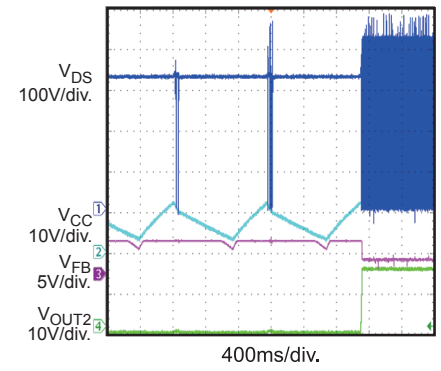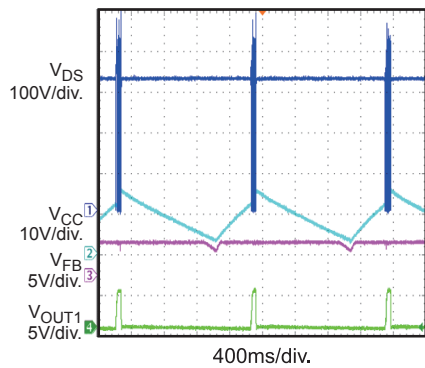
40ms/div.

Output1 Ripple

20µs/div.

Output2 Ripple

20µs/div.

SCP Entry

400ms/div.

SCP Recovery

400ms/div.

OLP, 5V Over Load

400ms/div.

OLP, 16V Over Load

400ms/div.

OVP

No Load

20ms/div.
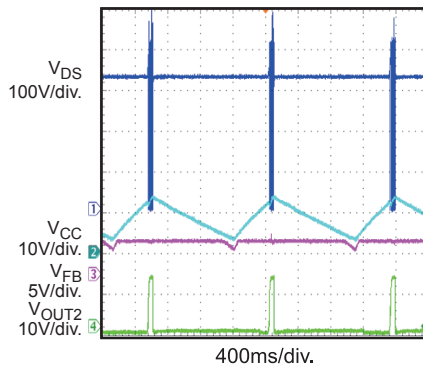
TYPICAL PERFORMANCE CHARACTERISIC *(continued)*

V_{IN}=230VAC, V_{OUT1}=5V, I_{OUT1}=3A, V_{OUT2}=16V, I_{OUT2}=1.5A, T_A=25°C, unless otherwise noted.

OVP

Full Load
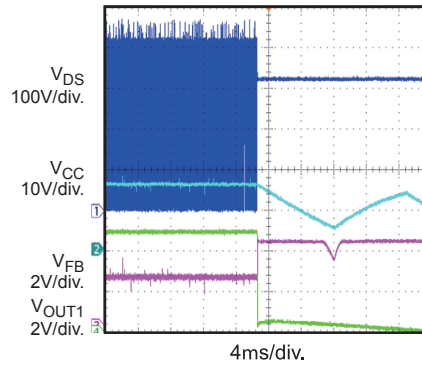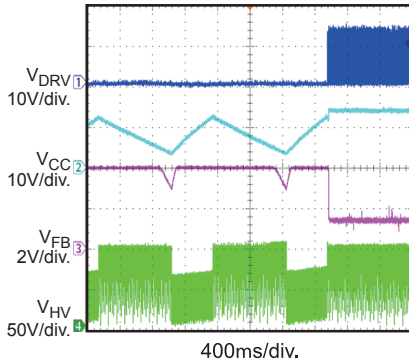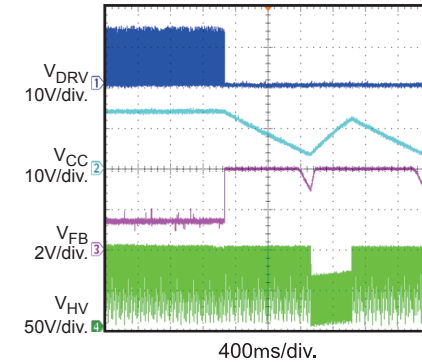
V_{OUT1}
5V/div.

V_{OUT2}
10V/div.

V_{CC}
10V/div.

20ms/div.

OTP Entry

V_{DS}
100V/div.

V_{CC}
10V/div.

V_{FB}
2V/div.

V_{OUT1}
2V/div.

4ms/div.

OTP Recovery

V_{DS}
100V/div.

V_{CC}
10V/div.

V_{FB}
2V/div.

V_{OUT1}
2V/div.

400ms/div.

Brown-in

V_{IN}=75VAC

V_{DRV}
10V/div.

V_{CC}
10V/div.

V_{FB}
2V/div.

V_{HV}
50V/div.

400ms/div.

Brown-out

V_{IN}=72VAC

V_{DRV}
10V/div.

V_{CC}
10V/div.

V_{FB}
2V/div.

V_{HV}
50V/div.

400ms/div.

X-cap Discharge

V_{IN}=265VAC, CX=0.22μF, No Load

V_{X-CAP}
100V/div.

100ms/div.

X-cap Discharge,

VIN=265VAC, CX=0.22μF, Full Load

V_{X-CAP}
100V/div.

100ms/div.

Conducted EMI

L-Wire

120
110
100
90
80
70
60 — EN55022Q
50 — EN55022A
40
30
20
10
0

150kHz   1MHz   10MHz   30MHz

Conducted EMI

N-Wire

120
110
100
90
80
70
60 — EN55022Q
50 — EN55022A
40
30
20
10
0

150kHz   1MHz   10MHz   30MHz

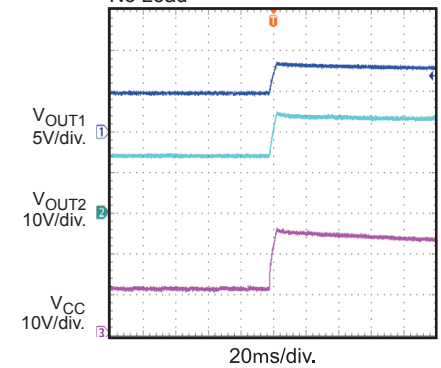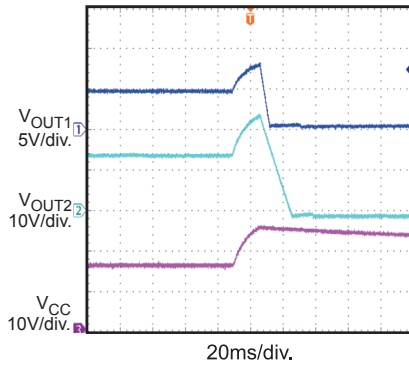## TYPICAL PERFORMANCE CHARACTERISIC *(continued)*

V_{IN}=230VAC, V_{OUT1}=5V, I_{OUT1}=3A, V_{OUT2}=16V, I_{OUT2}=1.5A, T_A=25°C, unless otherwise noted.
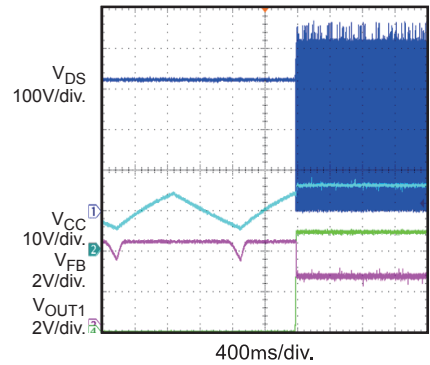
Efficiency
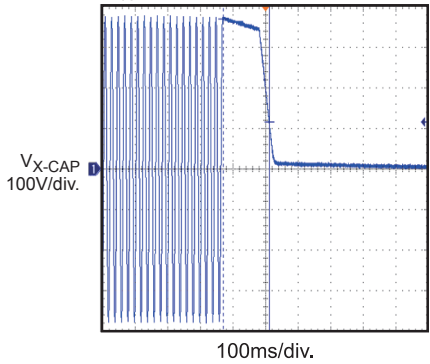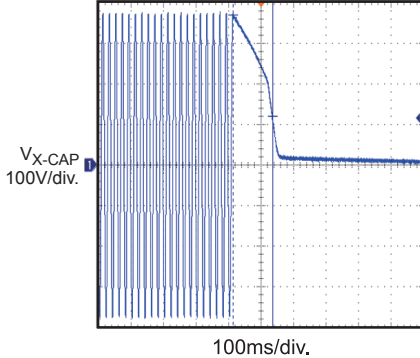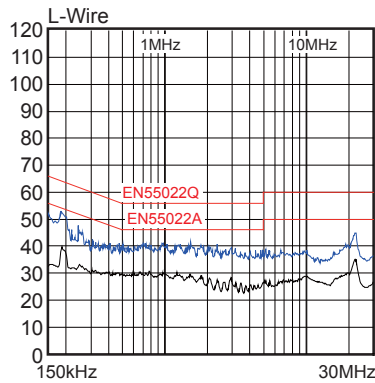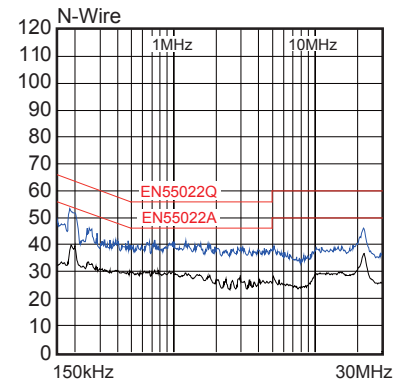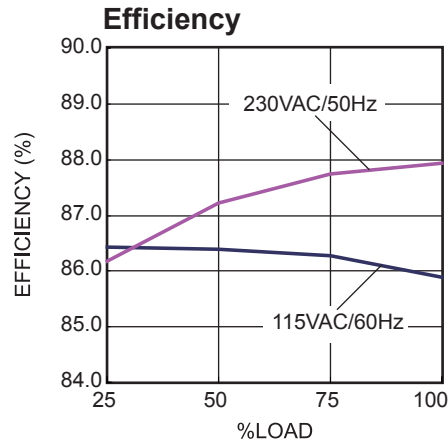
No Load Power Consumption

V_{IN} (VAC/Hz)		85/60	115/60	230/50	265/50
P_{IN} (mW)	5V/0A, 16V/0A	26.35	27.59	32.40	35.26
	5V/6mA, 16V/0A	71.92	72.72	80.70	84. 83

OPERATION

HFC0400 incorporates all the necessary features to build a reliable switch-mode power supply. It is a fixed-frequency current-mode controller with built-in slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. It also has excellent EMI performance thanks to frequency jittering.

Its high level of integration requires very few external components.

Figure 1: Functional Block Diagram

Fixed-Frequency with Jitter

Frequency jitter reduce s EMI b y dissipating th e energy. Figure 2 show s the circuit of frequen cy jittering.

Figure 2: Frequency Jitter Circuit

A controlled current s ourced (fixed at 2.72µA when V $_{FB}$=2V) chargers the internal 14pF capacitor. Comparing t he capacitor voltage to the TIMER voltage estimates the switching frequency as per equation (1). V $_{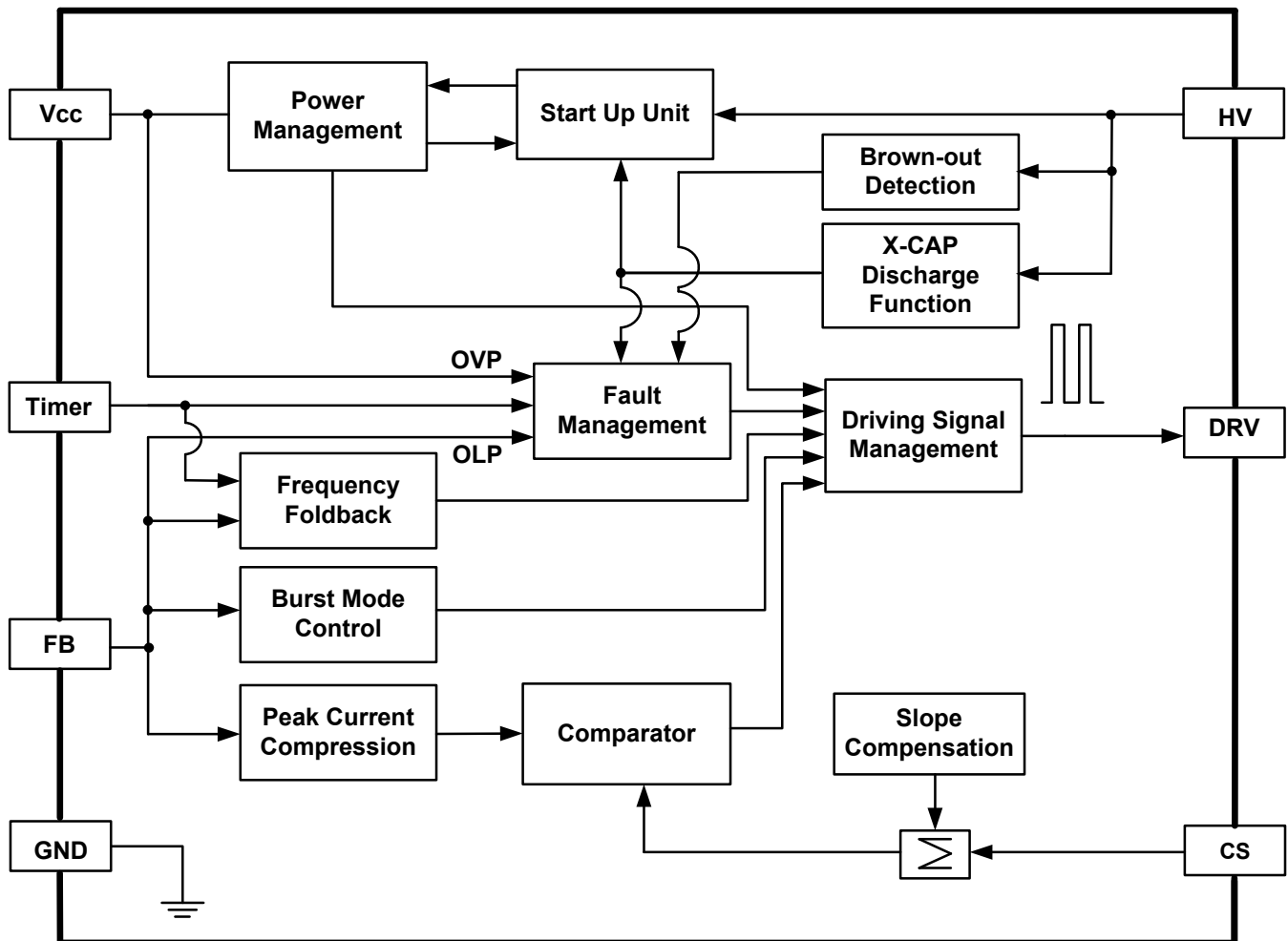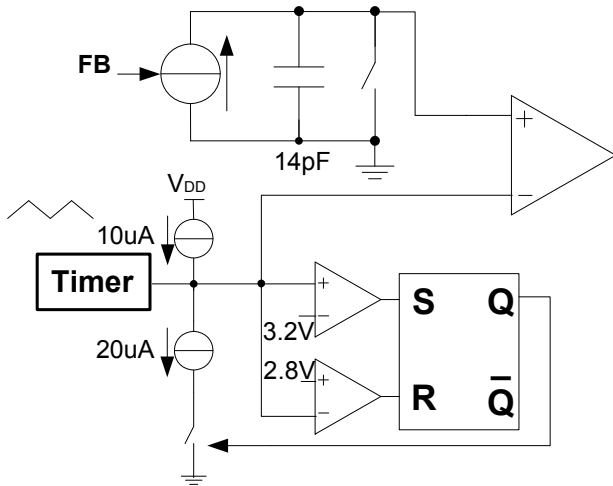TIMER}$ is a triangular wave that ranges between 2. 8V and 3.2V with a charging/ discharging current of 10 µA. Figure 3 shows shows the frequency jitter, τ_{jitter}, as per equation (2).

$$f_s = \frac{1}{14pF \cdot V_{TIMER}/2.72\mu A + 0.2\mu s} \quad (1)$$

$$\tau_{\overline{jitter}} \quad 2 \cdot \frac{C_{TIMER} \cdot (3.2V - 2.8V)}{10\mu A} \quad (2)$$
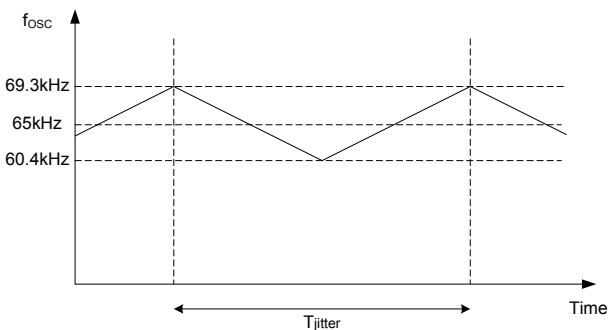

Figure 3: Frequency Jitter

Frequency Foldback

The HFC0400 implements frequen cy foldback at light load condition to improve overall efficiency.

When the load de creases to a given le vel (1.33V<V$_{FB}$<2V), the controller freezes the peak current (as measured as the voltage on the CS pin, 0.67V) and reduces its switching frequency down to 25kHz which helps to reduce the switching loss. If the load continues to decrease, the peak current decreases at a 25kHz fixed frequency to avoid audible noise. Figure 4 shows the frequency vs.V$_{FB}$ and peak current (V$_{CS}$) vs. V$_{FB}$.
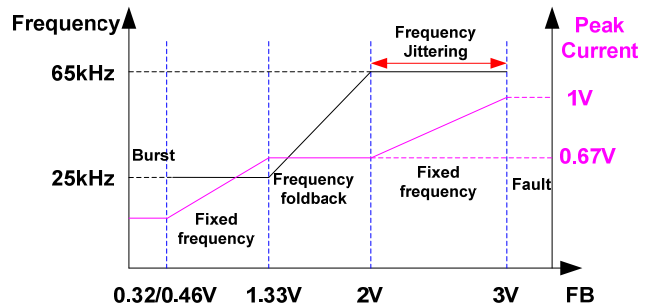
Figure 4: Frequency and Peak Current (V$_{CS}$) vs V$_{FB}$

Current-Mode Operation with Slope Compensation

V$_{FB}$ controls the primary-peak curre nt. When th e peak current reaches the level determined by V$_{FB}$, DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wid e input voltage range because its internal synchronous slope compensation (30mV/µs) avoids sub-harmonic oscillations w hen the duty cycle exceeds 50%.

High Voltage Startup Current Source with Brown-Out Detection

Initially, the internal hig h-voltage current source drawn from the HV pin supplies th e IC. The I C turns off th e current source as soon as V $_{CC}$ reaches 14. 5V and detects the voltage on HV. Once the HV voltage e xceeds HV$_{ON}$ before V $_{CC}$ drops down to 11.5V, the controller sta rts switching. Otherwise the system treats th e condition a s a brown-out to to lock the driver

output, causing V_{CC} to drop down to 5.3V and the high-voltage current sou rce turns on to recharge V_{CC}. The a uxiliary tran sformer win ding supplie s the IC after the controlle r starts switching. If V $_{CC}$ falls below 8.0V, the switching pu lse stop s an d the current source tu rns on ag ain. Figure 5 shows the typical V $_{CC}$ under-vol tage locko ut waveform.

Figure 5: V_{CC} Under-Voltage Lockout

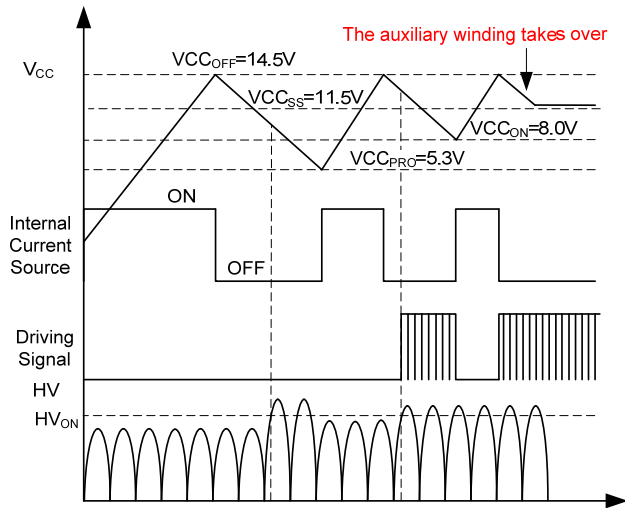The V_{CC} lower threshold UVLO drop s from 8V t o 5.3V under fault conditions, such a s OLP, SCP, brown-out, OVP, and OTP.

Soft Start

The peak current (co ntrolled by the TIMER voltage) gradually increases from 0.25V to 1V, as does the switching fre quency, to reduce th e stress on p ower components and to smoothly establish t he output voltage as the TIMER voltage incr eases from 1V to 1.75V during start -up. Figure 6 shows the typical soft-star t waveform. The TIMER capacitor d etermines the start-up duration as per equation (3).

$$\tau_{\overline{Soft-start}} \quad \frac{C_{TIMER} \cdot (1.75V - 1V)}{10/4\mu A} \qquad (3)$$
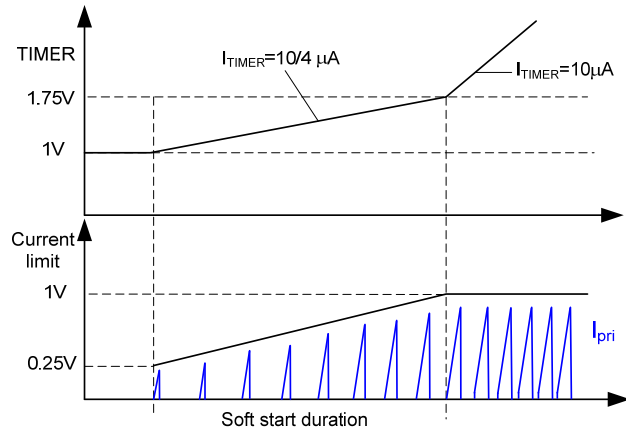
Figure 6: Soft-Start

Burst Mode

The HFC0400 enters burst-mode operation to minimize p ower dissip ation at no load or light load. As the load decreases, V $_{FB}$ decreases. The IC stops the switching cycle when V $_{FB}$ drop s below the lower threshold, V $_{BRUL}$−0.32V. The output voltage starts to drop, which causes V_{FB} to increase ag ain. Once V $_{FB}$ exceeds V$_{BRUH}$−0.46V, switching r esumes. V $_{FB}$ then rises and f alls repeatedly. Burst mode alternately enables an d disables MOSFET switching, thereby reducing no load or light load switching losses.

Timer-Based Over-Load Protection

In a flyback convert er, a fixed switchin g frequency results in a peak-current-limit ed maximum output power. When the outp ut demand exceeds the power limit, the output voltage drops below t he set value. Then th e current flowing through primary an d secondar y optocoupler falls and V$_{FB}$ is pulled high. T he HFC0400 implements a timer-based OLP blo ck as per Figure 7.

Figure 7: Overload Protection Block

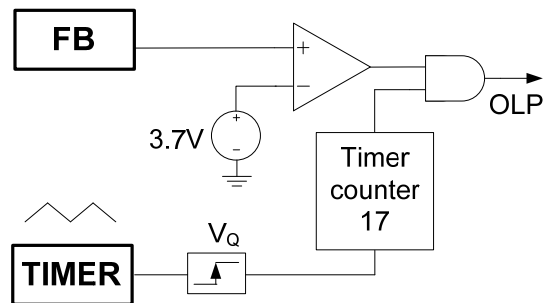When FB exceeds 3.7V (considered an error), the timer starts to count the V_Q rising edge. Removing the error flag resets the timer. If the timer reaches its completion (a count of 17), OLP triggers. This timer duration avoids triggering OLP during the power supply start-up or a load transition phase. Figure 8 shows OLP.
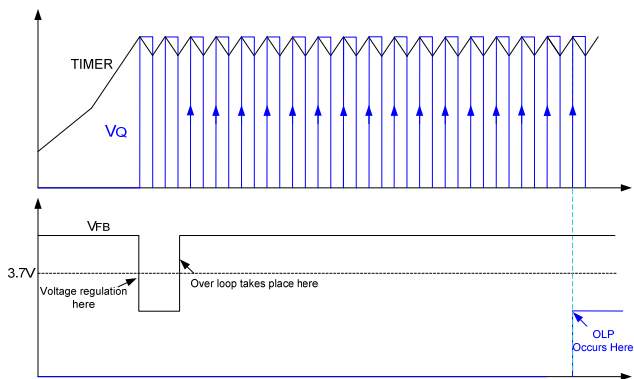

Figure 8: Overload Protection

Timer-Based Brown-Out Protection

The brown-out protection block is similar to the OLP block. When the HV voltage drops below HV_{OFF} (which is an error), the timer starts to count the V_Q rising edges. Once the HV voltage exceeds HV_{OFF}, the timer resets. When the timer has counted to 17, brown-out protection triggers and the switching pulse stops.

Short-Circuit Protection (SCP)

The HFC0400 has short-circuit protection that senses the CS voltage and stops switching if V_{CS} reaches 1.5V after a reduced leading-edge blanking (LEB) time. As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown (TSD)

To prevent from any lethal thermal damage, HFC0400 shuts down switching when the inner temperature exceeds 150°C. As soon as the inner temperature drops below 125 °C, the power supply resumes operation. During TSD, the V_{CC} UVLO lower threshold drops from 8.0V to 5.3V.

V_{CC} Over-Voltage Protection (OVP)

The HFC0400 enters latched fault condition if V_{CC} goes above 25V for 25 µs. The controller stays fully latched until V_{CC} drops below 2.5V, e.g. when the user power-cycles the main input.

TIMER Latch-Off for OVP and OTP

Pulling TIMER down below 1.0V for 12µs latches the HFC0400 off for external OVP and OTP etc.

X-Cap Discharge Function

X-caps typically filters the differential-mode EMI noise from a power supply's input. These components pose a potential hazard because they can store unsafe levels of high-voltage energy for long after the AC line is disconnected. Resistors in parallel to the X-cap provide a discharge path to meet safety standards, but constantly dissipate power while the AC is connected, and contribute to no-load and standby input power consumption.
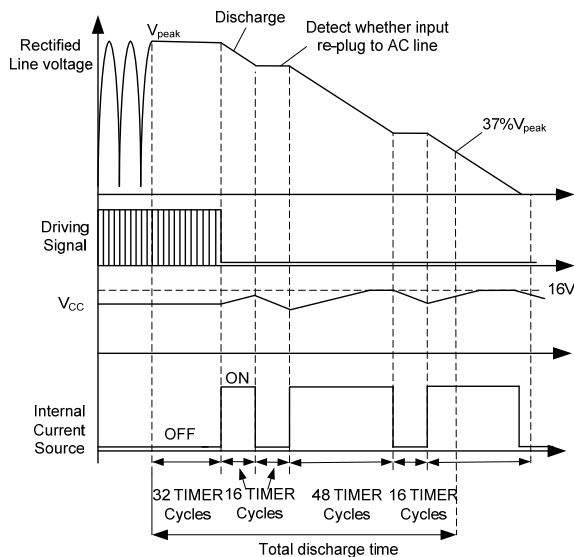

Figure 9: X-Cap Discharger

The HFC0400's HV acts as a smart X-cap discharger. In the presence of an AC voltage, the internal high-voltage current source turns off to block HV current flow and the IC monitors the HV voltage. Upon removing the AC voltage, the IC turns on the high-voltage current source after about 32 TIMER cycles to discharge the X-cap. The first discharge duration is 16 cycles, then the IC turns off the current source for 16 cycles to detect the presence of the AC line. If the AC input remains disconnected, the IC turns on the current source for 48 cycles, then off for 16 cycles repeatedly until the voltage on X-cap drops to V_{CC}. Upon detecting an AC input, the high-voltage current source remains off until V_{CC}

drops to VCC_{PRO} (5.3V) before recharging V_{CC} to restart the system. Figure 9 shows t he discharge function waveforms.

This approach provides a discharg e path for t he X-cap, eliminating discharge resistors and reduce power loss.

Clamped Driver

The DRV voltage is safely clamped at 13.4V when V_{CC} exceeds 16V, allowing the use o f any standard MOSFET.

Leading-Edge Blanking

An internal leading-ed ge blankin g (LEB) unit containing two LEB times is employed between the CS pin and the current comparator input to avoid premature switch ing pulse te rmination due to the parasitic capacitances. During the blanking time, the current comparator is disa bled and ca n not turn off the external MOSFET . Figure 10 shows the LEB waveform.
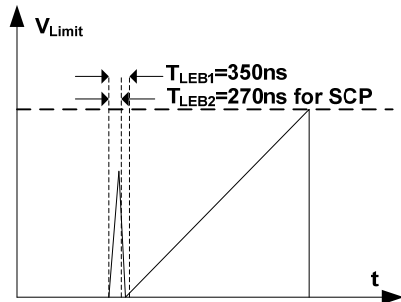

Figure 10: Leading-Edge Blanking

APPLICATION INFORMATION
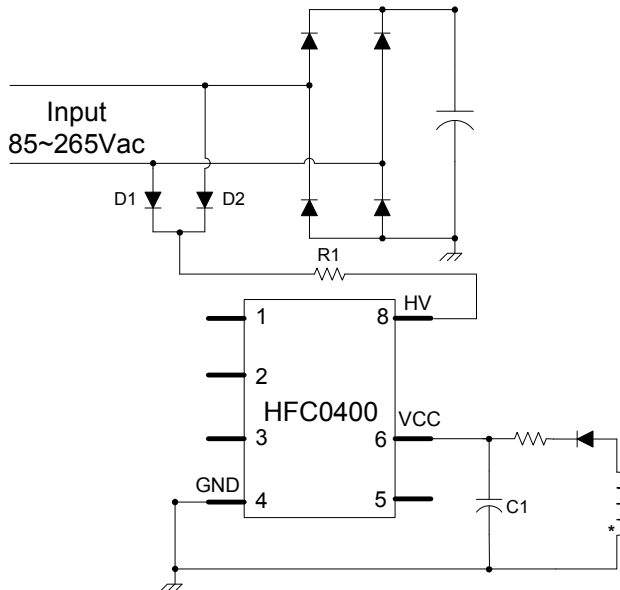
VCC Capacitor Selection

Figure 11: Start-Up Circuit

Figure 11 shows the start-up circuit. The value s of R1 and C1 deter mine the system start-up delay time: a larger R1 or C1 increa ses the start-up delay. The V_{CC} duration (from $V_{CC,OFF}$ to $V_{CC,SS}$) for brown-out detectio n should exceed half the input period, equation (4) provides an estimated value for th e V_{CC} capacitor, where $I_{CC(noswitch)}$ is the internal consumption (close t o $I_{CClatch}$), a nd τ_{input} is pe riod of th e AC input. For most applications, chose a V_{CC} capacit or value th at exceeds 10µF.

$$C_{VCC} > \frac{I_{CC(noswitch)} \cdot 0.5 \ \tau_{input}}{VCC_{OFF} - VCC_{SS}} \qquad (4)$$

Primary-Side Inductor Design (L_m)

With build-in slope compensation, HFC040 0 supports CCM when the duty cy cle exceeds 50%. Set a ratio (K$_P$) of the primary ind uctor's ripple current amplitude vs. th e peak curr ent value to 0<$K_P \leq$1, wh ere K_P=1 for DCM. Figure 12 shows the relevant waveforms. A larger in ductor lead s to a smaller K $_P$ leads, which can reduce RMS current but increase tra nsformer size. An optim al K_P value is between 0.6 and 0.8 for the universal input range and 0.8 t o 1 for a 230VAC inpu t range.
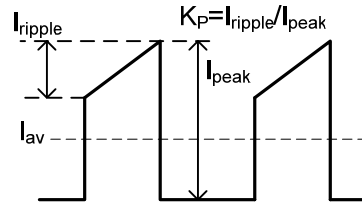

Figure 12: Typical Primary-Current Waveform

The input p ower (P_{in}) at the minimum input ca n be estimated as

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \qquad (5)$$

Where V_O is the outpu t voltage, I_O is the rate d output curr ent, η is t he estimat ed efficiency. Generally, η is between 0.75 and 0.85 depending on the input range and output application.

For CCM at minimum input, the converter dut y cycle is:

$$D = \frac{(V_O + \cdot V_F) \ N}{(V_O + \cdot V_F) \ N + V_{in(min)}} \qquad (6)$$

Where:

V_F is the secondary diode's forward voltage,

N is the transformer turn ratio, and

$V_{in(min)}$ is the minimum voltage on bulk capacitor.

The MOSFET turn-on time is

$$\tau_{on} = D \cdot \tau_s \qquad (7)$$

Where τ_s is the frequency jitter's dominant switching period, $\frac{1}{\tau_s} = f_s \quad 65kHz$.

The averag e, peak, ripple and valley values of the primary current are described as follows:

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \qquad (8)$$

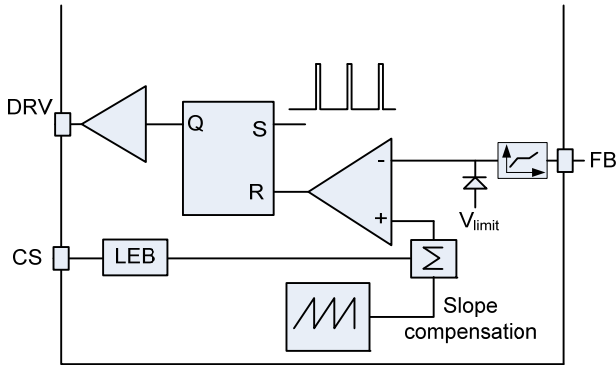$$I_{peak} = \frac{I_{av}}{(1 - \cdot \frac{K_P}{2}) \ D} \qquad (9)$$

$$I_{ripple} = K_P \cdot I_{peak} \qquad (10)$$

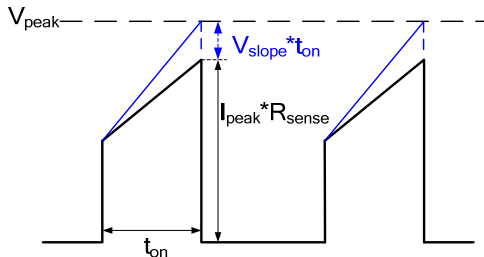$$I_{valley} = (1 - K_P) \cdot I_{peak} \qquad (11)$$

The following equation estimates L_m as

$$L_m = \frac{V_{in(min)} \cdot \tau_{on}}{I_{ripples}} \qquad (12)$$

Current-Sense Resistor

a) Peak-Current-Comparator Circuit

b) Typical Waveform

Figure 13: Peak-Current Comparator

Figure 13 shows the peak-current-comparator logic and the subsequent waveform. When the sum of the sensing resistor voltage and the slope compensator reaches V_{peak}, the comparator goes HIGH to reset the RS flip-flop, and the DRV pin is pulled down to turn off the MOSFET. The maximum current limit (V_{limit}, as measured by V_{CS}) is 0.95V. The slope compensator (V_{slope}) is ~25mV/µs. Given the margin, use 0.95×V_{limit} as V_{peak} at full load. The voltage on sensing resistor is then:

$$V_{sense} = 95\% \cdot V_{limit} - V_{slope} \cdot \tau_{on} \qquad (13)$$

So the value of the sense resistor is

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \qquad (14)$$

Select the current sense resistor with an appropriate power rating based on the power loss:

$$PI_{sense} = \left[\left(\frac{I_{peak} + I_{valley}}{2}\right)^2 + \frac{1}{2}\left(I_{peak} - I_{valley}\right)^2\right] \cdot D \cdot R_{sense}$$
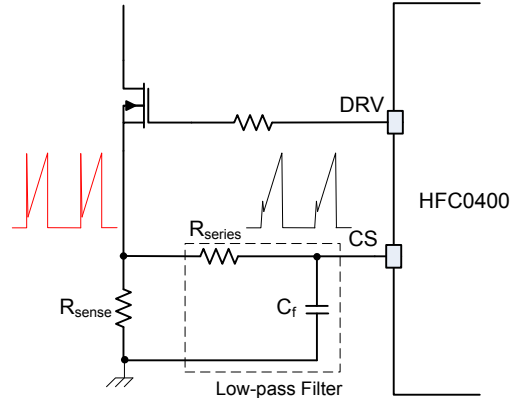
(15)

Low-Pass Filter on CS Pin

Figure 14: Low-Pass Filter on CS Pin

A small capacitor connected to the CS pin with R_{series} forms a low-pass filter for noise filtering when the MOSFET turns on and off, as shown in Figure 14. The series resistance (R_{series}) should not exceed 1k Ω. The low-pass filter's R×C constant should not exceed 1/3 of the leading-edge blanking period for SCP (LEB2, 270ns), or the filtered sensed voltage won't reach the SCP point (1.5V) to trigger SCP if an output short circuit occurs.

Jitter Period

Frequency jitter is an effective method to reduce EMI by dissipating energy. The nth-order harmonic noise bandwidth is

$B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$, where Δf is the frequency jitter amplitude. If B_{Tn} exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150 kHz, 9 kHz for noise frequency between 150kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on the TIMER pin determines the period of the frequency jitter. A 10µA current source charges the capacitor; when the TIMER voltage reaches 3.2V, another 10µA current

source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period In theory, a smaller f_{jitter} is more effective at EMI reduction. However, the measurement bandwidth requires that f_{jitter} should be large compared to spectrum analyzer RBW for effective EMI reduction. Also, f_{jitter} should be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. So for most applications, select f_{jitter} between 200Hz and 400Hz.

X-Cap Discharge Time

Figure 9 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input and under no-load because the energy on X-cap dissipates but won't transfer to the bulk capacitor.

The maximum discharge delay time is

$$\tau_{delay} = 32 \cdot \tau_{jitter} \qquad (16)$$

When the high-voltage current source turns on, a constant supply current (I_{HV}, 1.6mA typically) flows into HV. The current-source discharge time for the X-cap to drop to 37% of peak voltage can be estimated by:

$$\tau_{discharge} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{ac(max)}}{I_{HV}} \qquad (17)$$

Where C_X is the X-cap capacitance, $V_{ac(max)}$ is the maximum AC-input RMS value.

The first discharging period is $16 \times \tau_{jitter}$, with subsequent period equal to $48 \times \tau_{jitter}$. The sections times approximately eequals:

$$n = \frac{\tau_{discharge} - 16 \cdot \tau_{jitter}}{48 \cdot \tau_{jitter}} + 1 \qquad (18)$$

Rounding n determins the number of detecting sections, as every section is $16 \times \tau_{jitter}$, the detecting time is shown as follow:

$$T_{detect} = 16 \cdot \tau_{jitter} \cdot n \qquad (19)$$

As a result, the total discharge time is then.

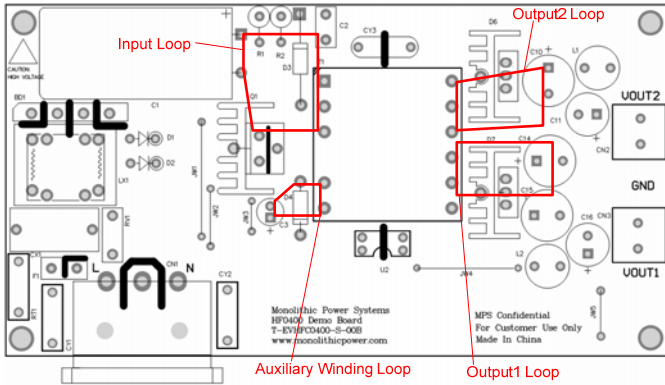$$\tau_{total} = \tau_{delay} + \tau_{discharge} + \tau_{detect} \qquad (20)$$

The total discharge time is relative to τ_{jitter}. For example, if C_{TIMER} is 47nF and τ_{jitter}=3.7ms, the X-cap discharge margin is 1s due to X-cap value deviations (around ±10% typically), select an X-cap less than 3.3µF.

Though the X-cap has been discharged, it may still retain a high-voltage on the bulk capacitor. For safety, make sure it is released before the debugging the board.
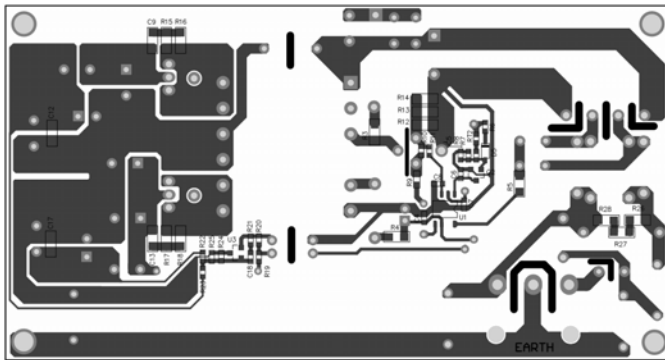
PCB Layout Guide

PCB layout is important to achieve reliable operation, good EMI performance, and good thermal performance. Follow these guidelines to optimize performance.

1) Minimize the power stage switching stage loop area. This includes the input loop (C1 - T1 - Q1 – R12/R13 – C1), the auxiliary winding loop (T1 – D4 – R4 – C3 – T1), and the output loop (T1 – D6 – C10 – T1 and T1 – D7 – C14 – T1).

2) The input loop GND and control circuit should be separate and only connect at C1.

3) Connecting the Q1 heatsink to the primary GND plane improves EMI.

4) Place the control circuit capacitors (such as those for FB, CS and VCC pins) close to IC to decouple noise.

a) Top

Design Example

Below is a design example of HFC0400 for dual-output applications.

Table 1—Design Spec.

V_{IN}	85 to 265VAC
V_{OUT1}	5V
I_{OUT1}	3A
V_{OUT2}	16V
I_{OUT2}	1.5A

b) Bottom

Figure 15: PCB Layout

Typical Application Circuit
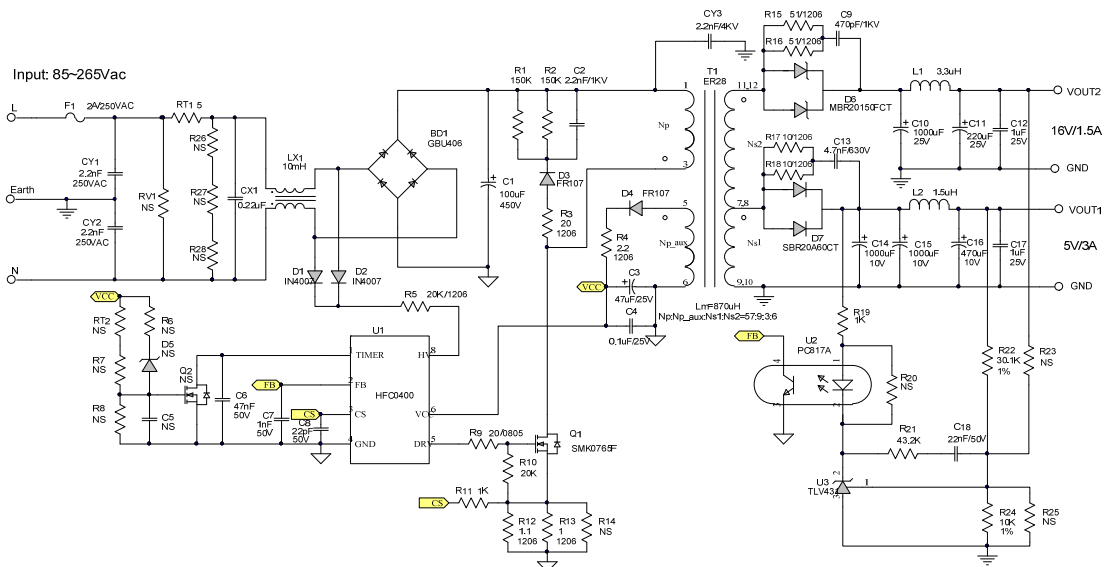
Figure 16: Example of a Typical Application

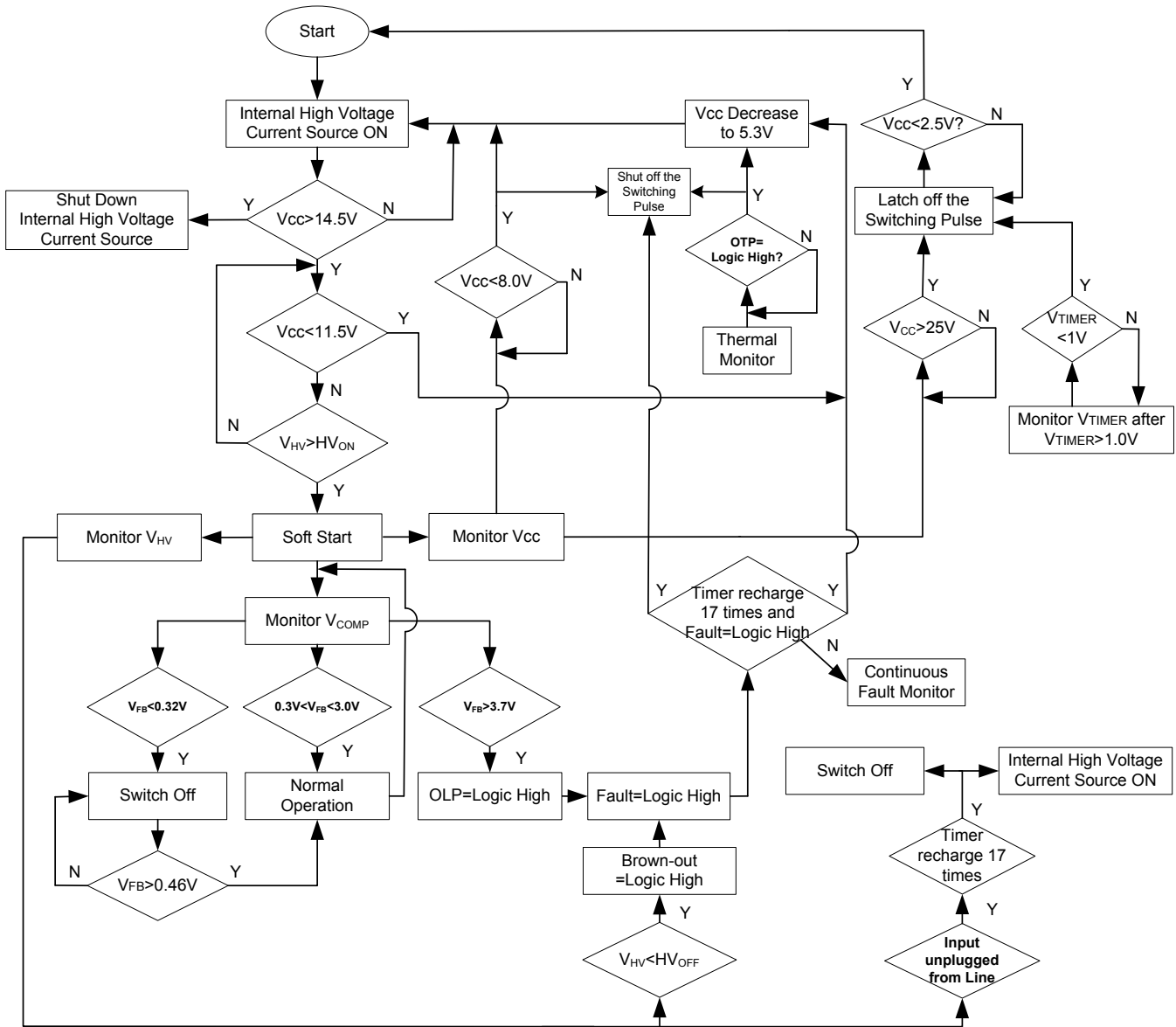a) Connection Diagram

b) Winding Diagram
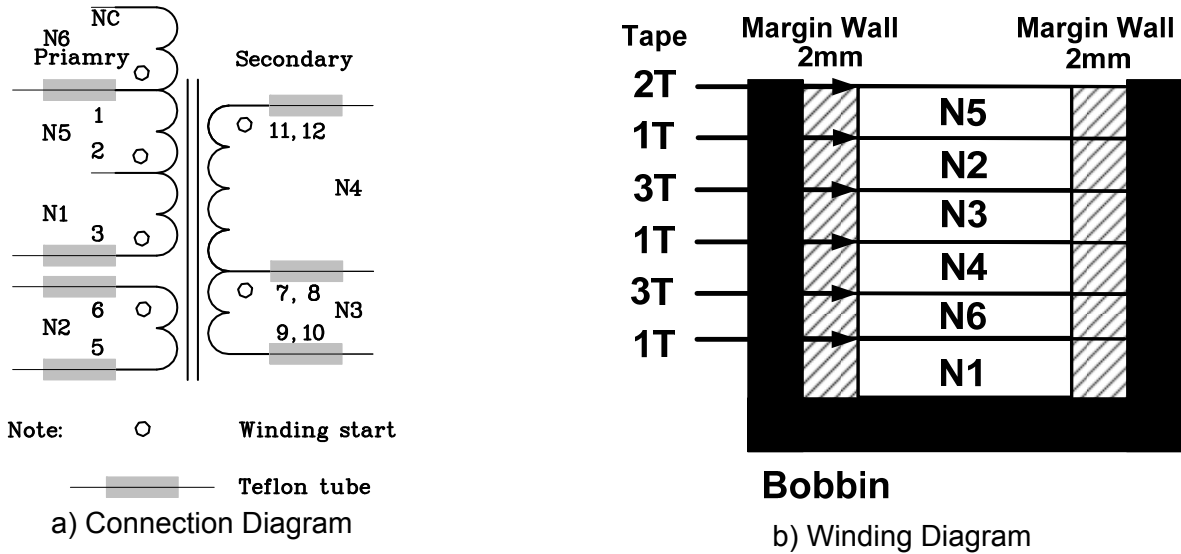
Figure 17: Transformer Structure

Table 2—Winding Order

Tape (T)	Winding	Margin Wall PRI side	Terminal Start—>End	Margin Wall SEC side	Wire Size (φ)	Turns (T)
1	N1 2mm		3—>2	2mm	0.27mm*2	28
1	N6 2mm		1—>NC	2mm	0.3mm*1	20
3	N4 2mm		7,8—>9,10	2mm	0.33mm*12	3
1	N3 2mm		11,12—>7,8	2mm	0.33mm*5	6
3						
1 N2		2mm	5—>6	2mm	0.27mm*1	9
2 N5		2mm	2—>1	2mm	0.27mm*2	29

FLOW CHART

UVLO, brown-out, OTP & OLP is auto restart, OVP on VCC and Latch-off on TIMER are latch mode

Release from the latch condition, need to unplug from the main input.

Figure 18: Control Flow Chart
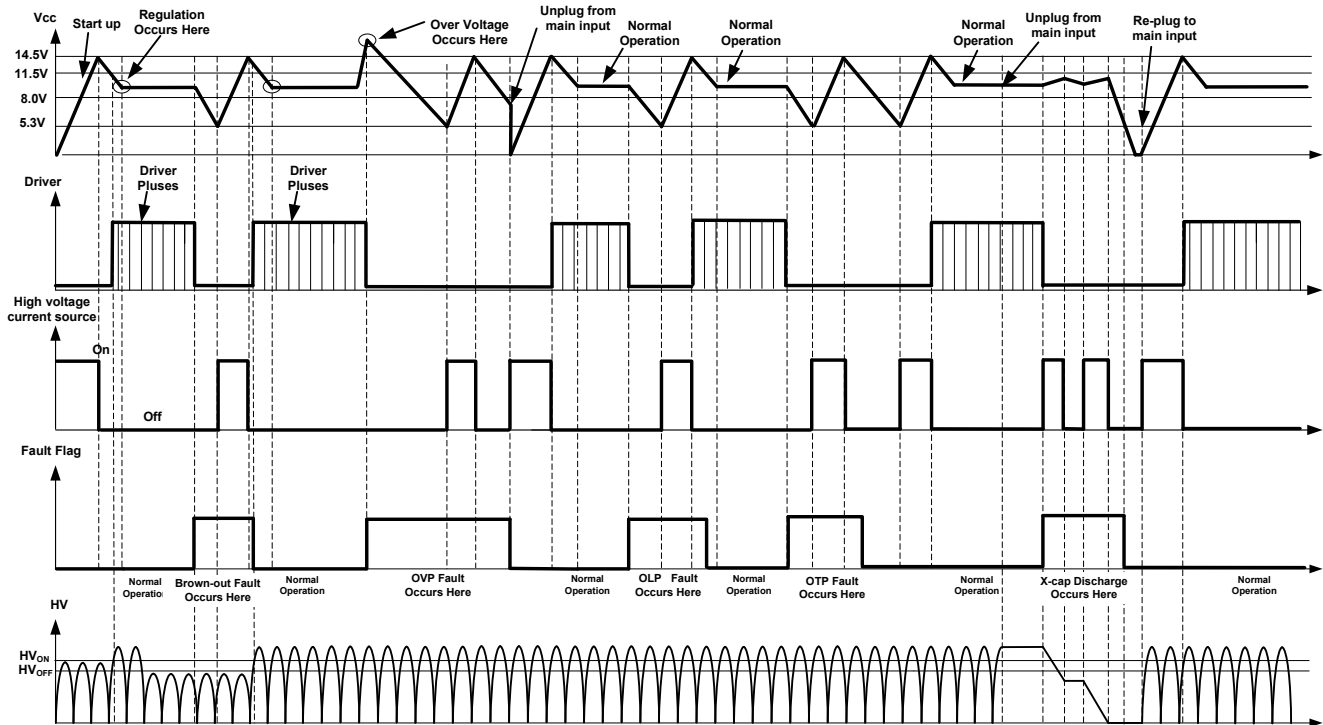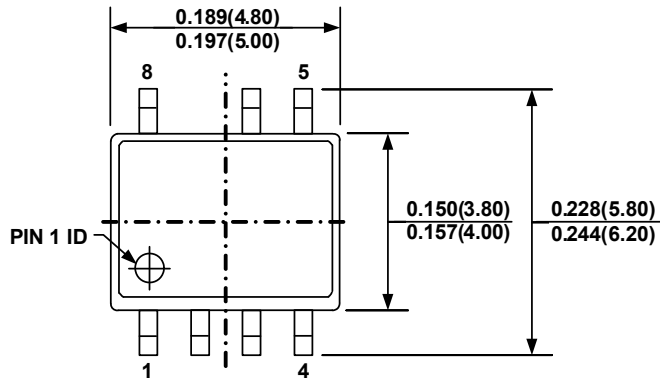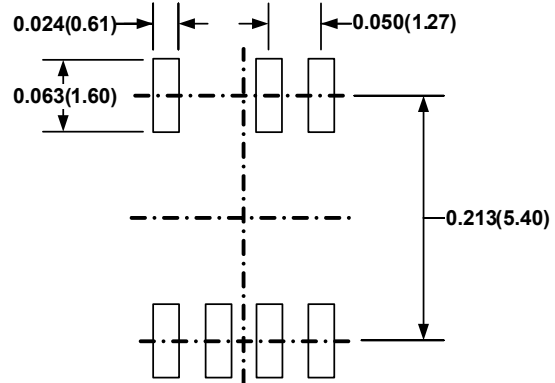
EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

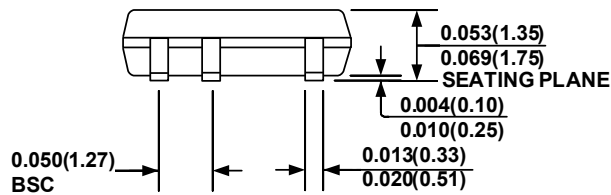**Figure 19: Signal Evolution in the Presence of Faults**

PACKAGE INFORMATION

SOIC8-7A

TOP VIEW

0.189(4.80)
0.197(5.00)

8   5

PIN 1 ID

1   4

0.150(3.80)
0.157(4.00)

0.228(5.80)
0.244(6.20)

RECOMMENDED LAND PATTERN

0.024(0.61)

0.050(1.27)

0.063(1.60)

0.213(5.40)

FRONT VIEW

0.053(1.35)
0.069(1.75)

SEATING PLANE

0.004(0.10)
0.010(0.25)

0.013(0.33)
0.020(0.51)

0.050(1.27)
BSC

SIDE VIEW

SEE DETAIL "A"

0.0075(0.19)
0.0098(0.25)

DETAIL "A"

0.010(0.25)
0.020(0.50) x 45°

GAUGE PLANE
0.010(0.25) BSC

0°-8°

0.016(0.41)
0.050(1.27)
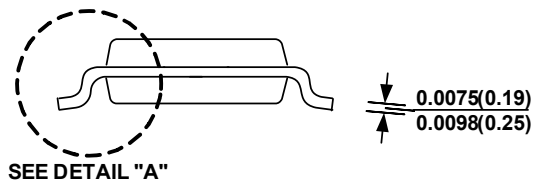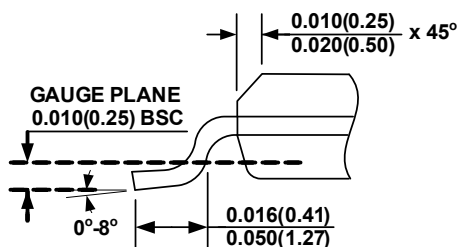
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.