The Future of Analog IC Technology®

Fixed-Frequency Flyback Controller

DESCRIPTION

The HFC0310 is a flyback controller with fixed-frequency operation.

The controller uses peak current mode to provide excellent transient response and ease loop compensation. When the output power falls below a given level, the controller enters burst mode to lower the stand-by power consumption.

An external capacitor connected between the FSET pin and GND programs the HFC0310 switching frequency. Otherwise, the HFC0310 uses a frequency shaping function that greatly reduces the noise level, and reduces the cost of the EMI filter.

The HFC0310 provides various protections, such as thermal shutdown, V_{CC} under-voltage lockout, over-load protection, over-voltage protection, and short-circuit protection.

The HFC0310 is available in a SOIC8 package.

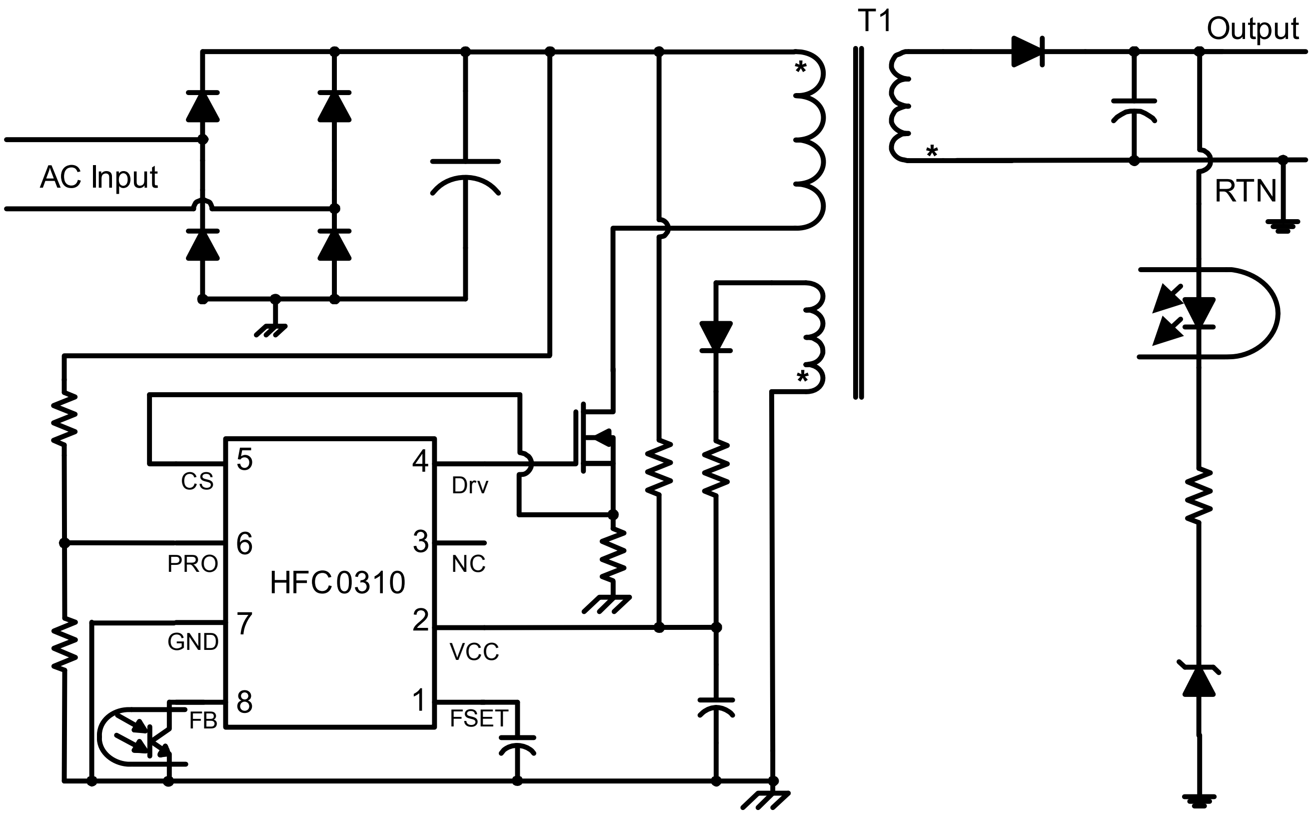
FEATURES

- Programmable switching frequency up to 600kHz
- Frequency shaping (±3.5%)
- Current-mode operation
- Very low start-up current (12μA)
- Very low standby power consumption via active-burst mode
- Internal 350ns leading-edge blanking
- Built-in 3ms soft-start function
- Internal slope compensation
- Built-in PRO pin pull-up (>3.25V) auto-restart function
- Over-temperature protection
- V_{CC} under-voltage lockout with hysteresis
- Over-voltage protection on VCC
- Time-based over-load protection
- Short-circuit protection

APPLICATIONS

- Power Meters
- Switching Mode Power Supplies
- AC/DC Adapters, Switching Chargers

TYPICAL APPLICATION



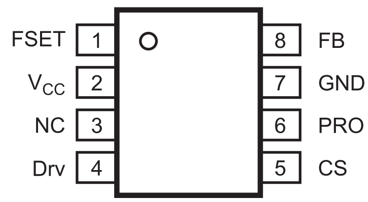
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
HFC0310GS	SOIC8	HFC0310	–40°C to +105°C

* For Tape & Reel, add suffix –Z (e.g. HFC0310GS–Z);

PACKAGE REFERENCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS [1]

Vcc .... –0.3V to 30 V
All Other Pins .... –0.3V to 7 V
Continuous Power Dissipation (T_A = +25°C) [2]
SOIC8 .... 1.04W
Junction Temperature .... 150°C
Lead Temperature .... 260°C
Storage Temperature .... -60°C to +150°C
Thermal Shut Down .... 150°C
Thermal Shut Down Hysteresis .... 40°C
ESD Capability Human Body Model (All Pins except Drain) 2.0kV
ESD Capability Machine Model 200V
Operating Temperature........... –40°C to +105°C

Recommended Operation Conditions [3]

V_{CC} to GND .... 8V to 20V
Maximum Junction Temp. (T_J) .... +125°C

Thermal Resistance [4] θ_{JA} θ_{JC}

SOIC8 .... 96 ...... 45... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} =12V, T_A=+25°C, unless otherwise noted

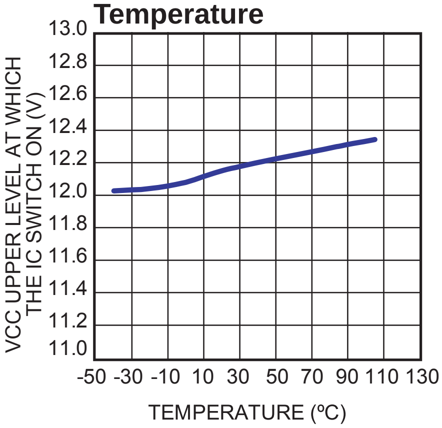
Parameter Sy	mbol	Conditions	Min	Typ	Max	Unit
Driving Signal (Pin Drv)						
Sourcing Resistor	R_H			20		Ω
Sinking Resistor	R_L			10		Ω
Supply Voltage Management (Pin Vcc)						
V_{CC} Upper Turn-On/Off Level	V_{CCH}		11	12	13	V
V_{CC}, Lower Turn-On/Off Level	V_{CCL}		8.5	9.3	10	V
Start-Up Current	I_{ST}	V_{CC}=V_{CCH}-0.5V, Before start up	12		20	μA
V_{CC} OVP Level	V_{OVP}		23.3	24.5	25.7	V
V_{CC} Protection-Enabled Recharge Level	V_{CCR}		5.7	6.2	6.7	V
Internal IC Consumption, Protection Phase	I_{Pro}	V_{CC} =6.0V		8	10	μA
Feedback Management (Pin FB)						
Internal Pull-Up Resistor	R_{FB}		12.5	14	15.5	kΩ
Internal Pull-Up Voltage	V_{UP}			4.5		V
FB to Current-Set–Point Division Ratio	I_{DIV}			3		
Internal Soft-Start Time	t_{SS}			3		ms
Falling FB Level Where the Regulator Enters Burst Mode	V_{BURL}			0.5		V
Rising FB Level where the Regulator Exits Burst Mode	V_{BURH}			0.7		V
Over-Load Set Point	V_{OLP}		3.5	3.8	4	V
Over-Load Delay Time	t_{Delay}	Fs=100 kHz		82		ms
Timing Capacitor(FSET)						
Maximum Voltage on the FSET Capacitor	$V_{FSETmax}$		0.83	0.87	0.91	V
Source Current	I_{FSET}		45	53	61	μA
FSET Capacitor Discharge Time (Active at drive turn on)	t_{DISCH}			400		ns
Frequency Spectrum Shaping range, in percentage of Fs	$R_{Shaping}$			±3.5		%
Current Sampling Management (CS)						
Leading-Edge Blanking for Current Sensor	t_{LEB1}			350		ns
Leading-Edge Blanking for SCP	t_{LEB2}			240		ns
Maximum Current Set-Point	V_{CS}		0.91	0.95	0.98	V
Short-Circuit–Protection Set Point	V_{SC}		1.55	1.65	1.75	V
Internal-Slope–Compensation Ramp	S_{Ramp}	f_S=100kHz		38		mV/μs
Protection Management (PRO)						
Protection Voltage	V_{PRO}		3.1	3.25	3.4	V
Protection Hysteresis	V_{HY}			0.2		V

PIN FUNCTIONS

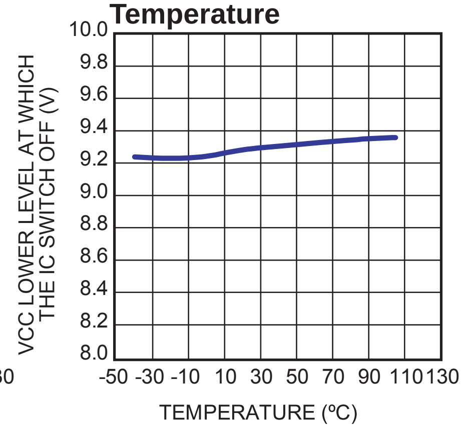
Package Pin #	Name	Description
1	FSET	Switching Converter Frequency Set. Connect a capacitor to GND to set the switching frequency up to 600kHz.
2	V_{CC}	Supply Voltage. Connect to a 47µF bulky capacitor and a 0.1µF ceramic capacitor for most applications. When V_{CC} rises to 12V, the IC starts switching; when it falls below 9.3V, the IC stops switching.
3	NC	Not Connected. This pin ensures adequate creepage distance.
4	Drv	Drive Signal Output.
5	CS	Primary Current Sense.
6	PRO	Pull up PRO to shut down the IC with hysteresis.
7	GND	Ground.
8	FB	Feedback. The output voltage from the external compensation circuit is fed into this pin. This pin and the current sense signal from Source determines the PWM duty cycle. A feedback voltage of 3.8V triggers over-load protection, while 0.5V triggers burst-mode operation. The regulator exits burst-mode operation and enters normal operation when the FB voltage reaches 0.7V

TYPICAL CHARACTERISTICS

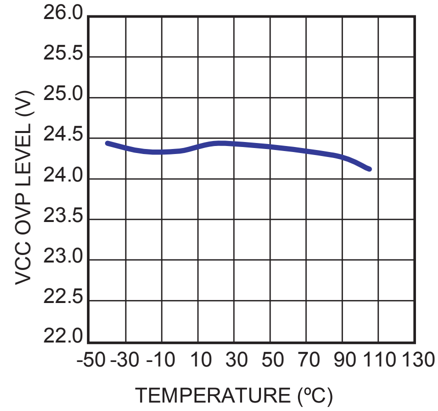
VCC Upper Level at which the IC switch on vs. Temperature



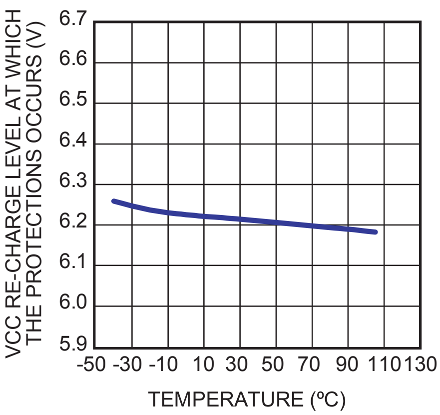
VCC Lower Level at which the IC switch off vs. Temperature



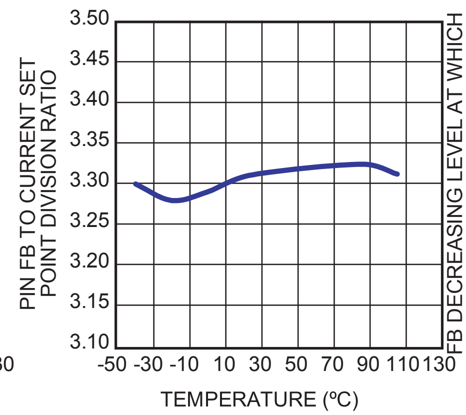
VCC OVP Level vs. Temperature



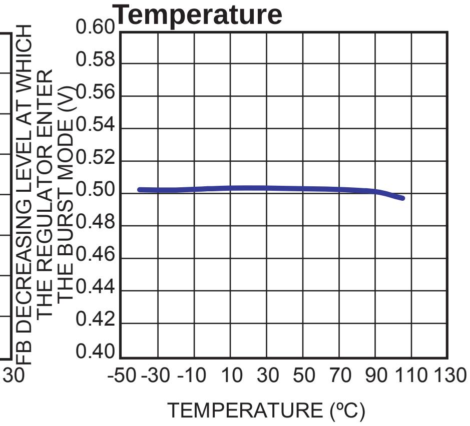
VCC Re-Charge Level at which the protections occurs vs.Temperature



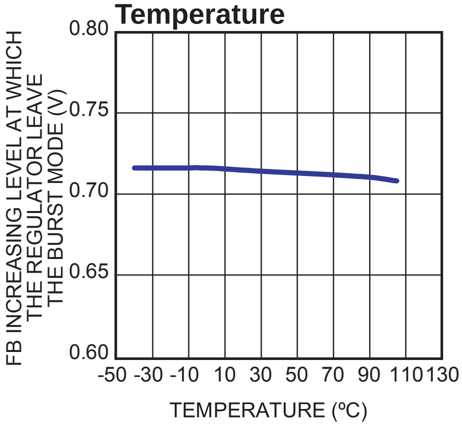
Pin FB to Current Set point Division Ratio vs. Temperature



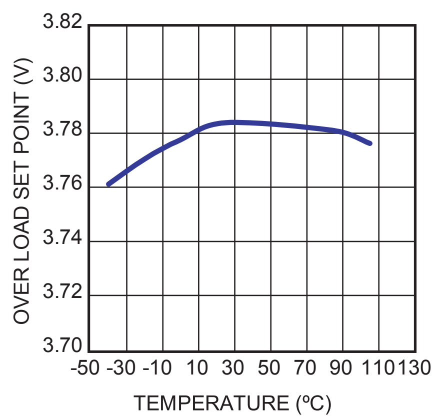
FB Decreasing Level at which the Regulator enter the Burst Mode vs. Temperature



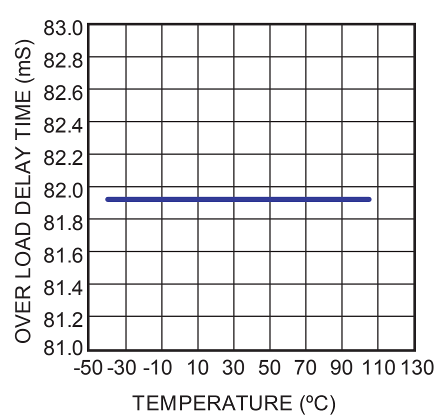
FB Increasing Level at which the Regulator leave the Burst Mode vs. Temperature



Over Load Set Point vs. Temperature

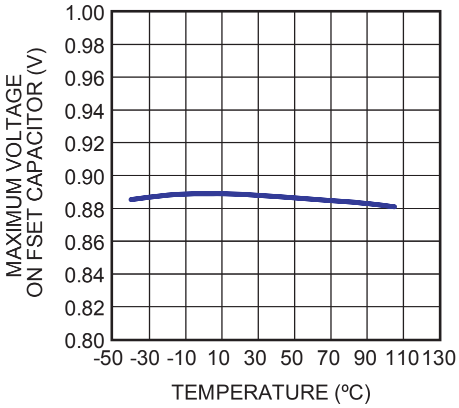


Over Load Delay Time vs. Temperature

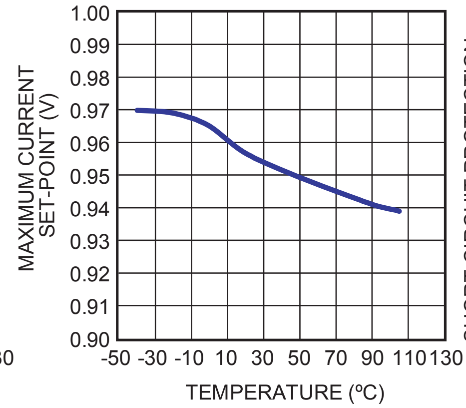


TYPICAL CHARACTERISTICS *(continued)*

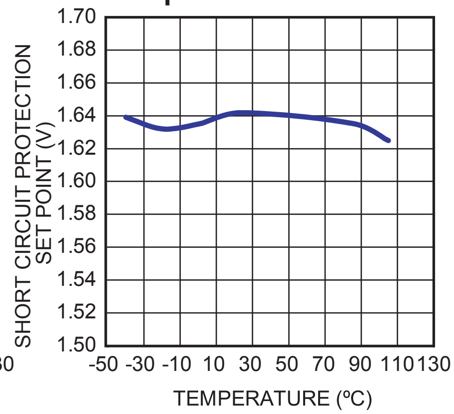
Maximum Voltage On FSET Capacitor vs. Temperature



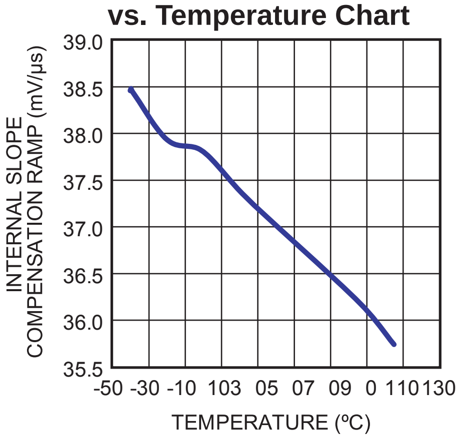
Maximum Current Set-point vs. Temperature



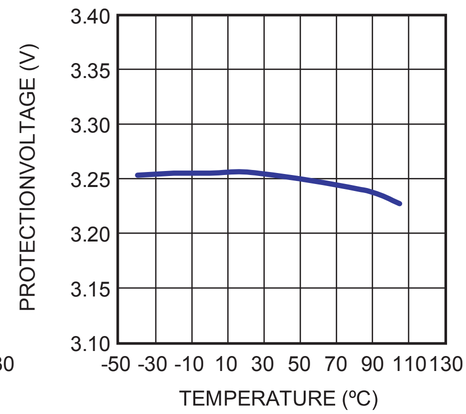
Short Circuit Protection Set Point vs. Temperature Chart



Internal Slope Compensation Ramp vs. Temperature Chart



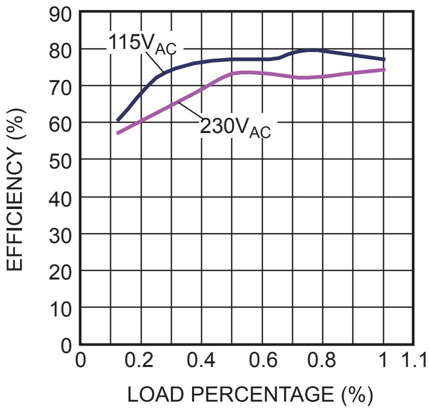
Protection Voltage vs. Temperature



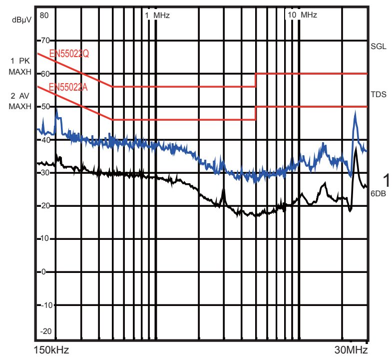
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=230VAC, V_{OUT1}=12V/0.8A, V_{OUT2}=8V/0.2A, V_{OUT3}=8V/0.05A, T_A=+25°C, unless otherwise noted.

Efficiency

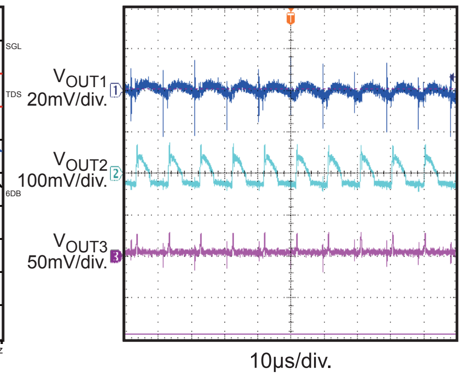


EMI



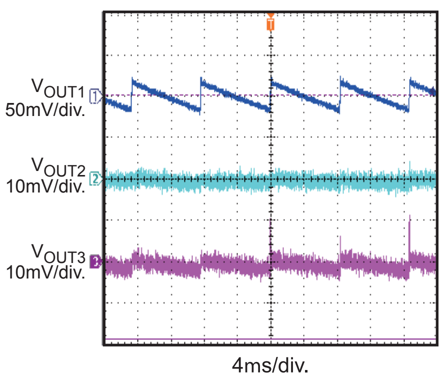
Output Voltage Ripple

Full Load



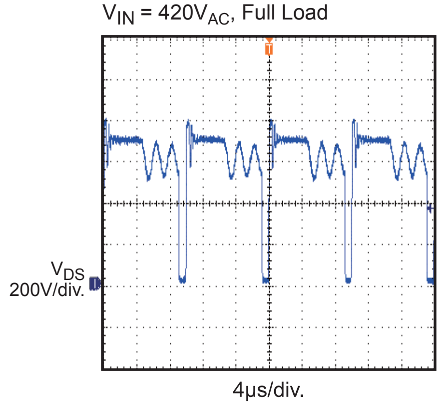
Output Voltage Ripple

No Load



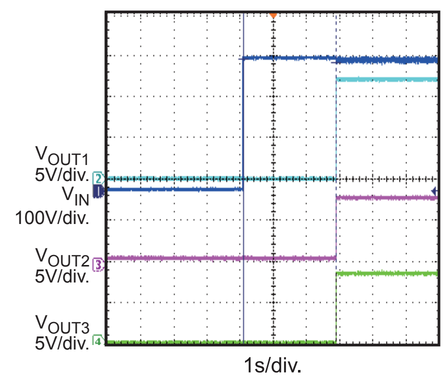
Stress

V_{IN} = 420V_{AC}, Full Load



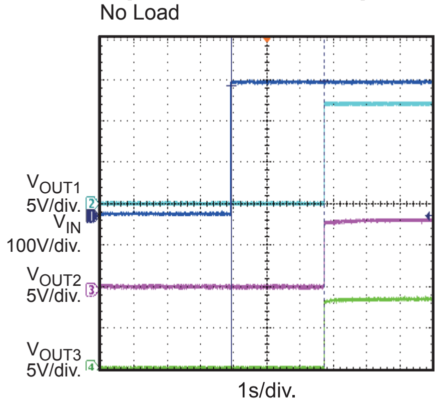
Input Power Startup

Full Load



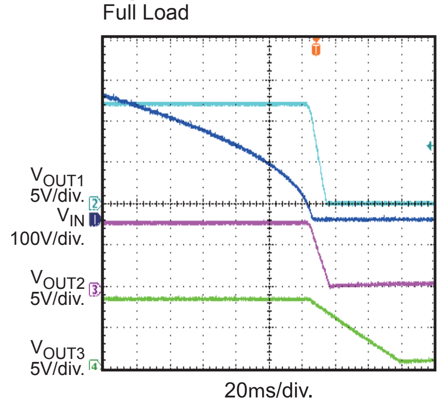
Input Power Startup

No Load



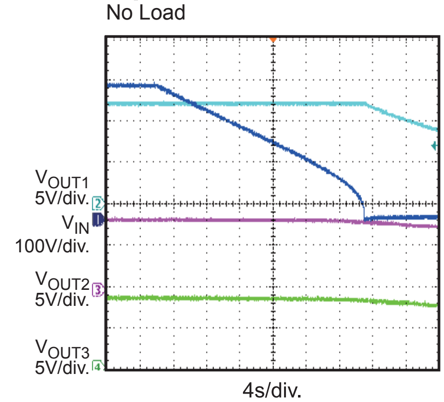
Input Power Shutdown

Full Load



Input Power Shutdown

No Load

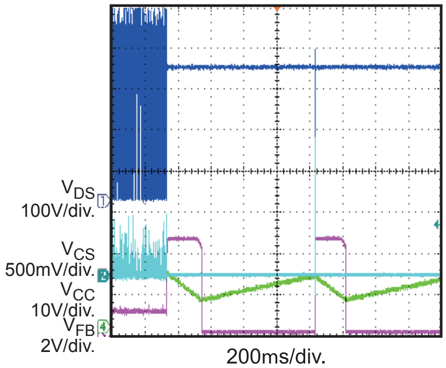


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=230VAC, V_{OUT1}=12V/0.8A, V_{OUT2}=8V/0.2A, V_{OUT3}=8V/0.05A, T_A=+25°C, unless otherwise noted.

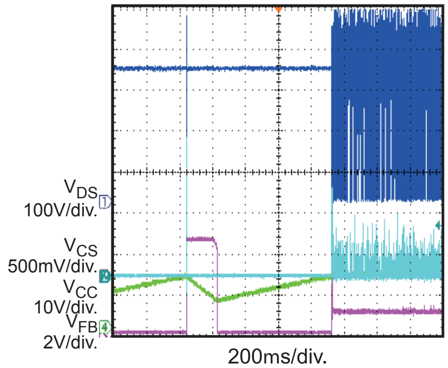
SCP Entry

Full Load



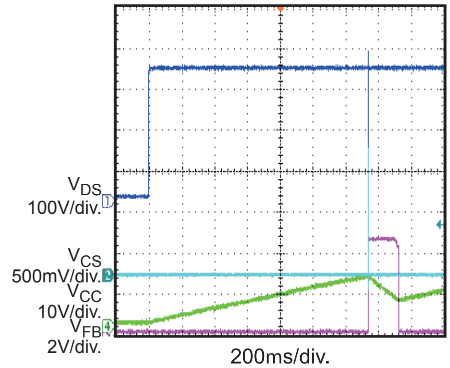
SCP Recovery

Full Load



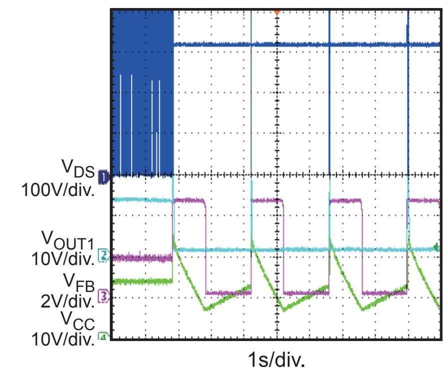
SCP Startup

Full Load



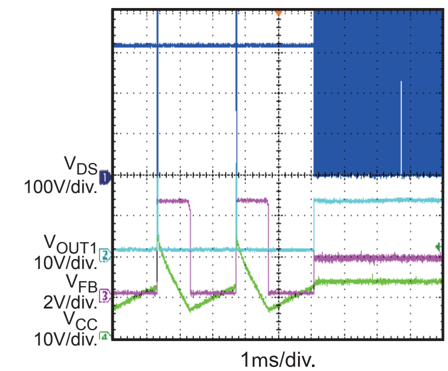
OVP Entry

Full Load



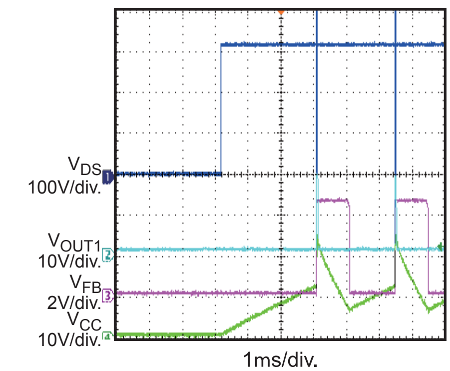
OVP Recovery

Full Load



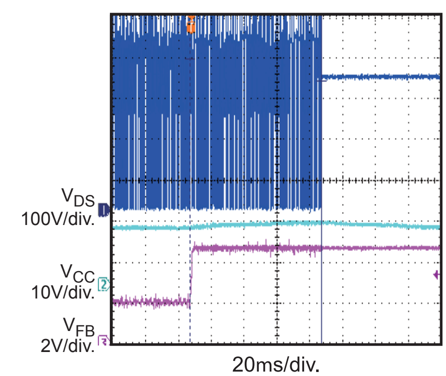
OVP Startup

Full Load



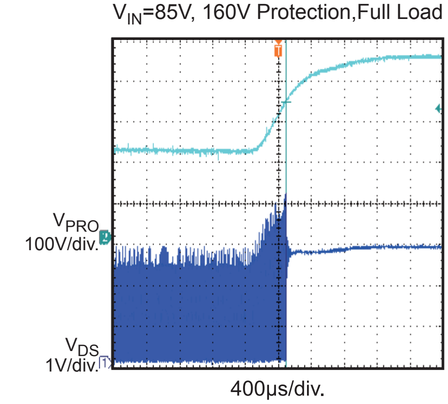
OCP Protection

Full Load



Pro Protection

V_{IN}=85V, 160V Protection,Full Load



BLOCK DIAGRAM

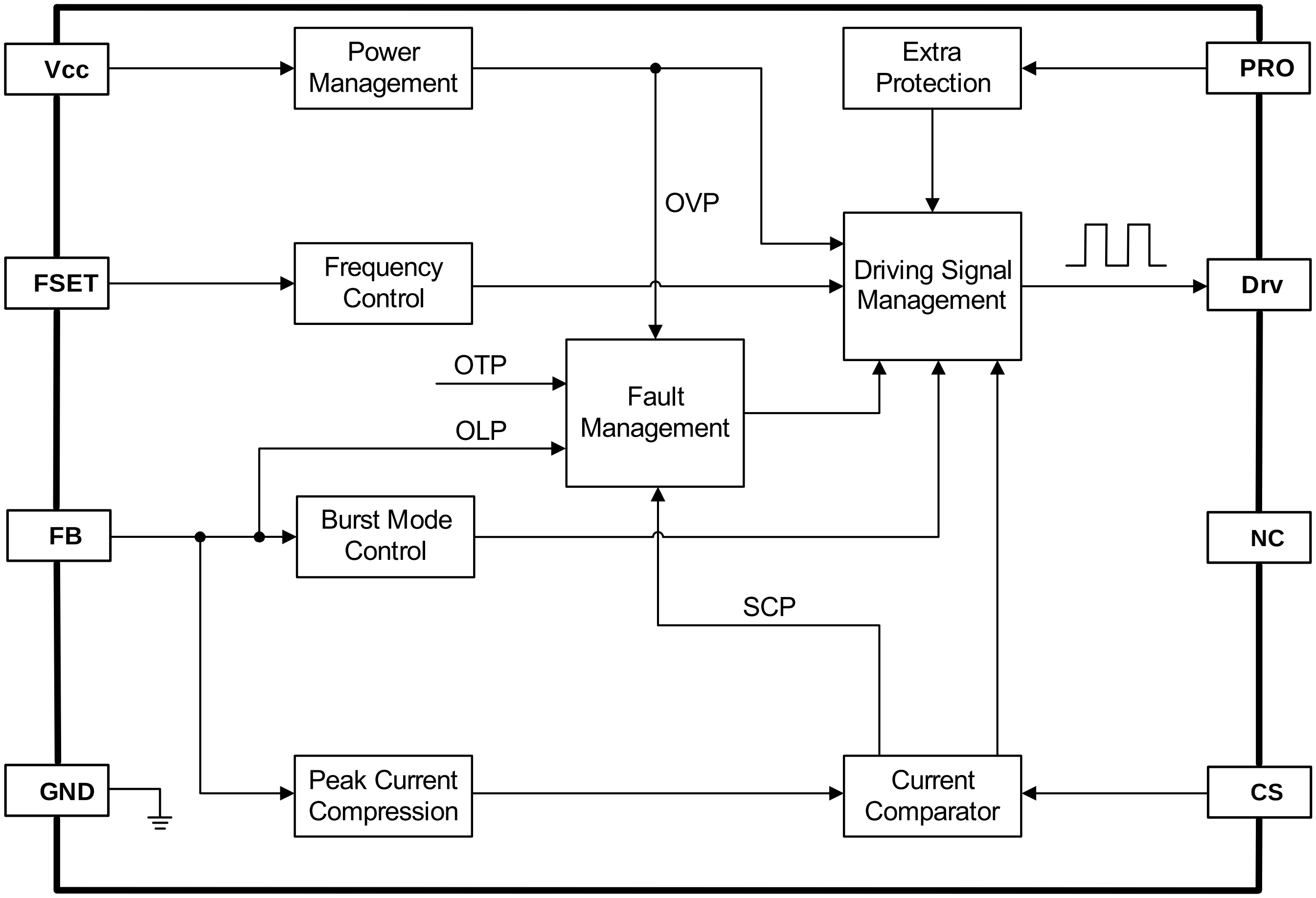


Figure 1: Functional Block Diagram

OPERATION

The HFC0310 incorporates all the necessary features to build a reliable switch-mode power supply. Its high level of integration requires very few external components. It has burst-mode operation to minimize the stand-by power consumption at light load. Protection features—such as auto-recovery for over-load protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), or thermal shutdown (TSD) for over-temperature protection (OTP)—contribute to a safer converter design without increasing circuit complexity.

PWM Operation

The HFC0310 is a fully integrated converter with adjustable-frequency peak-current-mode control PWM switching regulators. The output voltage is measured at FB through a resistive voltage divider, amplifier, and optocoupler. The voltage at the FB pin is compared to the internally measured switch current to control the output voltage. The integrated MOSFET turns on at the beginning of each clock cycle. The current in the inductor increases until it reaches the value set by the FB voltage, and then the integrated MOSFET turns off.

Start-Up and V_{CC} UVLO

During start-up, the IC only consumes the start up current (typically 12µA), and the current supplied through the start-up resistor charges the V_{CC} capacitor.

The IC starts switching and the current increases to 1mA when V_{CC} reaches 12V. At this point, the transformer's auxiliary winding powers the IC. When V_{CC} falls below 9.3V, the regulator stops switching and the current through the start up resistor charges the V_{CC} capacitor again.

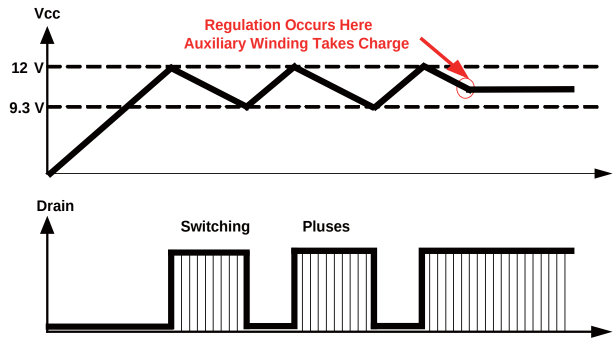


Figure 2: V_{CC} UVLO

The lower threshold of VCC under-voltage lock-out (UVLO) decreases from 9.3V to 6.2V when fault conditions occur, such as OLP, OVP, and OTP.

Soft-Start

To reduce stress on the primary MOSFET and the secondary diode during start-up and to smoothly establish the output voltage, the HFC0310 has an internal soft-start circuit that gradually increases the primary current sense threshold, which determines the MOSFET peak current during start-up. The pulse-width of the power switching device progressively increases to establish optimal operating conditions until the feedback control loop takes charge.

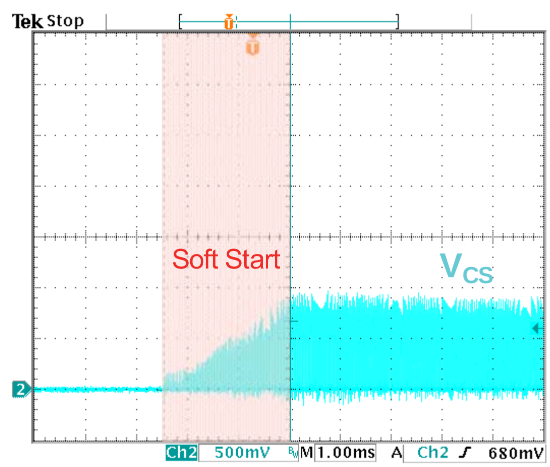


Figure 3: Soft Start

Switching Frequency

The capacitor between the FSET pin and GND sets the switching frequency of the HFC0310. Estimate the oscillator frequency as per the equation below:

$$f_S = \frac{1}{400\times10^{-9}\times C\times\frac{0.87}{53\times10^{-6}}}\ Hz$$

Over Voltage Protection

Monitoring the V_{CC} pin via a 20μs time constant filter allows the HFC0310 to enter OVP during an over-voltage condition; typically when V_{CC} goes above 24.5V. The controller will resume operation after the fault disappears.

Over-Current Protection

The HFC0310 continuously monitors the FB pin. When FB pulls up to 3.8V, if after a 8192 switching cycle delay the fault signal is still present, the HFC0310 shuts down as soon as the power supply undergoes an overload. When the fault disappears, the power supply resumes operation.

Short-Circuit Protection

By monitoring the CS pin, the HFC0310 shuts down when the voltage rises higher than 1.65 V, to indicate a short circuit. The HFC0310 enters a safe low-power mode that prevents any lethal thermal or stress damage. As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown

When the temperature of the IC exceeds 150°C, the OTP is activated and the controller enters auto-recovery mode.

Burst Operation

To minimize stand-by power consumption, the HFC0310 implements burst mode at no load or light load. As the load decreases, the FB voltage decreases. The IC stops switching when the FB voltage drops below the lower threshold, V_{BRUL} (0.5V). Then the output voltage drops at a rate dependent on the load. This causes the FB voltage to rise again due to the negative feedback control loop. Once the FB voltage exceeds the upper threshold, V_{BRUH} (0.7V), the switching pulse resumes. The FB voltage then decreases and the whole process repeats. Burst-mode operation alternately enables and disables the switching pulse of the MOSFET. Hence switching loss at no load or light load conditions is greatly reduced.

Figure 4 shows the signals generated by burst-mode operation.

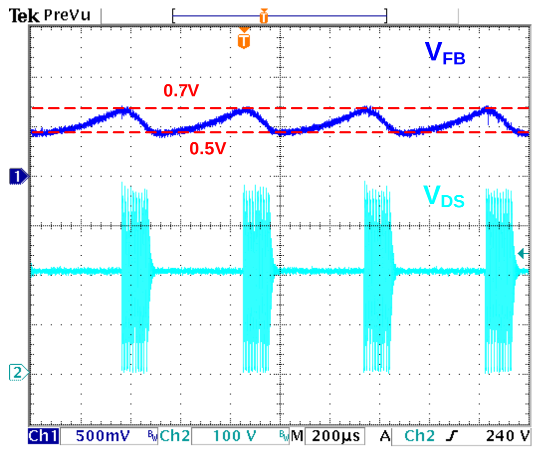


Figure 4: Burst-Mode Operation

PRO Pin

The PRO pin provides extra protection against abnormal conditions. Use the PRO pin for input OVP and/or other protections. If the PRO pin voltage exceeds 3.25V, the IC shuts down. As soon as the fault disappears, the power supply resumes operation.

Leading-Edge Blanking (LEB)

In normal operation, a shunt resistor between the Source pin and Ground senses the primary peak current. The FB voltage sets the turn-off threshold of the MOSFET, $V_{SENSE}=V_{FB}/3$. When the shunt resistor voltage drops to V_{SENSE}, the MOSFET turns off.

During start-up and over-load condition, the primary peak current threshold is internally limited to 0.95V even if V_{FB} voltage exceeds 2.85V to avoid excessive output power and lower the switch voltage rating.

In order to avoid turning off the MOSFET by mis-triggered spikes shortly after the switch turns on, the IC implements a 350ns leading-edge blanking period. During blanking time, any trigger signal on the source pin is blocked. Figure 5 shows the primary-current–sense waveform and the leading-edge blanking.

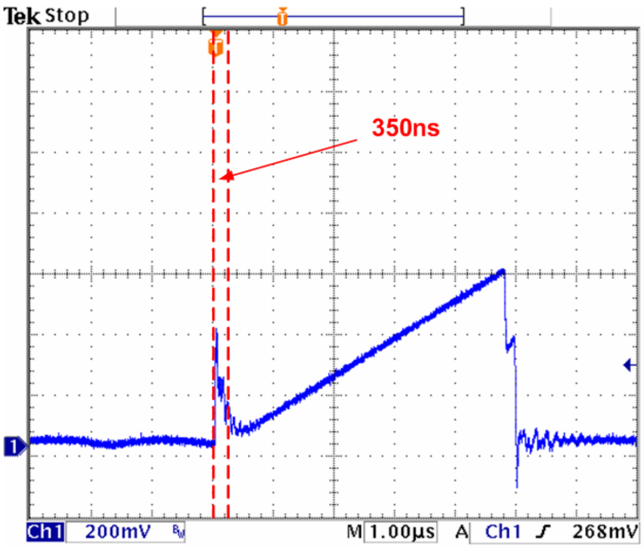


Figure 5: Leading-Edge Blanking

Design Example

The following is a de sign examp le using th e application guidelines for the given specifications:

V_{IN}	85V to 420V
V_{OUT1}	12V
V_{OUT2}	8V
V_{OUT3}	8V
f_{SW}	100kHz

The detaile d applicatio n schematic is shown in Figure 6. T he typical performance and circuit waveforms have bee n shown in the Typi cal Performance Characteristics section. For more possible applications of this device, please refer to the related Evaluation Board datasheets.

TYPICAL APPLICATION CIRCUITS

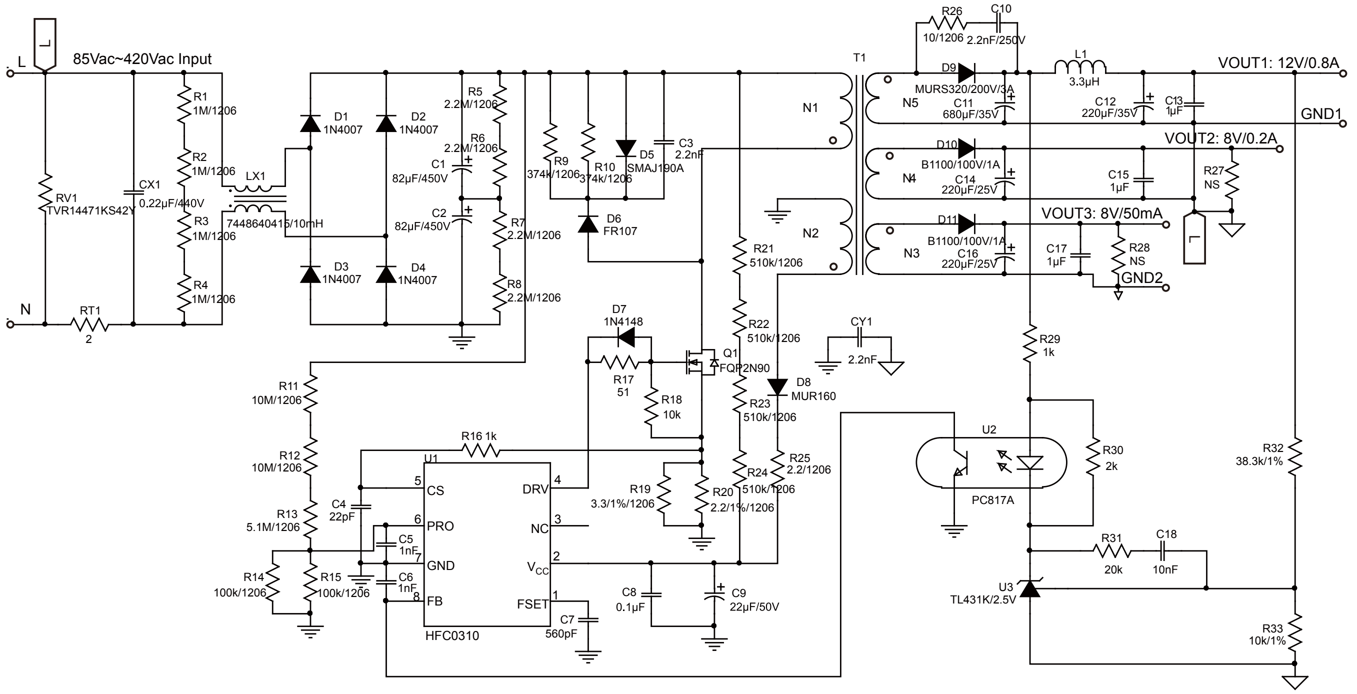
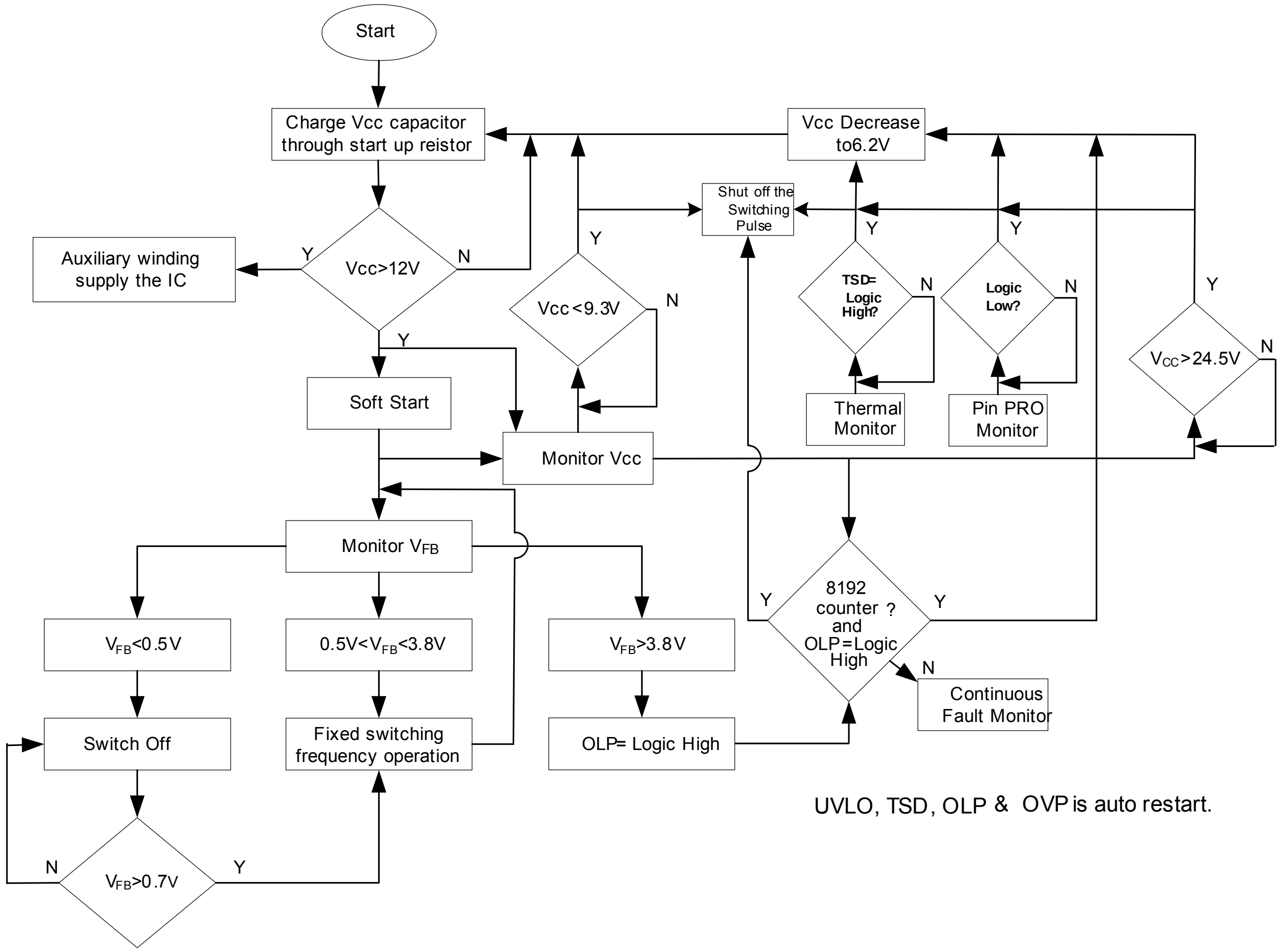


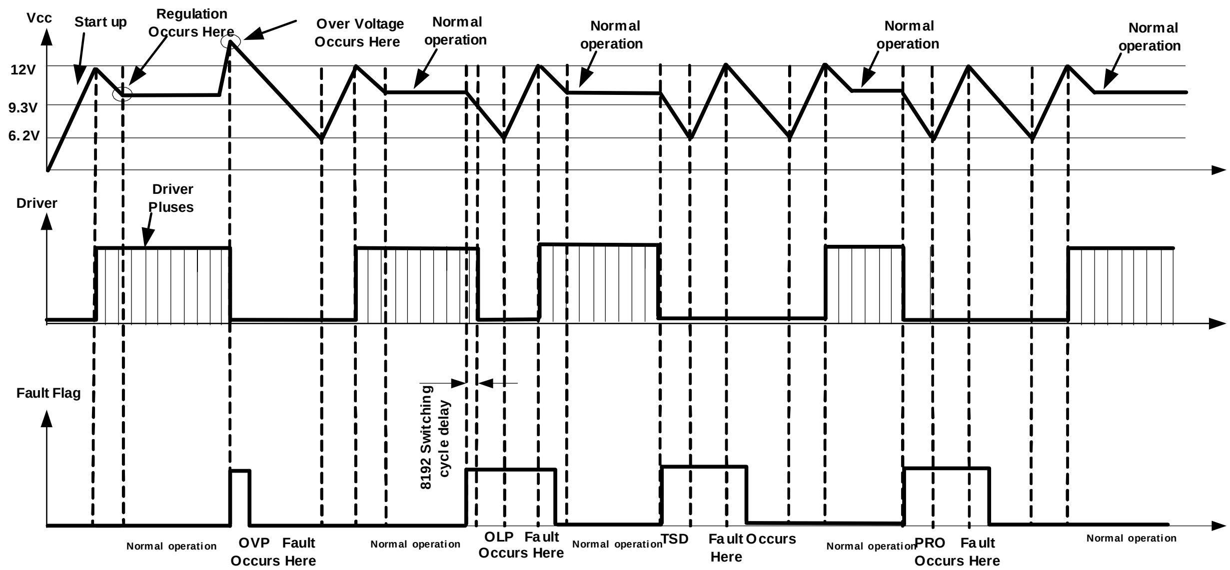
Figure 6: Typical Application Schematic

FLOW CHART



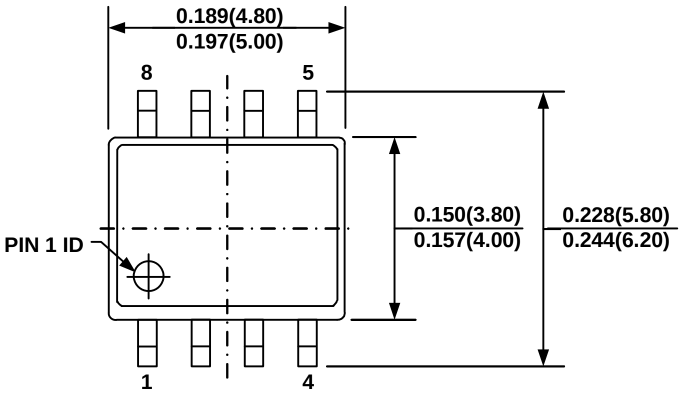
UVLO, TSD, OLP & OVP is auto restart.

SIGNAL EVOLUTION IN THE PRESENCE OF FAULTS

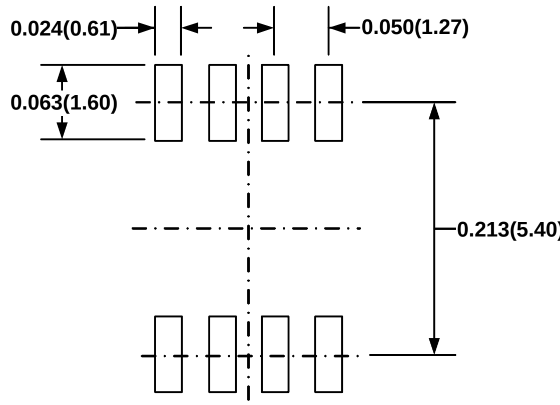


PACKAGE INFORMATION

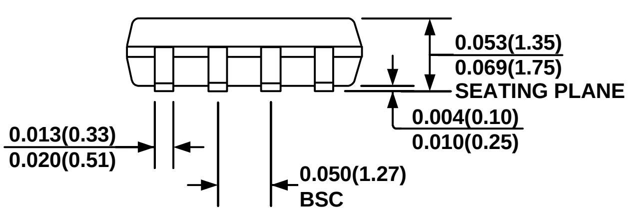
SOIC8



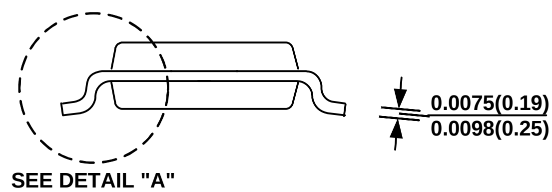
TOP VIEW



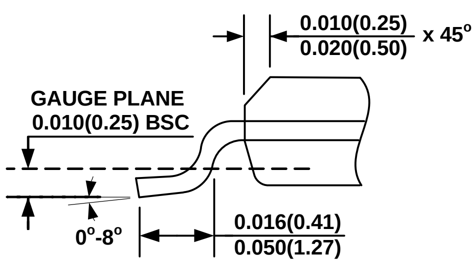
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.