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6-Port DS3/E3/STS-1 Integrated Line Termination Device for ATM, Packet Processing and TDM Transport

M29306 – DS3/E3/STS-1 "Line-Card-on-a-Chip"

The M29306 provides the most complete physical-layer solution for flexible DS3/E3/STS-1 ATM, packet and TDM services on a single chip. The M29306 aggressively drives down cost for existing solutions and as well as reduces PCB real-estate and power.

Each port of the M29306 operates independently allowing for a mix of different rates and protocols. This flexibility allows service providers to provide a combination of clear channel DS3/E3 for packet, DS3/E3 ATM UNI or T3/E3/STS-1 TDM services on the same card. This enables ADMs/OEDs and MSPPs to deploy a single line card that supports the simultaneous mapping for SDH or SONET transport of both DS3 and E3.

The M29306 integrates all the functional physical-layer blocks for a DS3/E3/STS-1 line card. It includes: 6 independent electrical line interface units (LIUs) with built-in digital jitter attenuators (DJAT), 12 DS3/E3 framers, and 6 STS-1 framers. Each port is supported by a number of protocol options that may be selected on a per port basis from high level data link controllers (HDLC), ATM cell delineators, or DS3/E3 SONET/SDH mappers/demappers. The only requirement on the line side is the addition of transformers and passive termination.

The device incorporates flexible system interfaces to support cell/packet termination into an industry-standard system bus of UTOPIA Level 2 (UL2) for ATM, POS-PHY Level 2 or SPI-3 for HDLC packets, and STS-12/STM-4 support for the SONET/SDH traffic via a standard 8-bit, 77 MHz TDM telecom bus. Thus, a channelized OC-12/STM-4 can be broken down to DS3/E3 streams by the M29306 on a channel-by-channel basis.

KEY FEATURES

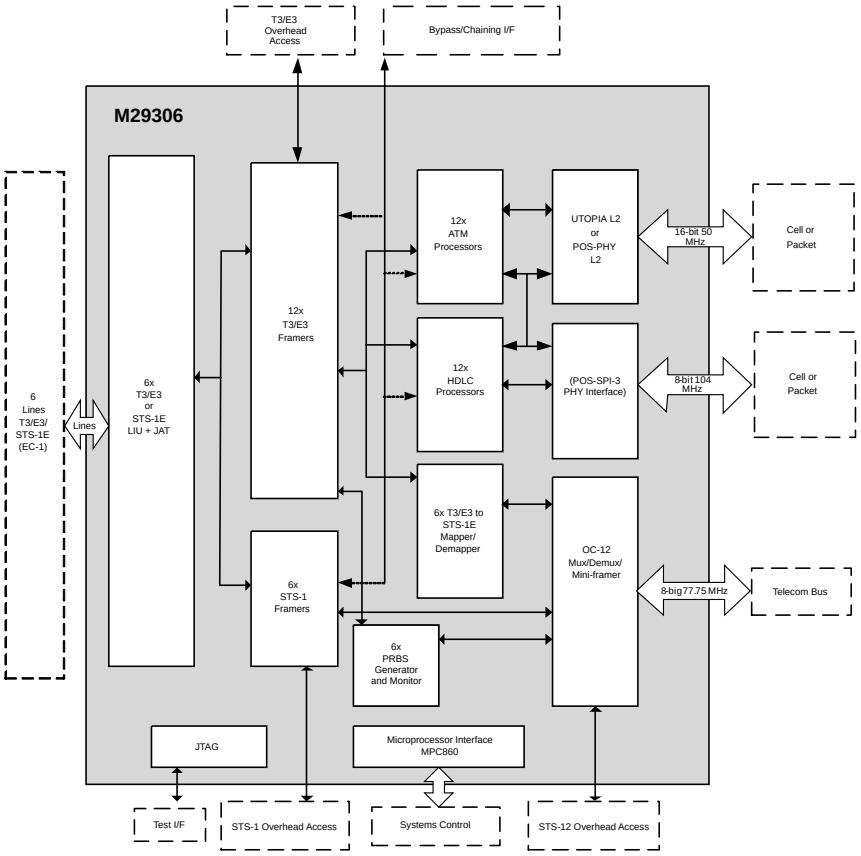
- High integration – LIUs with DJAT, T3/E3, STS-1 framers/mappers, STS-12/STM-4 framer, ATM & HDLC processors
- Flexibility – mix ATM, TDM and packet as well as T3, E3 and STS-1 services on one device
- Easy implementation – TAP software + high integration = faster time-to-market
- Parallel 8-bit, 77.76 MHz TDM telecom bus
- ATM/packet interfaces
  - SPI-3, 8-bit 25–104 MHz
  - UTOPIA Level 2/POS-PHY Level 2, 16-bit 25-50 MHz
- Fractional T3/E3 support
- T3/E3/STS-1 payload access
- Embedded CLADs for supported line rates
- Pattern generator/detector for BERT
- Comprehensive loopbacks

The M29306 requires only one 19.44 MHz reference clock (passive crystal) for generating all the necessary internal line rate clocks and enabling the same reference clock to be available on an output pad. In addition it can use a 77.76 MHz or 155.52 MHz reference.

Fractional DS3/E3 service is also supported through a bypass mode that allows external access to the DS3/E3 channel's data stream between the framer and the ATM/HDLC control allowing for external processing of the payload. This bypass mode also provides the capability of chaining two M29306s together to support a 12 line to one system side implementation. A STS-1 bypass on each of the STS-1 framers also allows for external access to the STS-1 payload.

For maintenance, the M29306 supports pseudo-random bit sequence (PRBS) testing and a full set of loopback functions are provided at different functional blocks.

Using the telecom application package (TAP) software to abstract the physical registers, developers can easily implement the M29306 solution, reducing design time.



M29306 Functional Block Diagram

Product Features

- 6 DS3/E3/STS-1E LIUs with jitter attenuation/desynchronization
  - Adaptive receive equalizer enables > 1800 ft of cable reach
  - Programmable transmit pulse mask configuration
  - Dynamic loop bandwidth to comply with all standard intrinsic and output jitter requirements
- 12 T3/E3 framers support T3-M13, T3-M23, T3 C-bit parity E3-G.751, E3-G.832
- 12 ATM processors support both direct (for C-Bit parity/M13/M23 T3 and G.832 E3) and PLCP-based mapping (for C-Bit parity DS3/M13/M23 and E3-G.751)
- 12 bit-synchronous HDLC processors
- 6 DS3/E3 mappers/demappers supporting T3/VC-3/AU-3; T3/TUG-3/AU-4; E3/VC-3/AU-3; E3/TUG-3/AU-4
- 6 STS-1 SONET/SDH framers support transport overhead access; includes monitor and generator
- STS-12/STM-4 SONET/SDH TDM supporting mapping/demapping of STS-1E or TUG-3 into/from STS-12/STM-4 frame
- Pointer processing
- Transport overhead insertion and extraction
- Parallel 77.76 MHz x 8-bit telecom bus interface
- ATM/packet interfaces
  - SPI-3 8-bit 25–104 MHz for HDLC packets
  - UTOPIA Level 2/POS-PHY Level 2, 16-bit 25–50 MHz ATM cells or HDLC packets
- Fractional T3/E3 interface for external FPGA or ASIC
- Synchronous 16-bit microprocessor interface bus at 30–77 MHz bus rate
  - Glueless connection to Motorola MPC860
- Local (source) and remote (line) loopback capability at various internal points in the device
- PRBS detector and generator supporting framed and unframed modes
- JTAG (IEEE 1149.1) boundary scan
- Single rail 1.8 V core supply with 3.3 V LvTTL I/O, 1.8V LVDS I/O
- Embedded CLADs internally generating the T3, E3, STS-1 clocks
- -40C to +85C operation

Applications

- SONET/SDH ADM/OED
- MSPP
- NGDLC/BLC
- Optical ADM
- PON OLT
- DCS
- Media Gateway

Ordering Information

- M29306-12P

www.mindspeed.com/salesoffices

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