

N-Channel Reduced Q_g , Fast Switching MOSFET

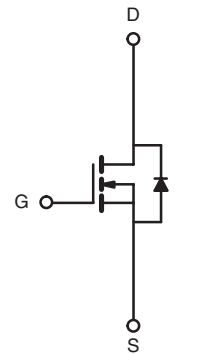
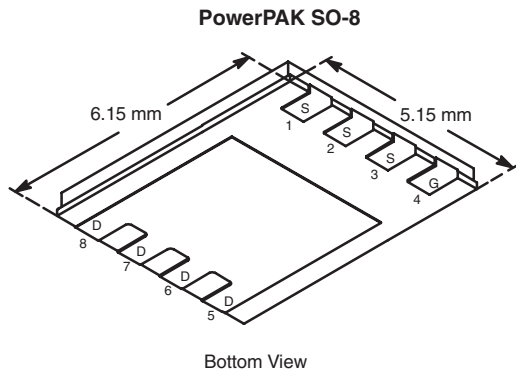
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.0185 at $V_{GS} = 10$ V	15
	0.030 at $V_{GS} = 4.5$ V	12

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- High-Efficient PWM Optimized
- 100 % R_g and UIS Tested



RoHS
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET

Ordering Information: Si7652DP-T1-E3 (Lead (Pb)-free)
Si7652DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted ^a			
Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	30	
Gate-Source Voltage	V_{GS}	± 25	
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_C = 25$ °C	15
		$T_C = 70$ °C	12
Pulsed Drain Current	I_{DM}	40	A
Continuous Source Current (Diode Conduction) ^a	I_S	3.2	
Single-Pulse Avalanche Current	I_{AS}	15	mJ
Avalanche Energy	E_{AS}	11.25	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	3.9
		$T_A = 70$ °C	2.5
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS ^a				
Parameter		Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	R_{thJA}	24	32	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	7	9	

Notes:

- Surface Mounted on 1" x 1" FR4 board, $t \leq 10$ s.
- Maximum under steady state condition is 75 °C/W.
- See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

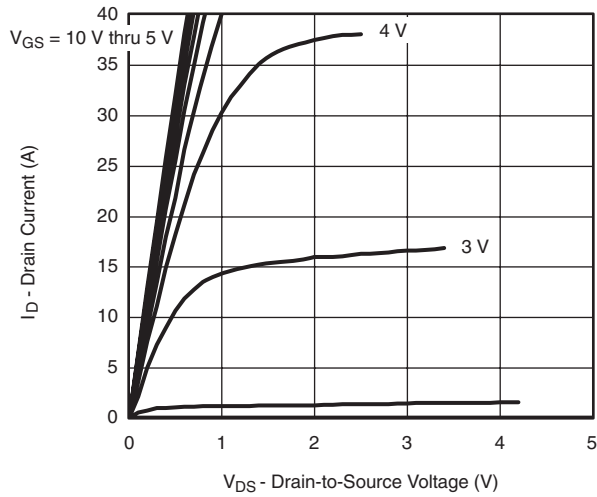
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.8		1.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$		0.0155	0.0158	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 7\text{ A}$		0.023	0.030	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 9\text{ A}$		16		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.3\text{ A}$, $V_{GS} = 0\text{ V}$		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 5.0\text{ V}$, $I_D = 9\text{ A}$		8.7	13	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_g		0.5	1.4	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$		7	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			32	50	
Fall Time	t_f			14	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		30	60	

Notes:

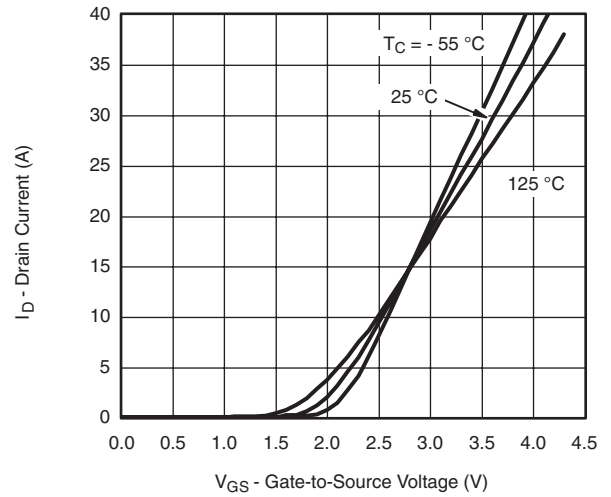
- a. Surface Mounted on 1" x 1" FR4 board, $t \leq 10\text{ s}$ Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Surface Mounted on 1" x 1" FR4 board, $t \leq 10\text{ s}$ Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

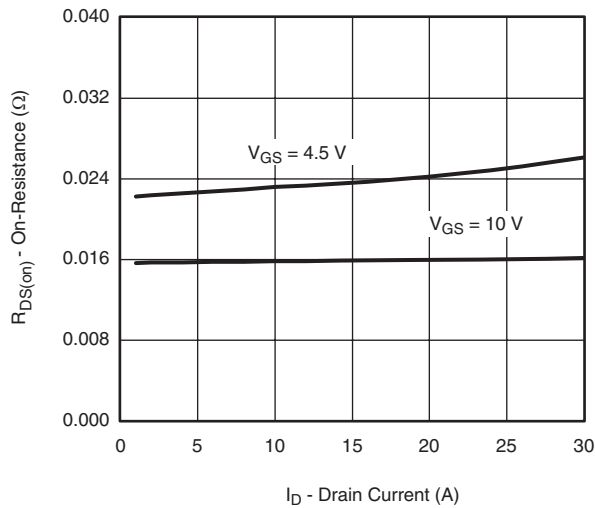
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



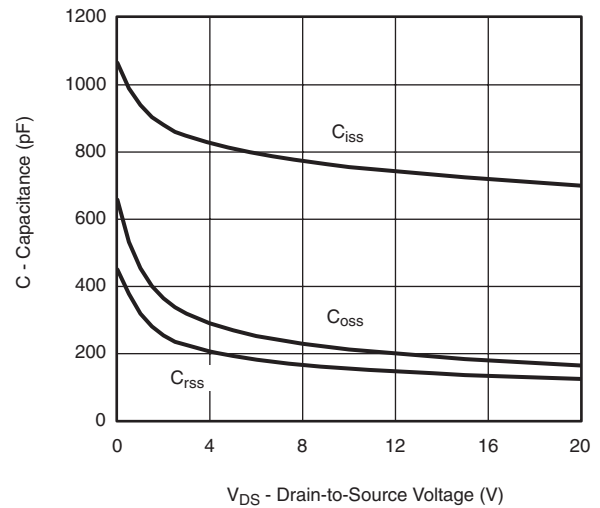
Output Characteristics



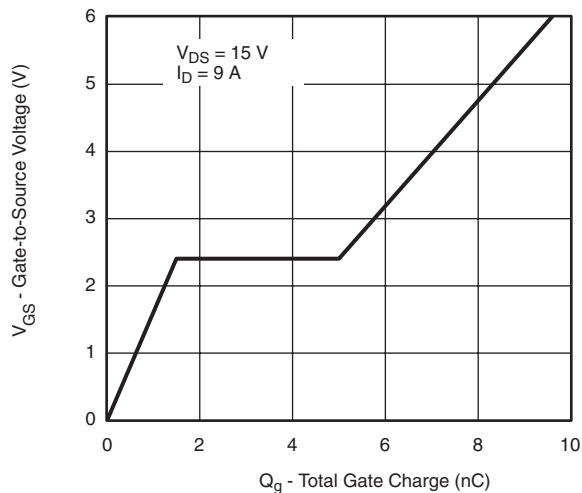
Transfer Characteristics



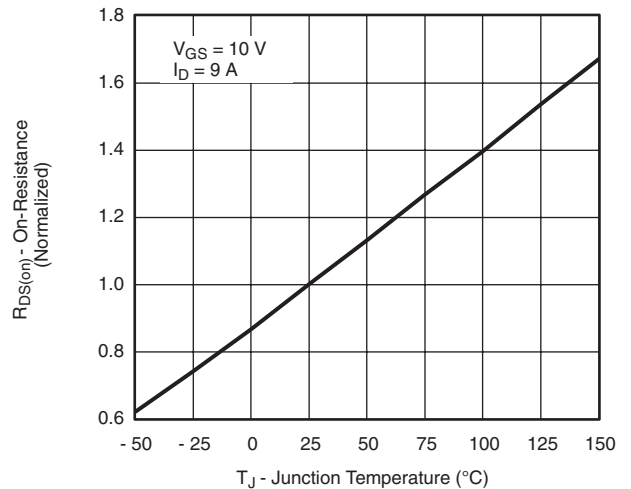
On-Resistance vs. Drain Current



Capacitance

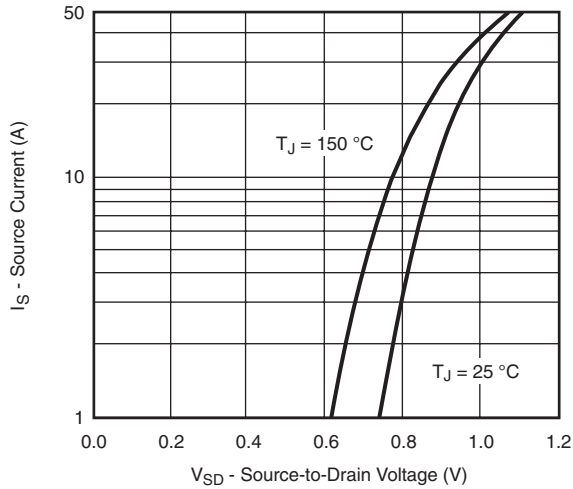


Gate Charge

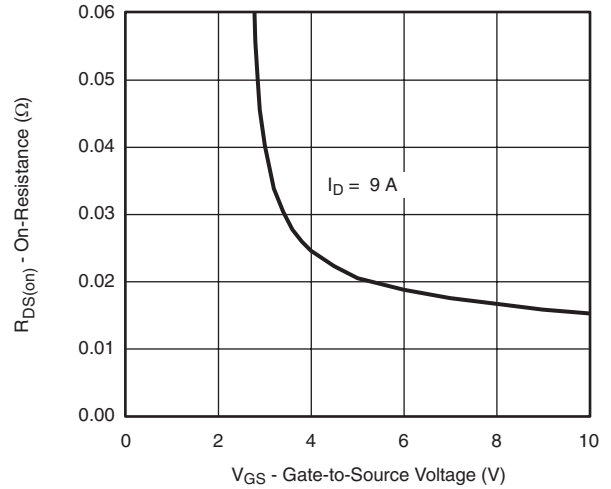


On-Resistance vs. Junction Temperature

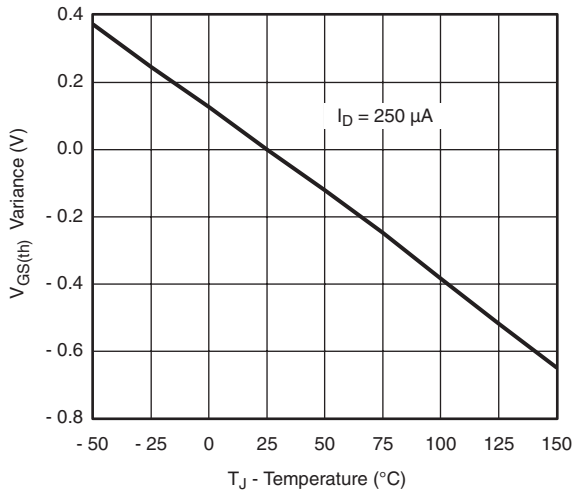
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



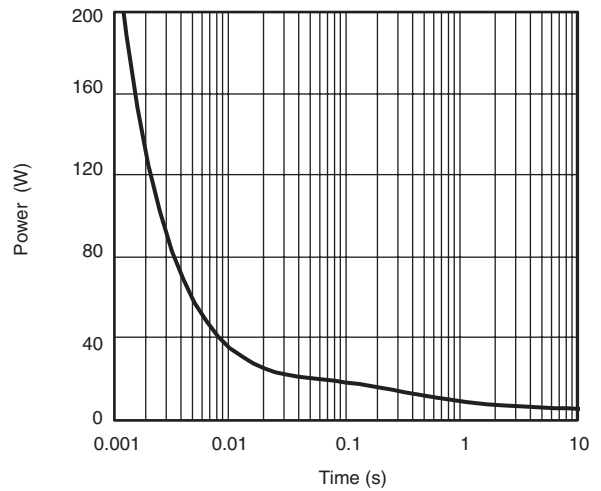
Source-Drain Diode Forward Voltage



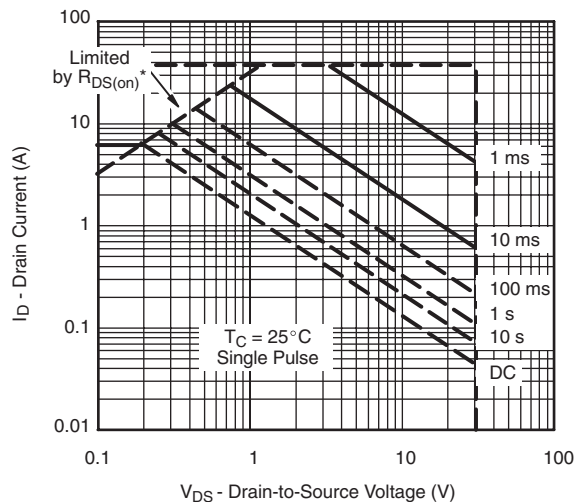
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



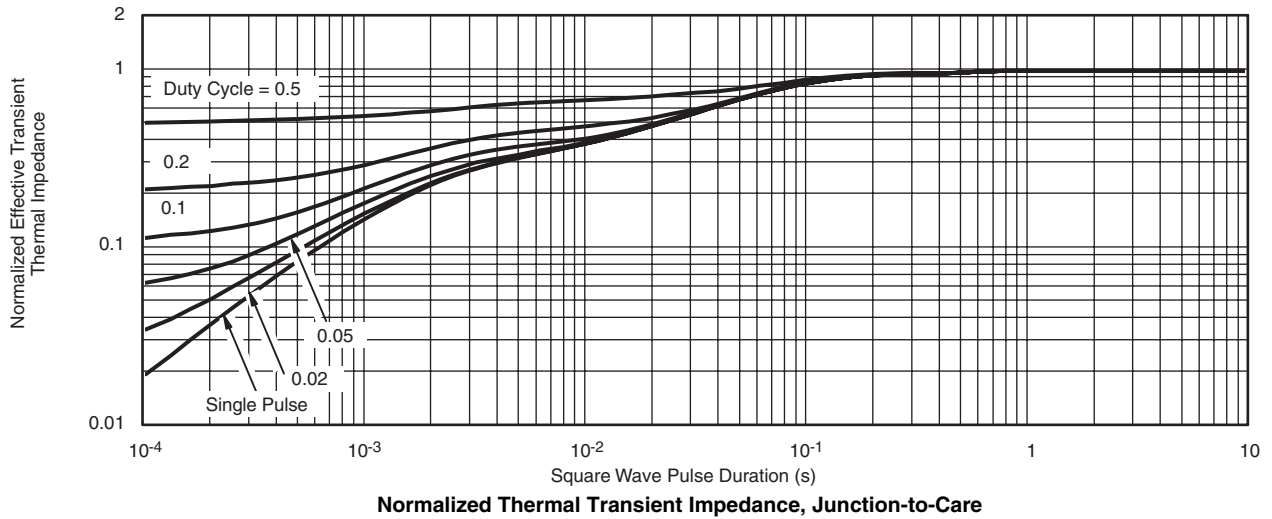
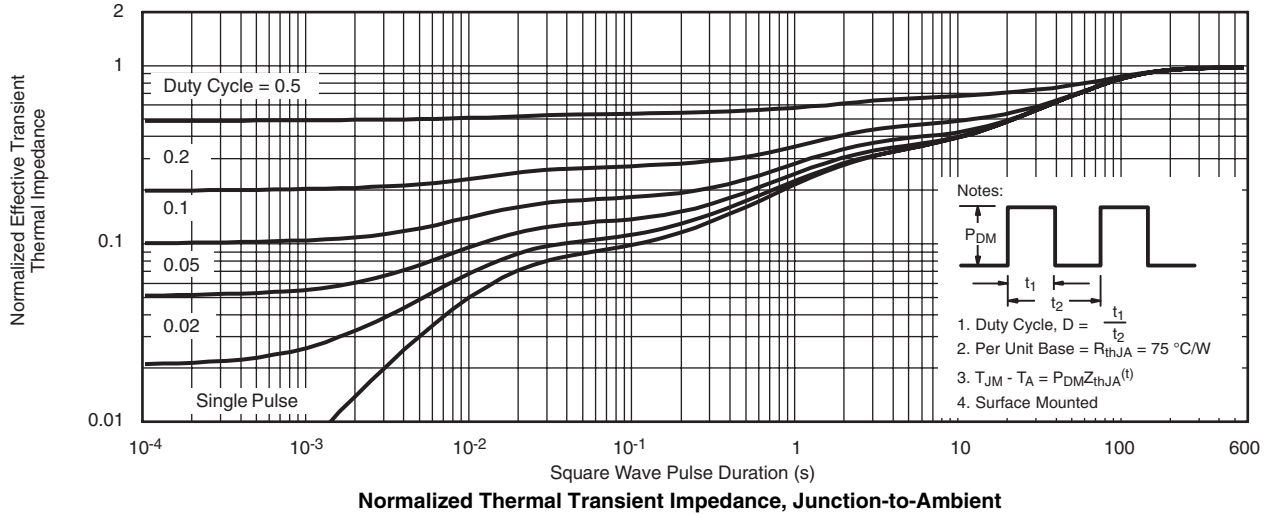
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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