

SPICE Device Model Si4896DY

Vishay Siliconix

N-Channel 80-V (D-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

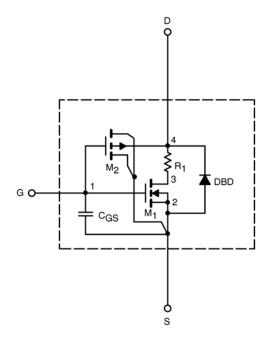
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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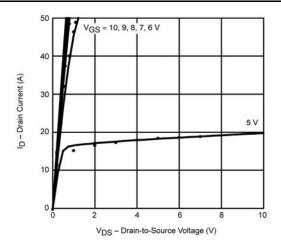
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.63	V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	319	А
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	0.0127	Ω
		V _{GS} = 6 V, I _D = 8 A	0.0175	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A	24	S
Diode Forward Voltage ^a	V_{SD}	I _S = 2.8 A, V _{GS} = 0 V	0.83	V
Dynamic ^b				
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_{D} = 10 A	37.6	nC
Gate-Source Charge	Q _{gs}		7.5	
Gate-Drain Charge	Q_{gd}		11	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 40 V, R_L = 40 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω	18	ns
Rise Time	t _r		22	
Turn-Off Delay Time	t _{d(off)}		30	
Fall Time	t _f		45	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.8 A, di/dt = 100 A/μs	40	1

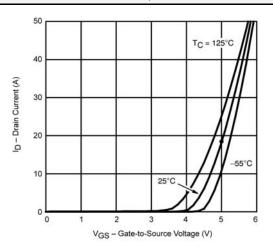
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

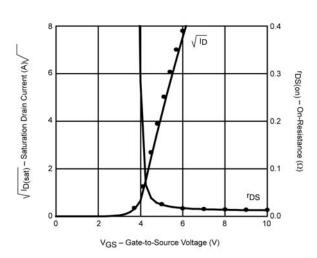


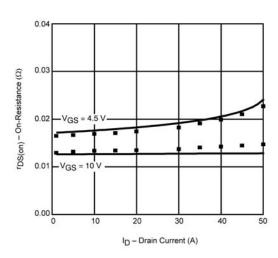
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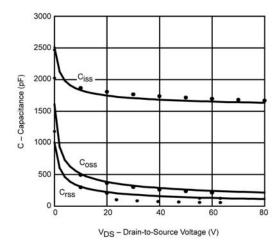
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

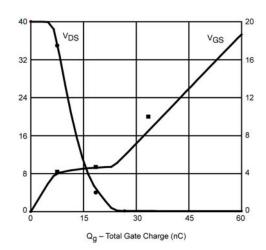












Note: Dots and squares represent measured data



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